



LB11872H

Monolithic Digital IC For Polygonal Mirror Motors Three-Phase Brushless Motor Driver

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Overview

The LB11872H is a three-phase brushless motor driver developed for driving the motors used for the polygonal mirror in laser printers and similar applications. It can implement, with a single IC chip, all the circuits required for polygonal mirror drive, including speed control and driver functions. The LB11872H can implement motor drive within minimal drive noise due to its use of current linear drive.

Features

- Three-phase bipolar current linear drive + midpoint control circuit.
- PLL speed control circuit.
- Speed is controlled by an external clock signal.
- Supports Hall FG operation.
- Built-in output saturation prevention circuit.
- Phase lock detection output (with masking function).
- Includes current limiter, thermal protection, rotor constraint protection, and low-voltage protection circuits on chip.
- On-chip output diodes.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		30	V
Output current	I _O max	T ≤ 500ms	1.2	A
Allowable power dissipation	P _d max1	Independent IC	0.8	W
	P _d max2	*With specified substrate	2.0	W
Operating temperature	T _{opr}		-20 to +80	°C
Storage temperature	T _{stg}		-55 to +150	°C

* When mounted on the specified printed circuit board : 114.3mm × 76.1mm × 1.6mm, glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
Supply voltage range	V_{CC}		10 to 28			V
6.3 V regulator-voltage output current	I_{REG}		0 to -20			mA
LD pin applied voltage	V_{LD}		0 to 28			V
LD pin output current	I_{LD}		0 to 15			mA
FGS pin applied voltage	V_{FG}		0 to 28			V
FGS pin output current	I_{FG}		0 to 10			mA

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = VM = 24\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Supply current 1	I_{CC1}	Stop mode		5	7	mA	
Supply current 2	I_{CC2}	Start mode		17	22	mA	
Output saturation voltages $V_{AGC} = 3.5\text{V}$							
SOURCE (1)	$VSAT1-1$	$I_O = 0.5\text{A}$, $RF = 0\Omega$		1.7	2.2	V	
SOURCE (2)	$VSAT1-2$	$I_O = 1.0\text{A}$, $RF = 0\Omega$		2.0	2.7	V	
SINK (1)	$VSAT2-1$	$I_O = 0.5\text{A}$, $RF = 0\Omega$		0.4	0.9	V	
SINK (2)	$VSAT2-2$	$I_O = 1.0\text{A}$, $RF = 0\Omega$		1.0	1.7	V	
Output leakage current	I_O (LEAK)	$V_{CC} = 28\text{V}$			100	μA	
6.3V Regulator-voltage output							
Output voltage	V_{REG}		5.90	6.25	6.60	V	
Voltage regulation	ΔV_{REG1}	$V_{CC} = 9.5$ to 28V		50	100	mV	
Load regulation	ΔV_{REG2}	$I_{load} = -5$ to -20mA		10	60	mV	
Temperature coefficient	ΔV_{REG3}	Design target value* ¹		0		$\text{mV}/^\circ\text{C}$	
Hall amplifier block							
Input bias current	I_B (HA)	Differential input : 50mVp-p		2	10	μA	
Differential input voltage range	V_{HIN}	SIN wave input	50		*600	mVp-p	
Common-phase input voltage range	V_{ICM}	Differential input : 50mVp-p	2.0		$V_{CC}-2.5$	V	
Input offset voltage	V_{IOH}	Design target value* ¹	-20		20	mV	
FG amplifier and schmitt block (IN1)							
Input amplifier gain	GFG			5		Times	
Input hysteresis (high to low)	V_{SHL}			0		mV	
Input hysteresis (low to high)	V_{SLH}			-10		mV	
Hysteresis width	V_{FGL}	Input conversion	4	7	12	mV	
Low-voltage protection circuit							
Operating voltage	V_{SD}		8.4	8.8	9.2	V	
Hysteresis width	ΔV_{SD}		0.2	0.4	0.6	V	
Thermal protection circuit							
Thermal shutdown operating temperature	T_{SD}	Design target value* ¹ (junction temperature)	150	180		$^\circ\text{C}$	
Hysteresis width	ΔT_{SD}	Design target value* ¹ (junction temperature)		40		$^\circ\text{C}$	
Current limiter operation							
Acceleration limit voltage	V_{RF1}		0.53	0.59	0.65	V	
Deceleration limit voltage	V_{RF2}		0.32	0.37	0.42	V	
Error amplifier							
Input offset voltage	V_{IO} (ER)	Design target value* ¹	-10		10	mV	
Input bias current	I_B (ER)		-1		1	μA	
High-level output voltage	V_{OH} (ER)	$I_{OH} = -500\mu\text{A}$	$V_{REG-1.2}$	$V_{REG-0.9}$		V	
Low-level output voltage	V_{OL} (ER)	$I_{OL} = 500\mu\text{A}$			0.9	1.2	V
DC bias level	V_B (ER)		-5%	1/2 V_{REG}	5%	V	

Note* : Since kickback can occur in the output waveform if the Hall input amplitude is too large, the Hall input amplitudes should be held to under 350mVp-p .

*¹ : This parameter is a design target value and is not measured.

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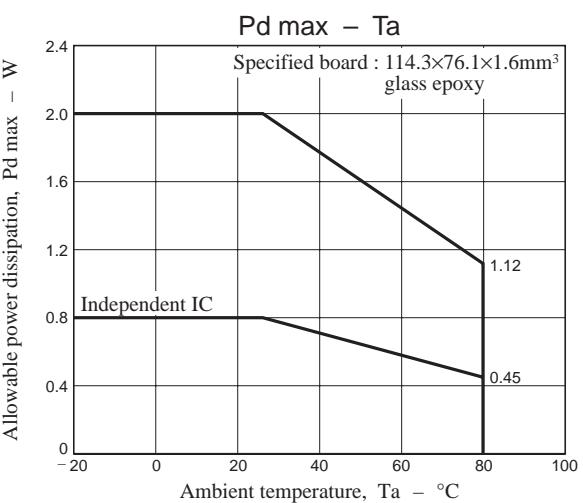
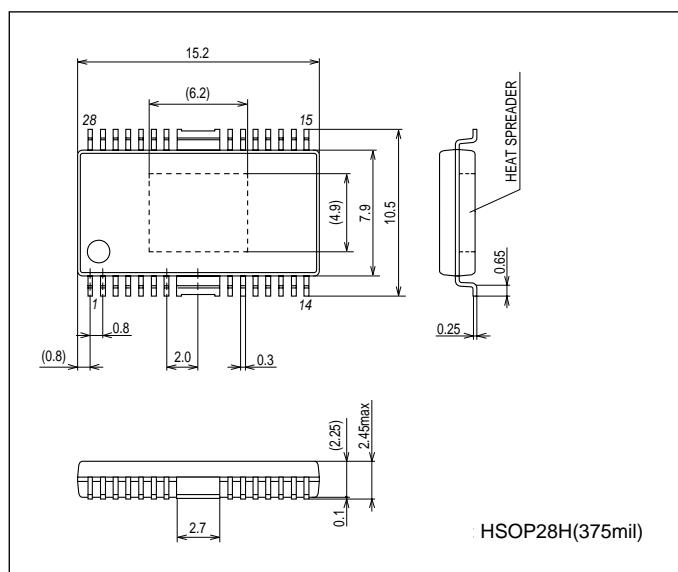
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Phase comparator output						
High-level output voltage	VPDH	$I_{OH} = -100\mu A$	VREG-0.2	VREG-0.1		V
Low-level output voltage	VPDL	$I_{OL} = 100\mu A$		0.2	0.3	V
Output source current	IPD ⁺	VPD = VREG/2			-500	μA
Output sink current	IPD ⁻	VPD = VREG/2	1.5			mA
Lock detection output						
Output saturation voltage	VLD (SAT)	ILD = 10mA		0.15	0.5	V
Output leakage current	ILD (LEAK)	VLD = 28V			10	μA
FG output						
Output saturation voltage	VFG (SAT)	IFG = 5mA		0.15	0.5	V
Output leakage current	IFG (LEAK)	VFG = 28V			10	μA
Drive block						
Dead zone width	VDZ	With the phase is locked	50	100	300	mV
Output idling voltage	VID				6	mV
Forward gain 1	GDF+1	With phase locked	0.4	0.5	0.6	Times
Forward gain 2	GDF+2	With phase unlocked	0.8	1.0	1.2	Times
Reverse gain 1	GDF-1	With phase locked	-0.6	-0.5	-0.4	Times
Reverse gain 2	GDF-2	With phase unlocked	-0.8	-1.0	-1.2	Times
Acceleration command voltage	VSTA		5.0	5.6		V
Deceleration command voltage	VSTO			0.8	1.5	V
Forward limiter voltage	VL1	$R_f = 22\Omega$	0.53	0.59	0.65	V
Reverse limiter voltage	VL2	$R_f = 22\Omega$	0.32	0.37	0.42	V
CSD oscillator circuit						
Oscillation frequency	f _{OSC}	$C = 0.022\mu F$		31		Hz
High-level pin voltage	V _{CSDH}		4.3	4.8	5.3	V
Low-level pin voltage	V _{CSDL}		0.75	1.15	1.55	V
External capacitor charge and discharge current	I _{CHG}		3	5	7	μA
Lock detection delay count	CSDCT1			7		
Clock cutoff protection operating count	CSDCT2			2		
Lock protection count	CSDCT3			31		
Initial reset voltage	V _{RES}			0.60	0.80	V
Clock input block						
External input frequency	f _{CLK}		400		10000	Hz
High-level input voltage	V _{IH} (CLK)	Design target value ^{*1}	2.0		VREG	V
Low-level input voltage	V _{IL} (CLK)	Design target value ^{*1}	0		1.0	V
Input open voltage	V _{IO} (CLK)		2.7	3.0	3.3	V
Hysteresis width	V _{IS} (CLK)	Design target value ^{*1}	0.1	0.2	0.3	V
High-level input current	I _{IH} (CLK)	$V (CLK) = VREG$		140	185	μA
Low-level input current	I _{IL} (CLK)	$V (CLK) = 0V$	-185	-140		μA
S/S pin						
High-level input voltage	V _{IH} (S/S)		2.0		VREG	V
Low-level input voltage	V _{IL} (S/S)		0		1.0	V
Input open voltage	V _{IO} (S/S)		2.7	3.0	3.3	V
Hysteresis width	V _{IS} (S/S)		0.1	0.2	0.3	V
High-level input current	I _{IH} (S/S)	$V (S/S) = VREG$		140	185	μA
Low-level input current	I _{IL} (S/S)	$V (S/S) = 0V$	-185	-140		μA

^{*1} : This parameter is a design target value and is not measured.

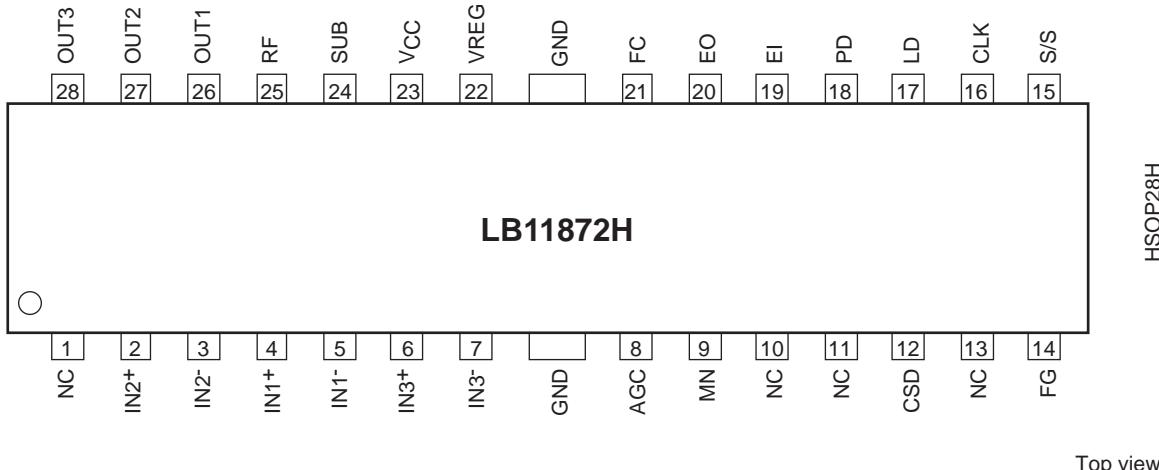
Package Dimensions

unit : mm (typ)

3233B



Pin Assignment



Top view

Truth Table

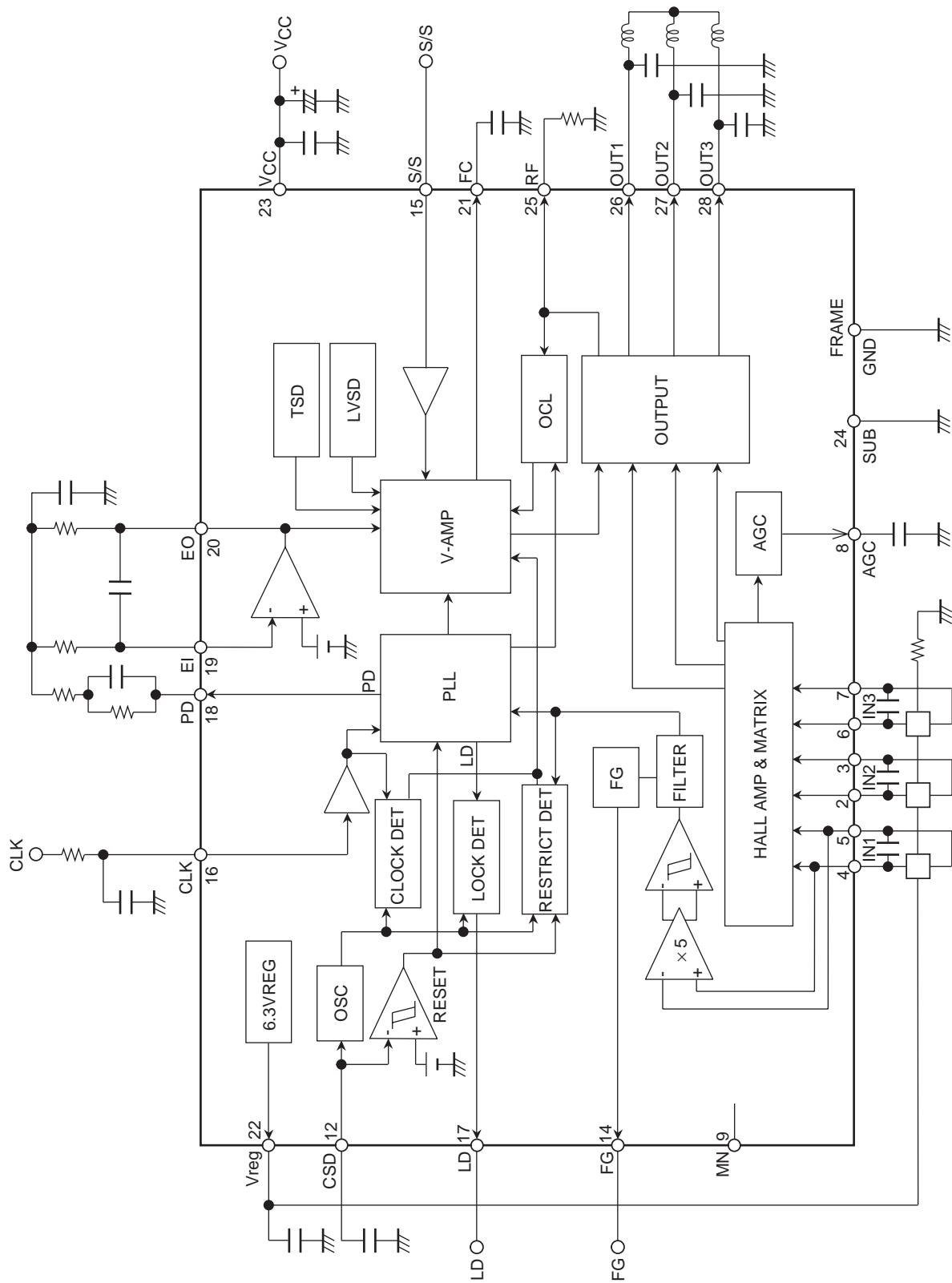
OUT1 to OUT3 (H : Source, L : Sink)

IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

For IN1 to IN3, "H" means that IN^+ is greater than IN^- , and "L" means IN^- is greater than IN^+ .

For OUT1 to OUT3, "H" means the output is a source, and "L" means that it is a sink.

Block Diagram



Pin Functions

Pin No.	Pin name	Function	Equivalent circuit
2	IN2 ⁺	Hall effect sensor signal inputs.	
3	IN2 ⁻	These inputs are high when IN ⁺ is greater than IN ⁻ and low when IN ⁻ is greater than IN ⁺ .	
4	IN1 ⁺	Insert capacitors between the IN ⁺ and IN ⁻ pins to reduce noise.	
5	IN1 ⁻		
6	IN3 ⁺	An amplitude of over 50mVp-p and under 350mVp-p is desirable for the Hall input signals. Kickback can occur in the output waveform if the Hall input amplitude is over 350mVp-p.	
7	IN3 ⁻		
8	AGC	AGC amplifier frequency characteristics correction. Insert a capacitor (about 0.022μF) between this pin and ground.	
9	MN	Monitor pin. This pin should be left open in normal operation.	
12	CSD	Used for both initial reset pulse generation and as the reference time for constraint protection circuits. Insert a capacitor between this pin and ground.	
14	FG	FG pulse output. This is an open-collector output.	
15	S/S	Start/stop control. Low : Start 0 to 1.0V High : Stop 2.0V to VREG This pin goes to the high level when open.	

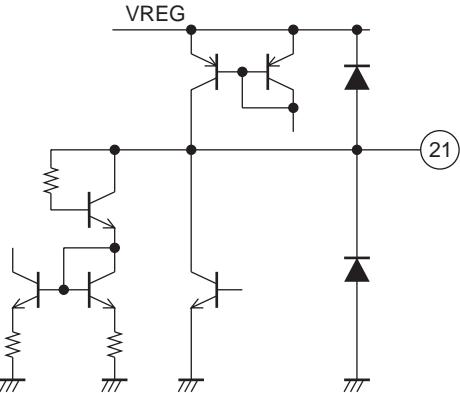
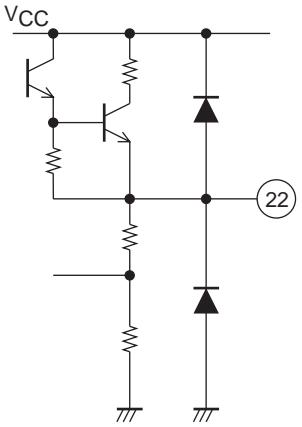
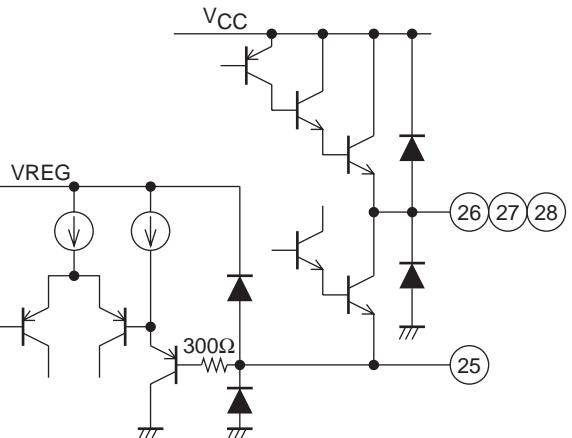
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Pin No.	Pin name	Function	Equivalent circuit
16	CLK	Clock input. Low : 0 to 1.0V High : 2.0V to VREG This pin goes to the high level when open.	
17	LD	Phase locked state detection output. This output goes to the on state when the PLL locked state is detected. This is an open-collector output.	
18	PD	Phase comparator output (PLL output). This pin output the phase error as a pulse signal with varying duty. The output current increases as the duty becomes smaller.	
19	EI	Error amplifier input pin.	
20	EO	Error amplifier output pin. The output current increases when this output is high.	

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Pin No.	Pin name	Function	Equivalent circuit
21	FC	Control amplifier frequency correction. Inserting a capacitor (about 5600pF) between this pin and ground will stop closed loop oscillation in the current control system. The output current response characteristics will be degraded if the capacitor is too large.	
22	VREG	Stabilized power supply (6.3V) Insert a capacitor (about 0.1μF) between this pin and ground for stabilization.	
23	VCC	Power supply.	
24	SUB	SUB pin. Connect this pin to ground.	
25	RF	Output current detection. Insert low-valued resistors (Rf) between these pins and ground. The output current will be limited to the value set by the equation $I_{OUT} = V_L/R_f$.	
26 27 28	OUT1 OUT2 OUT3	Motor drive outputs. If the output oscillates, insert a capacitor (about 0.1μF) between this pin and ground.	
1 10 11 13	NC	No connection (NC) pins. These pins may be used for wiring connections.	
FRAME	GND	Ground.	

LB11920 Description**1. Speed Control Circuit**

This IC adopts a PLL speed control technique and provides stable motor operation with high precision and low jitter. This PLL circuit compares the phase error at the edges of the CLK signal (falling edges) and FG signal (rising edges (low to high transitions) on the IN1 input), and the IC uses the detected error to control the motor speed. During this control operation, the FG servo frequency will be the same as the CLK frequency.

$$f_{FG}(\text{servo}) = f_{CLK}$$

2. Output Drive Circuit

To minimize motor noise, this IC adopts three-phase full-wave current linear drive. This IC also adopts a midpoint control technique to prevent ASO destruction of the output transistors.

Reverse torque braking is used during motor deceleration during speed switching and lock pull-in. In stop mode, the drive is cut and the motor is left in the free-running state.

Since the output block may oscillate depending on the motor actually used, capacitors (about $0.1\mu\text{F}$) must be inserted between the OUT pins and ground.

3. Hall Input Signals

This IC includes an AGC circuit that minimizes the influence on the output of changes in the Hall signal input amplitudes due to the motor used. However, note that if there are discrepancies in the input amplitudes between the individual phases, discrepancies in the output phase switching timing may occur.

An amplitude (differential) of at least 50mVp-p is required in the Hall input signals. However, if the input amplitude exceeds 350mVp-p , the AGC circuit control range will be exceeded and kickback may occur in the output.

If Hall signal input frequencies in excess of 1kHz (the frequency in a single Hall input phase) are used, internal IC heating during startup and certain other times (that is, when the output transistors are saturated) may increase.

Reducing the number of magnetic poles can be effective in dealing with problem.

The IN1 Hall signal is used as the FG signal for speed control internally to the IC. Since noise can easily become a problem, a capacitor must be inserted across this input. However, since this could result in differences between the signal amplitudes of the three phases, capacitors must be inserted across all of the three input phases.

Although VCC can be used as the Hall element bias power supply, using VREG can reduce the chances of problems occurring during noise testing and at other times. If VREG is used, since there is no longer any need to be concerned with the upper limit of the Hall amplifier common-mode input voltage range, bias setting resistors may be used only on the low side.

4. Power Saving Circuit

This IC goes into a power saving state that reduces the current drain in the stop state. The power saving state is implemented by removing the bias current from most of the circuits in the IC. However, the 6.3V regulator output is provided in the power saving state.

5. Reference Clock

Care must be taken to assure that no chattering or other noise is present on the externally input clock signal. Although the input circuit does have hysteresis, if problems do occur, the noise must be excluded with a capacitor.

This IC includes an internal clock cutoff protection circuit. If a signal with a frequency below that given by the formula below is input, the IC will not perform normal control, but rather will operate in intermittent drive mode.

$$f(\text{Hz}) \approx 0.64 \div CCSD \quad CCSD(\mu\text{F}) : \text{The capacitor inserted between the CSD pin and ground.}$$

When a capacitor of $0.022\mu\text{F}$ is used, the frequency will be about 29Hz .

If the IC is set to the start state when the reference clock signal is completely absent, the motor will turn somewhat and then motor drive will be shut off. After the motor stops and the rotor constraint protection time elapses, drive will not be restarted, even if the clock signal is then reapplied. However, drive will restart if the clock signal is reapplied before the rotor constraint protection time elapses.

6. Rotor Constraint Protection Circuit

This IC provides a rotor constraint protection circuit to protect the IC itself and the motor when the motor is constrained physically, i.e. prevented from turning. If the FG signal (edges of one type (rising or falling edges) on the IN1 signal) does not switch within a fixed time, output drive will be turned off. The time constant is determined by the capacitor connected to the CSD pin.

$$<\text{time constant (in seconds)}> \approx 30.5 \times 1.57 \times C_{CSD} (\mu\text{F})$$

If a 0.02 μ F capacitor is used, the protection time will be about 1.05 seconds.

To clear the rotor constraint protection state, the IC must be set to the stopped state or the power must be turned off and reapplied. If there is noise present on the FG signal during the constraint time, the rotor constraint protection circuit may not operate normally.

7. Phase Lock Signal

(1) Phase lock range

Since this IC does not include a counter or similar functionality in the speed control system, the speed error range in the phase locked state cannot be determined solely by IC characteristics. (This is because the acceleration of the changes in the FG frequency influences the range.) When it is necessary to stipulate this characteristic for the motor, the designer must determine this by measuring the actual motor state. Since speed errors occur easily in states where the FG acceleration is large, it is thought that the speed errors will be the largest during lock pull-in at startup and when unlocked due to switching clock frequencies.

(2) Masking function for the phase lock state signal

A stable lock signal can be provided by masking the short-term low-level signals due to hunting during lock pull-in. However, this results in the lock state signal output being delayed by the masking time.

The masking time is determined by the capacitor inserted between the CSD pin and ground.

$$<\text{masking time (seconds)}> \approx 6.5 \times 1.57 \times C_{CSD} (\mu\text{F})$$

When a 0.022 μ F capacitor is used, the masking time will be about 225ms. In cases where complete masking is required, a masking time with fully adequate margin must be used.

8. Initial Reset

To initially reset the logic circuits in start mode, the IC goes to the reset state when the CSD pin voltage goes to zero until it reaches 0.63V. Drive output starts after the reset state is cleared. The reset time can be calculated to a good approximation using the following formula.

$$<\text{reset time (seconds)}> \approx 0.13 \times C_{CSD} (\mu\text{F})$$

A reset time of over 100 μ s is required.

9. Current Limiter Circuit

The current limit value is determined by the resistor Rf inserted between the RF pin and ground.

$$I_{LIM} = V_L/R_f \quad V_L = 0.59V \text{ (typical)} \text{ (during acceleration)} \text{ and } 0.37V \text{ (typical)} \text{ (during deceleration)}$$

10. Power Supply Stabilization

An adequately large capacitor must be inserted between the VCC pin and ground for power supply stabilization. If diodes are inserted in the power supply lines to prevent destruction of the device if the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.

If high-frequency noise is a problem, a ceramic capacitor of about 0.1 μ F must also be inserted in parallel.

11. VREG Stabilization

A capacitor of at least 0.1 μ F must be used to stabilize the VREG voltage, which is the control circuit power supply. The capacitor must be connected as close as possible to the pins.

12. Error Amplifier External Component Values

To prevent adverse influence from noise, the error amplifier external components must be located as close to the IC as possible.

13. FRAME Pin and Heat sink Area

The FRAME pin and the heat sink area function as the control circuit ground terminal. It is desirable that this ground line and the Rf resistor ground line be grounded at a single point at the ground for the electrolytic capacitor. Thermal dissipation can be improved significantly by tightly bonding the metallic surface of the back of the IC package to the PCB with, for example, a solder with good thermal conductivity.

14. CSD Pin

The capacitor connected to the CSD pin influences several operational aspects of this IC, including the rotor constraint protection time and the phase lock signal mask time. The following are possible ways of determining the value of this capacitor.

(1) If removing chattering from the phase lock state signal is most important :

Select a capacitance that can assure an adequate mask time.

(2) If startup time is more important than chattering :

Select a capacitance such that the rotor constraint protection circuit does not operate at startup time and verify that there are no problems with the clock cutoff protection circuit and initial reset time.

Operation of the rotor constraint protection circuit may hinder the study of motor characteristics in the uncontrolled state. It is possible to only operate the initial reset function and not operate the rotor constraint protection circuit by inserting a resistor (about $390\text{k}\Omega$) in parallel with the capacitor between the CSD pin and ground.

15. FC Pin

The capacitor connected to the FC pin is required for current limiter loop phase compensation. If the value is too low, the output will oscillate. If the value is too large, it will be easier for currents in excess of the limit value to flow during the current limit time (time before the circuit operates) in states where the output is saturated. (This is because the control response characteristics become worse.)

16. AGC Pin

A capacitance that allows a certain amount of smoothing of the AGC pin voltage in the motor speed range used must be selected for the capacitor connected to the AGC pin. It is also desirable to use a capacitance that allows the AGC voltage to reach an essentially stabilized voltage before the initial reset is cleared. (If the capacitance is too large, the rate of change of the AGC voltage will become slower.)

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