

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM5N15FU

1. Applications

- High Speed Switching Applications
- Analog Switch Applications

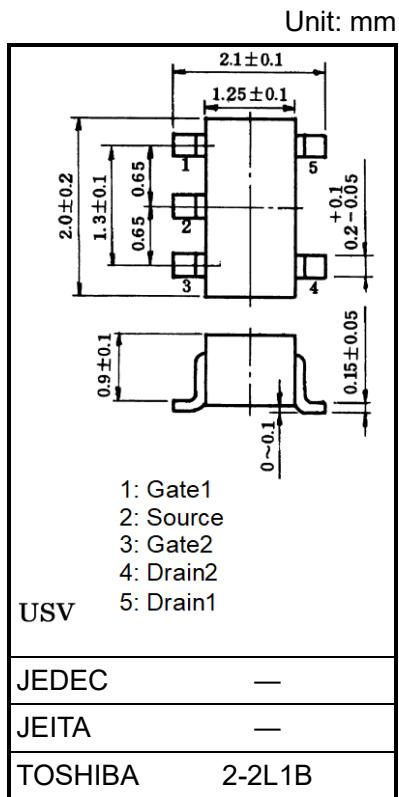
2. Features

- Small package
- Low ON resistance: $R_{DS}(\text{ON}) = 4.0 \Omega \text{ (max)} (@VGS = 4 V)$
- $: R_{DS}(\text{ON}) = 7.0 \Omega \text{ (max)} (@VGS = 2.5 V)$

3. Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

(Q1, Q2 Common) (Note)

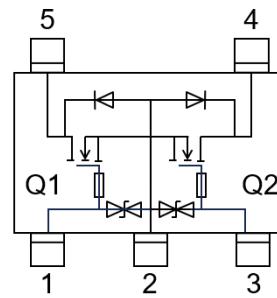
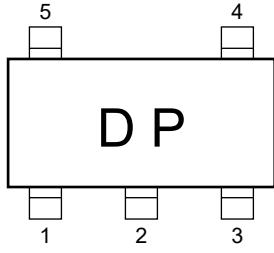
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation ($T_a = 25^\circ\text{C}$)		P_D (Note1)	200	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note1: Total rating

4. Marking, Equivalent Circuit (top view)



5. Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2001-02

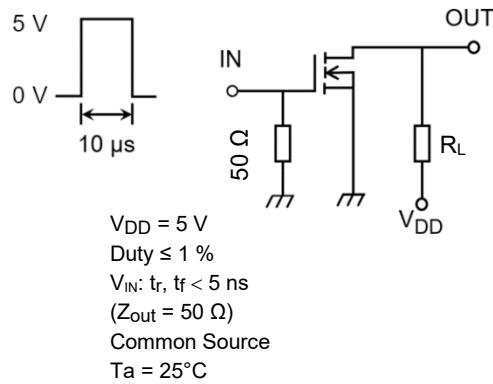
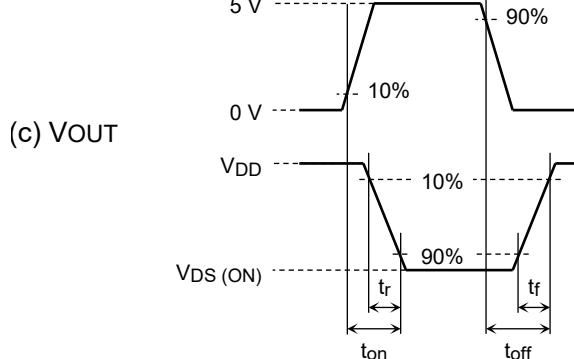
6. Electrical Characteristics

6.1. Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 1	μA
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	30	-	-	V
Drain cut-off current	I_{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.8	-	1.5	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 10 \text{ mA}$	25	-	-	mS
Drain-Source ON resistance	$R_{DS(\text{ON})}$	$I_D = 10 \text{ mA}, V_{GS} = 4 \text{ V}$	-	2.2	4.0	Ω
		$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$	-	4.0	7.0	
Input capacitance	C_{iss}	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	7.8	-	pF
Reverse transfer capacitance	C_{rss}		-	3.6	-	pF
Output capacitance	C_{oss}		-	8.8	-	pF
Switching time	Turn-on time	$V_{DD} = 5 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0 \text{ to } 5 \text{ V}$ See 6.2	-	50	-	ns
	Turn-off time		-	180	-	

6.2. Switching Time Test Circuit (Q1, Q2 common)

(a) Test circuit

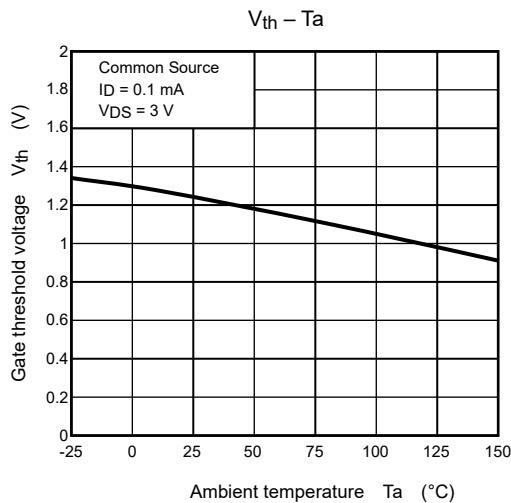
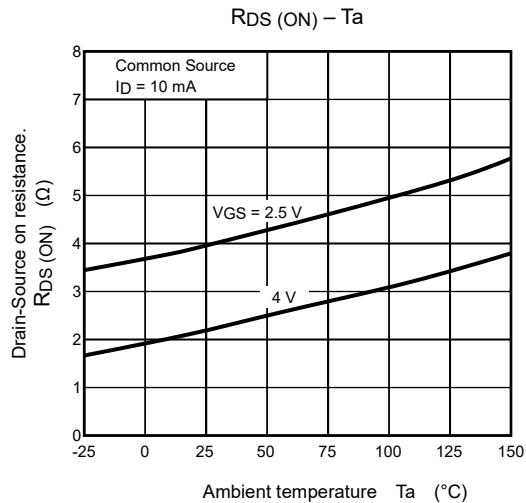
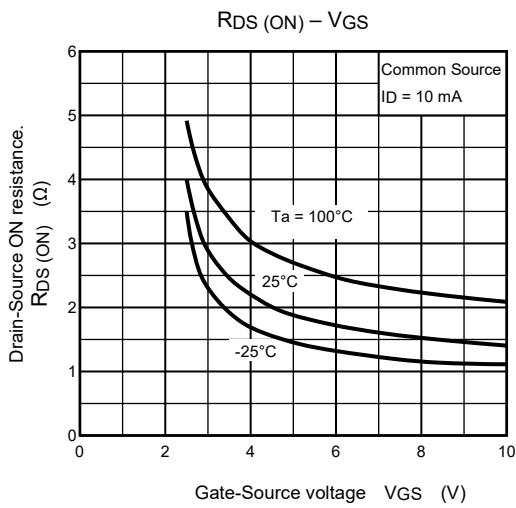
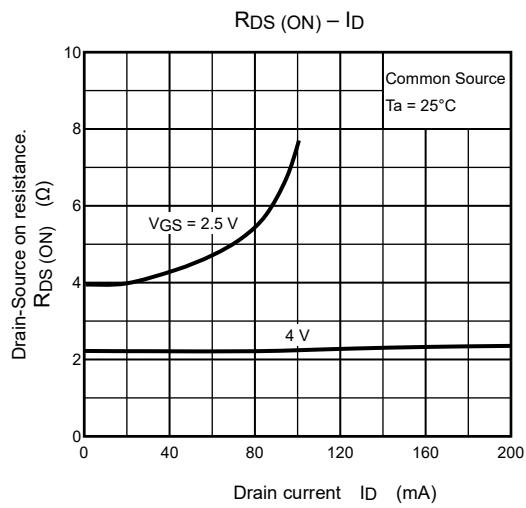
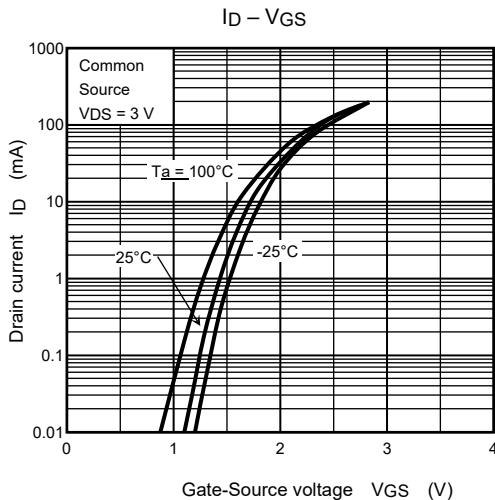
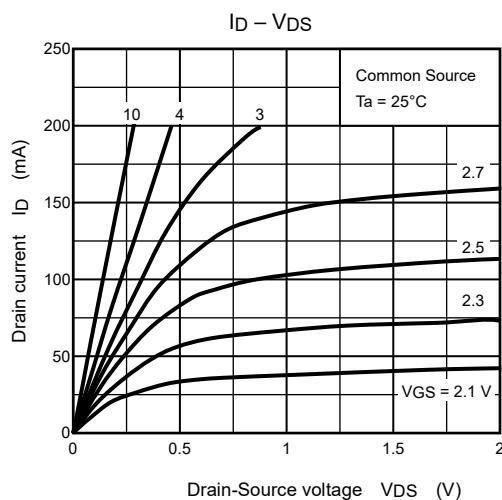
(b) V_{IN} (c) V_{OUT}

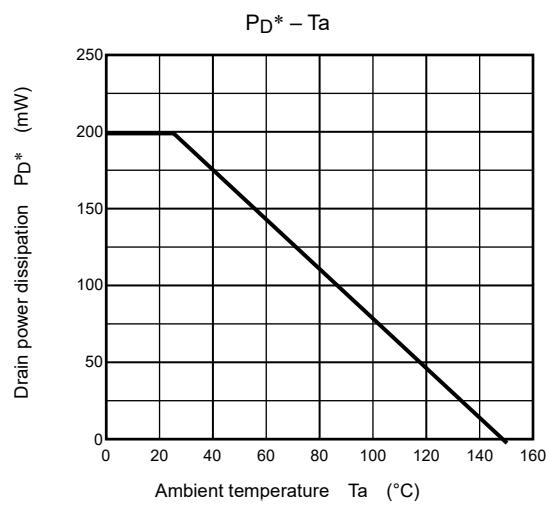
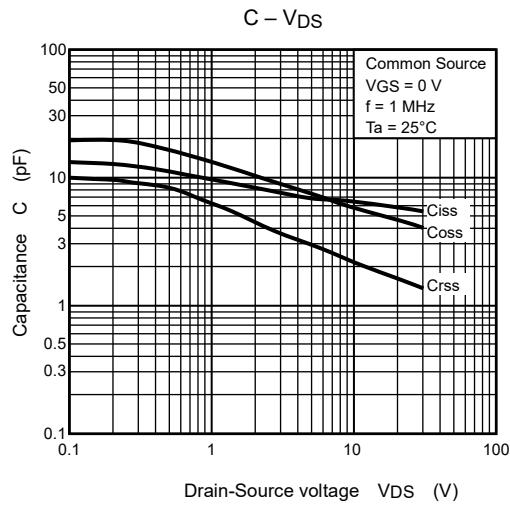
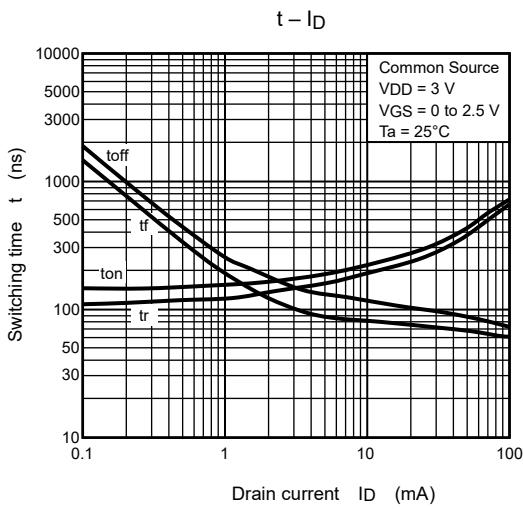
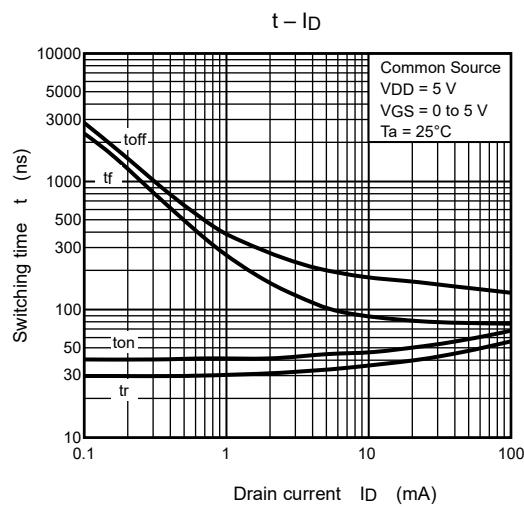
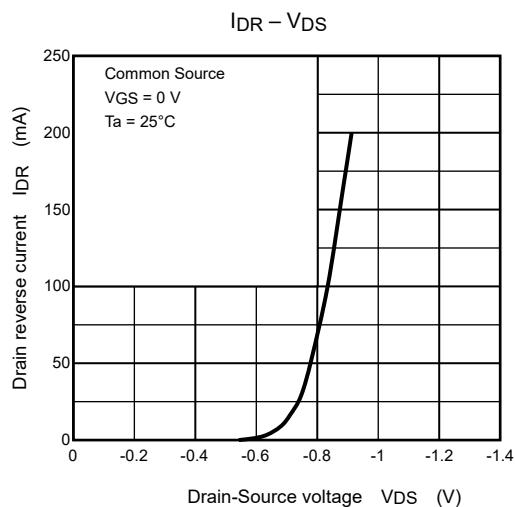
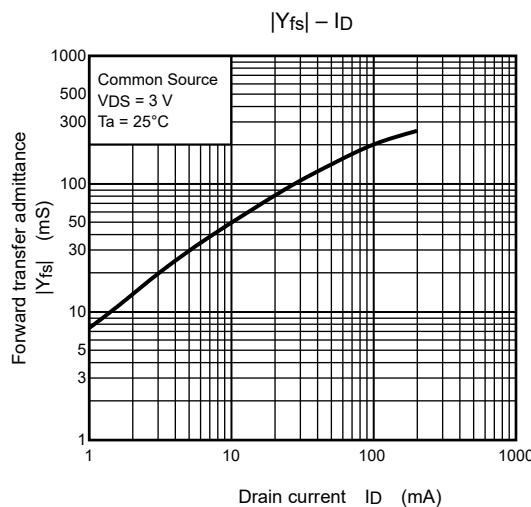
6.3. Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(\text{on})}$ requires higher voltage than V_{th} and $V_{GS(\text{off})}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(\text{off})} < V_{th} < V_{GS(\text{on})}$)

Please take this into consideration for using the device.

7. Characteristic Chart(Q1, Q2 common) (Note)





Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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