Bipolar Power Transistors 40 V, 3.0 A, Low VCE(sat) PNP Transistor

NSS40300CT

onsemi's e^{2}PowerEdge family of low $V_{CE(sat)}$ transistors are surface mount devices featuring ultra-low saturation voltage, $V_{CE(sat)}$, and high current gain capability. These are designed for use in lower voltage, high speed switching applications where affordable efficient energy control is important.

Housed in an ultra slim LFPAK4 5x6 package, typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, digital cameras and MP3 players where PCB space is at a premium. The LFPAK4 5x6 package also contains wettable flanks which are a requirement for the automotive industry's optical inspection methods that are implemented in end applications such as air bag deployment, powertrain control units, and instrument clusters.

Features

- Complement to NSS40301CT
- Ultra-slim LFPAK4 Package (5 x 6 mm) with Wettable Flanks
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

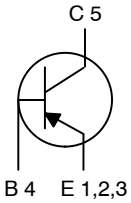
MAXIMUM RATINGS (T_C = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Base Current – Continuous	I_B	1.0	Adc
Collector Current – Continuous	I_C	3.0	Adc
Collector Current – Peak	I_{CM}	5.0	Adc
Total Power Dissipation Total P_D @ T_A = 25 °C (Note 1) Total P_D @ T_A = 25 °C (Note 2)	P_D	 2.0 0.80	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

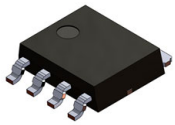
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 1″ sq. (645 sq. mm) Collector pad on FR-4 bd material.
2. Mounted on 0.012″ sq. (7.6 sq. mm) Collector pad on FR-4 bd material.

PNP TRANSISTOR
3.0 AMPERES
40 VOLTS

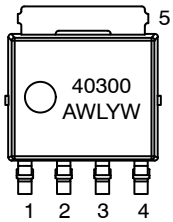


Schematic



LFPAK4 5x6
CASE 760AB

MARKING DIAGRAM



(Top View)

40300	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case Junction-to-Ambient on 1″ sq. (645 sq. mm) Collector pad on FR-4 bd material Junction-to-Ambient on 0.012″ sq. (7.6 sq. mm) Collector pad on FR-4 bd material	 $R_{\theta JA}$ $R_{\theta JA}$	 58 149	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	40			Vdc
Emitter-Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0			Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc)	I_{CBO}			100	nAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc)	I_{EBO}			100	nAdc
ON CHARACTERISTICS (Note 3)					
Collector-Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$			 0.070 0.150 0.400	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$			1.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$			0.9	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 200 175 100		 600	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{ob}		40		pF
Input Capacitance (V_{EB} = 5.0 Vdc, f = 1.0 MHz)	C_{ib}		130		pF
Current-Gain – Bandwidth Product (Note 4) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T		 160		MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$

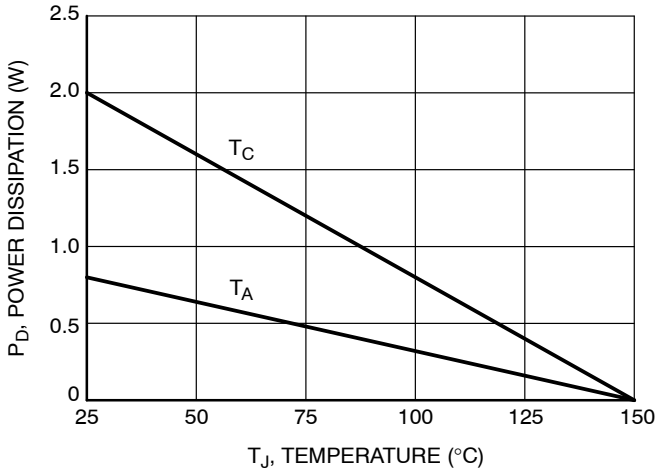

Figure 1. Power Derating

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TYPICAL CHARACTERISTICS

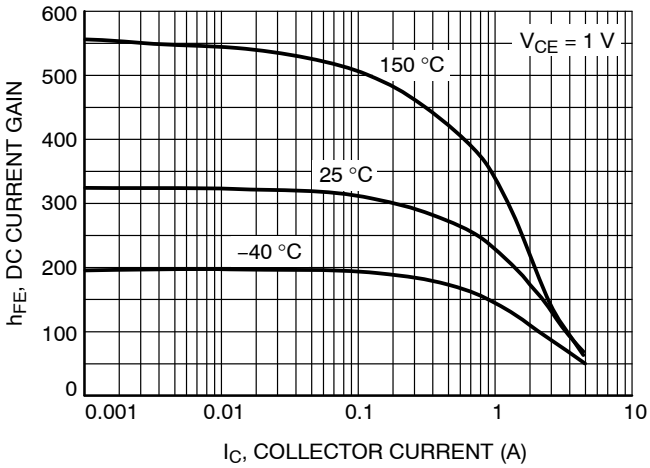

Figure 2. DC Current Gain

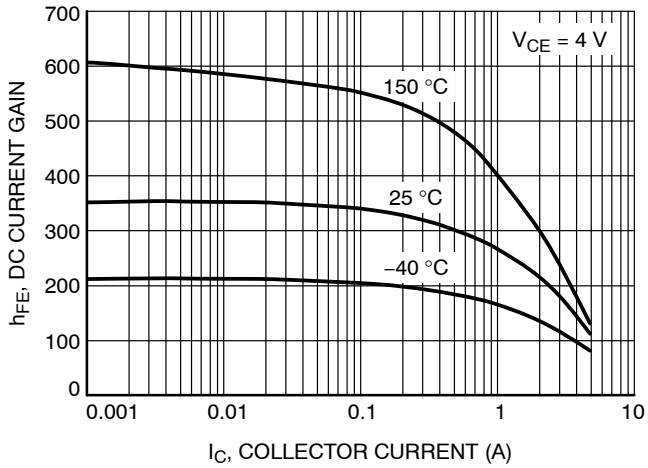

Figure 3. DC Current Gain

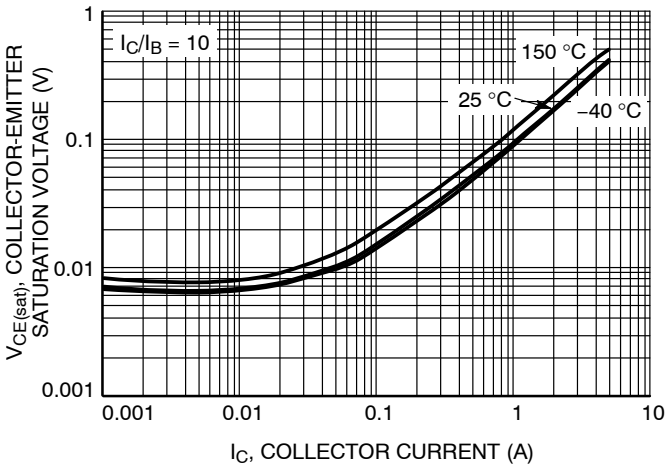

Figure 4. Collector-Emitter Saturation Voltage

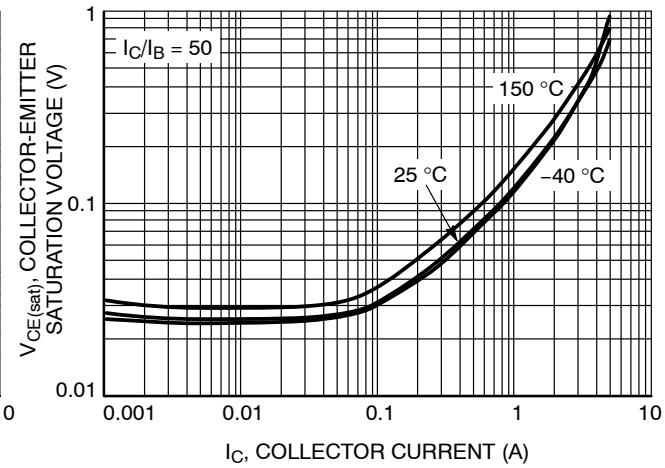

Figure 5. Collector-Emitter Saturation Voltage

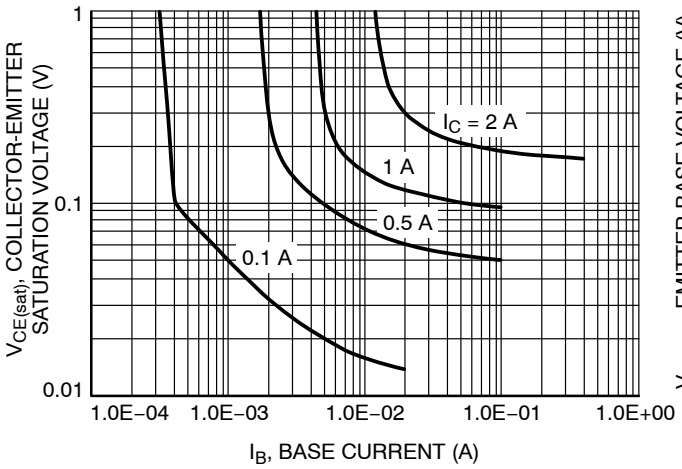

Figure 6. Collector Saturation Region

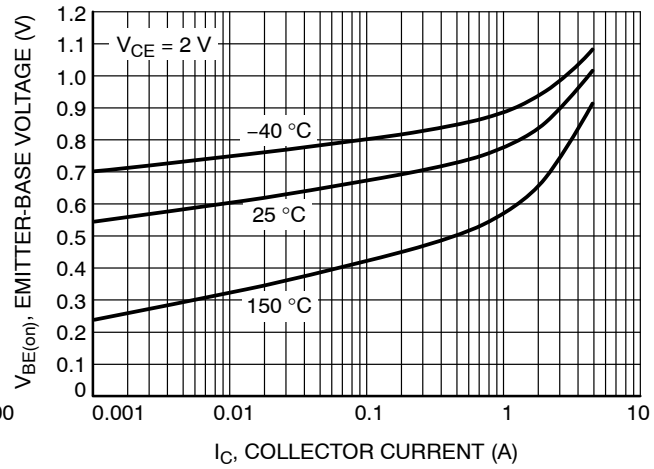

Figure 7. $V_{BE(on)}$ Voltage

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TYPICAL CHARACTERISTICS

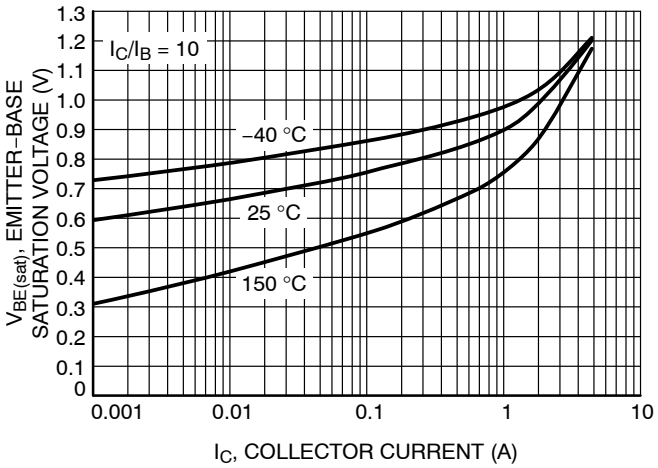

Figure 8. Base-Emitter Saturation Voltage

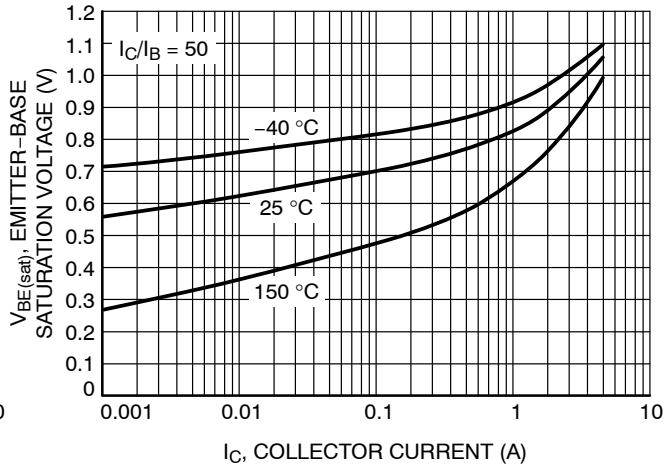

Figure 9. Base-Emitter Saturation Voltage

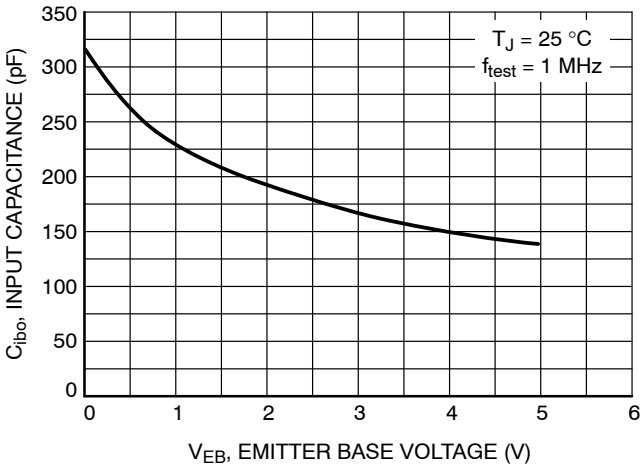

Figure 10. Input Capacitance

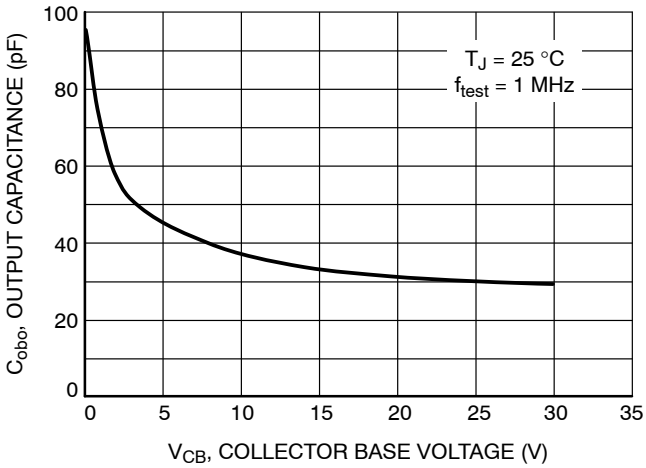

Figure 11. Output Capacitance

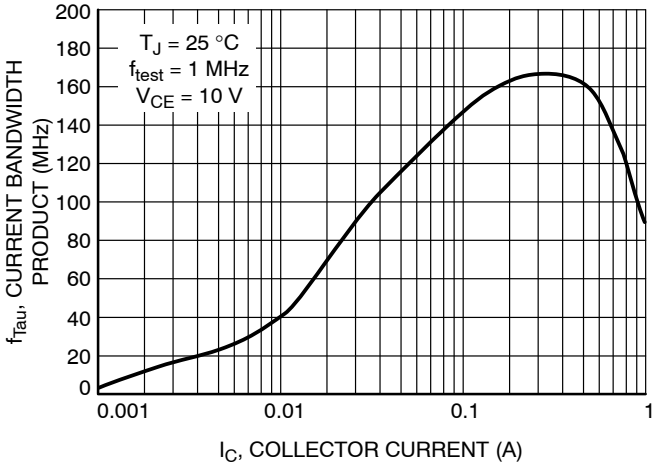

Figure 12. Current-Gain Bandwidth Product

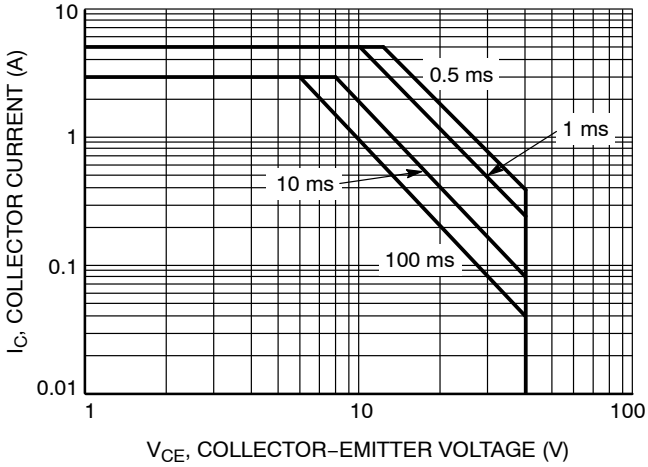

Figure 13. Safe Operating Area

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ORDERING INFORMATION

Device	Package	Shipping†
NSS40300CTWG	LFPAK4 5x6 (Pb-Free)	3,000 / Tape & Reel
NSV40300CTWG*	LFPAK 5x6 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

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REVISION HISTORY

Revision	Description of Changes	Date
3	Revision to change document formatting only	1/13/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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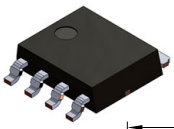
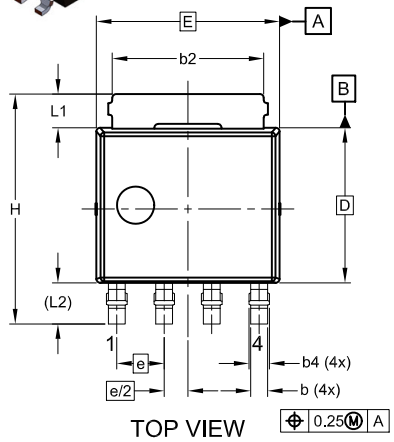
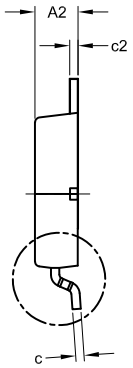
LFPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

DATE 22 MAY 2024



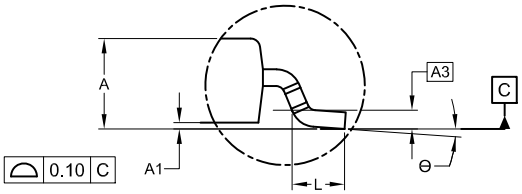


TOP VIEW

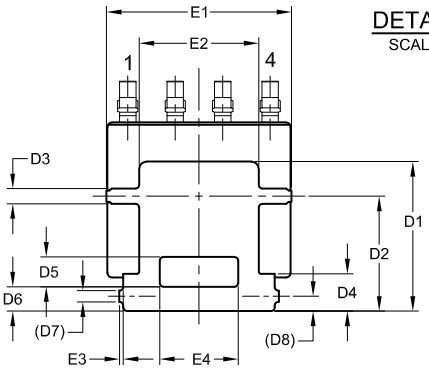


SIDE VIEW

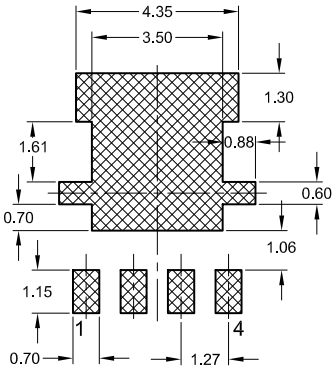
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.



DETAIL 'A'
SCALE: 2:1



BOTTOM VIEW

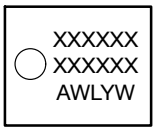


RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
θ	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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DESCRIPTION:	LFPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

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