ESD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

ESD8351P2, SZESD8351P2

The ESD8351P2 ESD protection diode is designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.55 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
  ISO 10605
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 2.0
- eSATA

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD) ISO 10605 330 pF / 2 kΩ Contact	ESD ESD ESD	±15 ±15 ±30	kV kV kV
Maximum Peak Pulse Current 8/20 μs @ T_A = 25°C	I_{pp}	5.0	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

This document contains information on some products that are still under development. **onsemi** reserves the right to change or discontinue these products without notice.

MARKING DIAGRAM



SOD−923
CASE 514AB

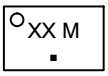


AC = Specific Device Code
M = Date Code



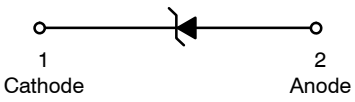
SCALE 8:1

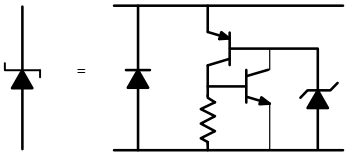
X2DFN2
CASE 714AB
(In Development)



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONFIGURATION AND SCHEMATIC





ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

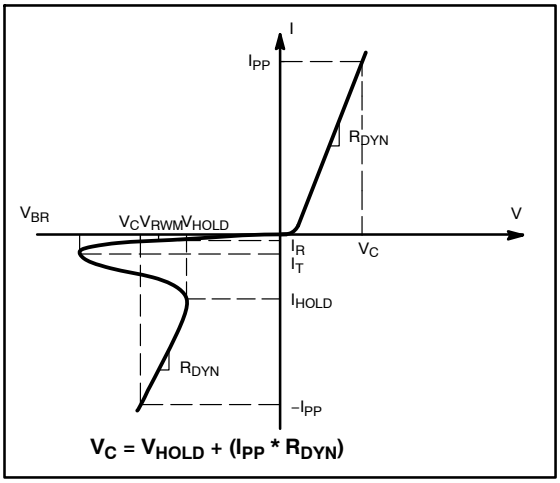
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND ESD8351P2T5G ESD8351N2T5G			3.3 3.7	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5	7.0	7.8	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND ESD8351P2T5G V_{RWM} = 3.7 V, I/O Pin to GND ESD8351N2T5G			500 1.0	nA μA
Holding Reverse Voltage	V_{HOLD}	I/O Pin to GND		1.15		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND		20		mA
Clamping Voltage TLP (Note 2) See Figures 1 through 11	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		5.7	6.5	V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		8.3	10	
Clamping Voltage (Note 3)	V_C	I_{PP} = 5 A } t_p = 8 x 20 μs		5.7	6.5	V
Dynamic Resistance	R_{DYN}	Pin1 to Pin2 Pin2 to Pin1		0.44 0.37		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 Mhz V_R = 0 V, f = 2.5 Ghz		0.37 0.35	0.55 0.45	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 8 and 9 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.
3. Non−repetitive current pulse at T_A = 20°C, per IEC 61000−4−5 waveform.

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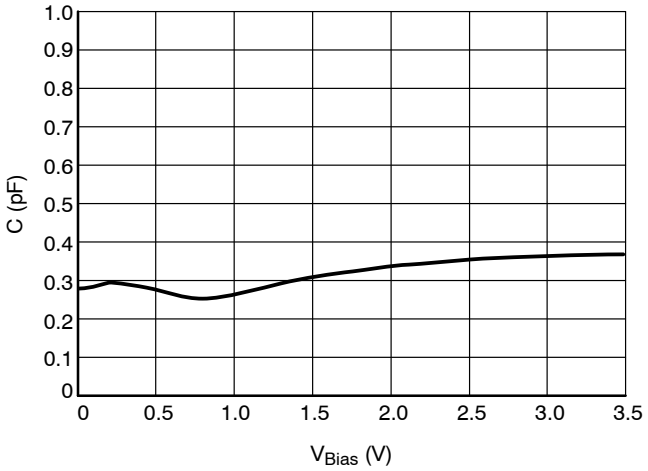


Figure 1. CV Characteristics

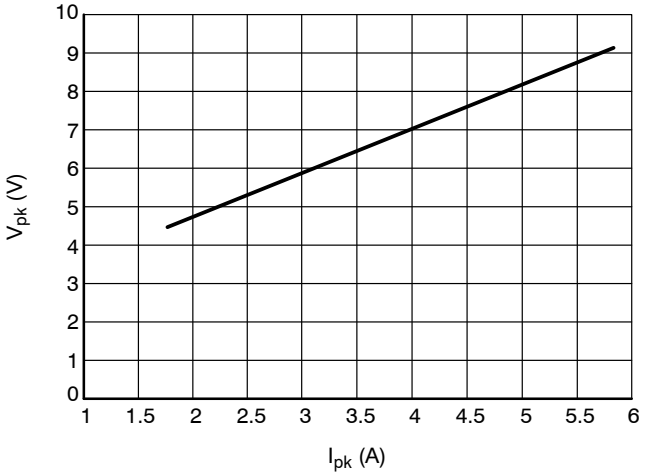


Figure 2. Clamping Voltage vs Peak Pulse Current (t_p = 8/20 μs)

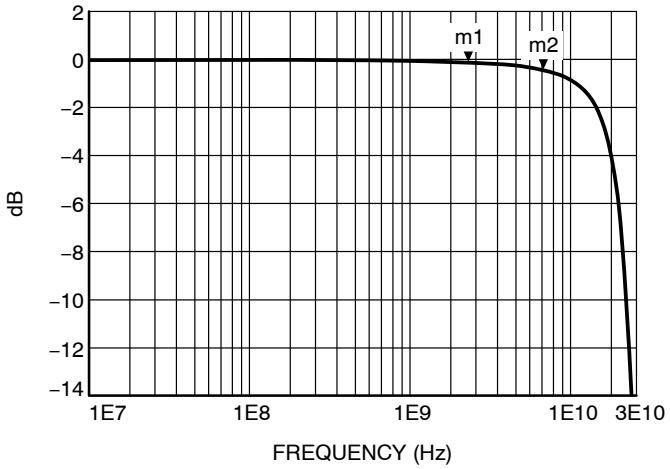


Figure 3. RF Insertion Loss

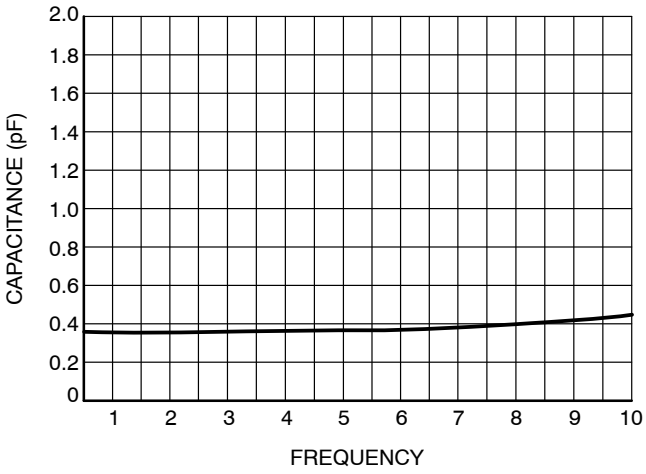


Figure 4. Capacitance over Frequency

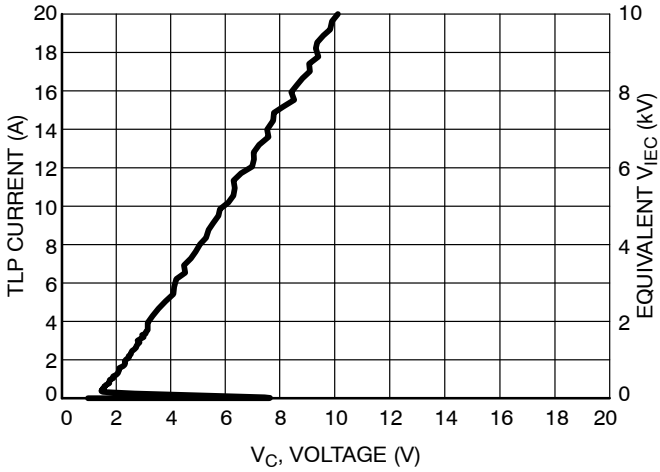


Figure 5. Positive TLP I−V Curve

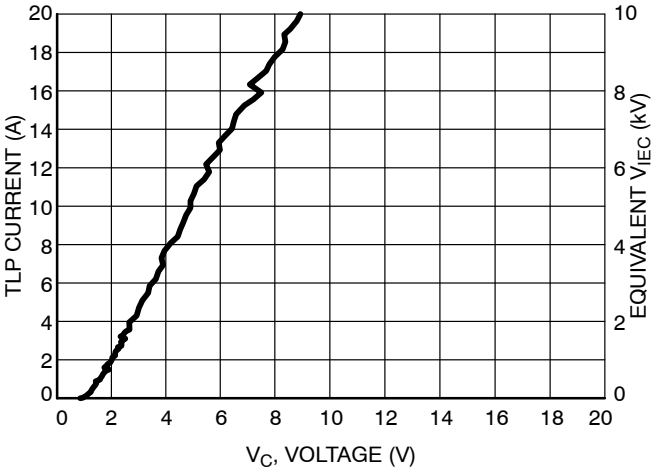


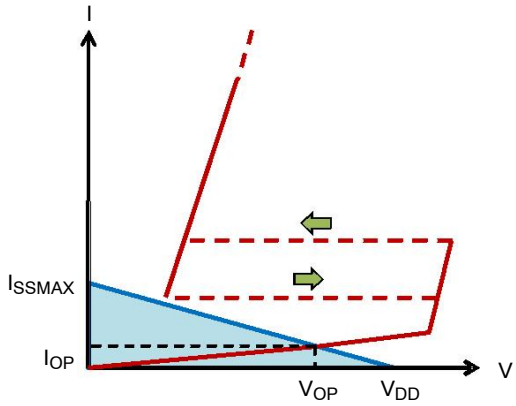
Figure 6. Negative TLP I−V Curve

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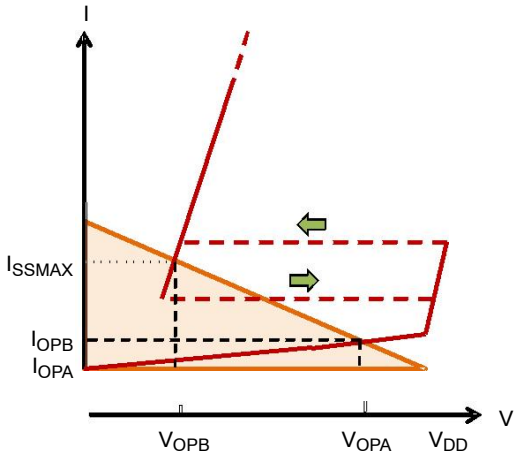
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Latch−Up Considerations

onsemi's 8000 series of ESD protection devices utilize a snap−back, SCR type structure. By using this technology, the potential for a latch−up condition was taken into account by performing load line analysis of common high speed serial interfaces. Example load lines for latch−up free applications and applications with the potential for latch−up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch−up free load line case, the IV characteristic of the snapback protection device intersects the load−line in one unique point (V_{OP}, I_{OP}). This is the only stable operating point of the circuit and the system is therefore latch−up free. In the non−latch up free load line case, the IV characteristic of the snapback protection device intersects the load−line in two points (V_{OPA}, I_{OPA}) and (V_{OPB}, I_{OPB}). Therefore in this case, the potential for latch−up exists if the system settles at (V_{OPB}, I_{OPB}) after a transient. Because of this, ESD8351P2 should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch−up. Please refer to Application Note AND9116/D for a more in−depth explanation of latch−up considerations using ESD8000 series devices.



ESD8351P2 Latch − up free:
USB 2.0 LS/FS, USB 2.0 HS, USB 3.0 SS, DisplayPort



ESD8351P2 Potential Latch − up:
HDMI 1.4/1.3a TMDS

Figure 7. Example Load Lines for Latch−up Free Applications and Applications with the Potential for Latch−up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH−UP FREE APPLICATIONS

Application	VBR (min) (V)	IH (min) (mA)	VH (min) (V)	onsemi ESD8000 Series Recommended PN
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004, ESD8351P2
USB 2.0 HS	0.482	N/A	1.0	ESD8004, ESD8351P2
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006, ESD8351P2
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006, ESD8351P2

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IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

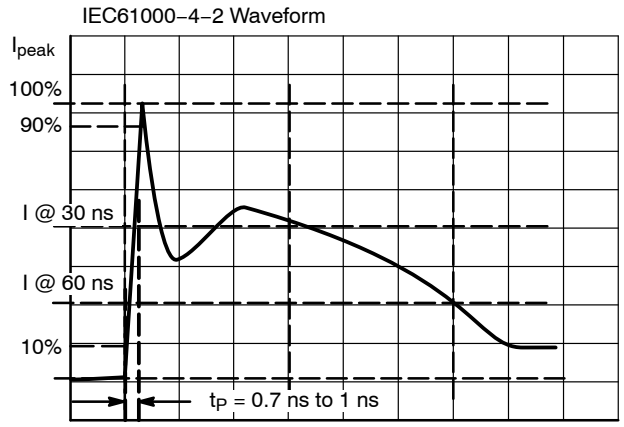


Figure 8. IEC61000−4−2 Spec

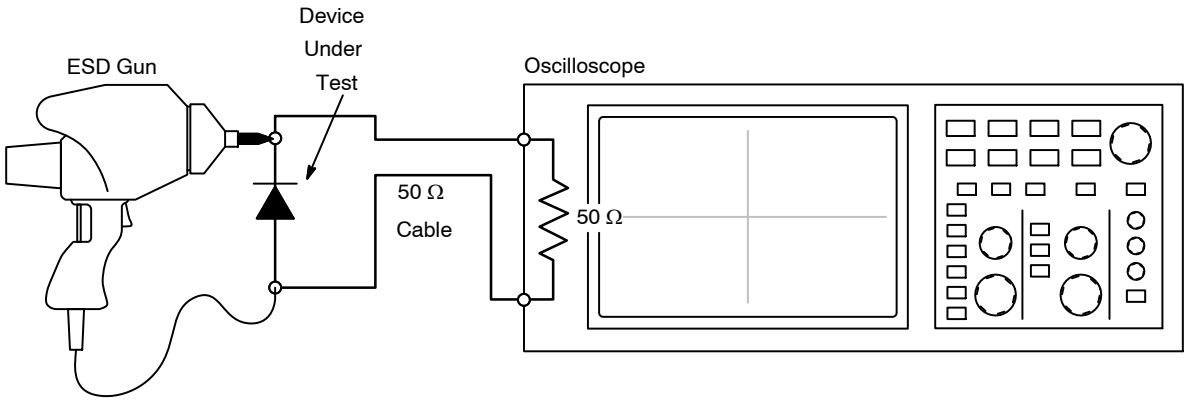


Figure 9. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

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Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 10. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 11 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

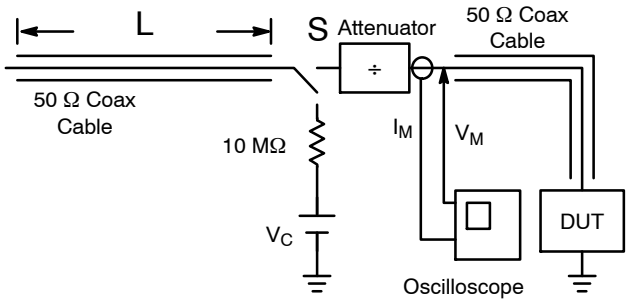


Figure 10. Simplified Schematic of a Typical TLP System

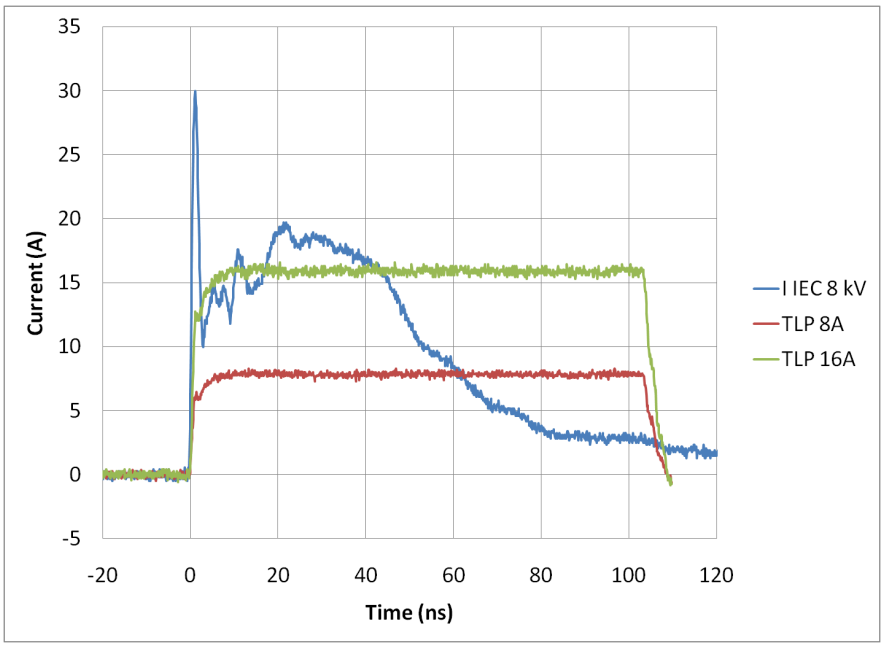


Figure 11. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

ORDERING INFORMATION

Device	Package	Shipping†
ESD8351P2T5G, SZESD8351P2T5G*	SOD−923 (Pb−Free)	8000 / Tape & Reel
ESD8351N2T5G (In Development)	X2DFN2 (Pb−Free)	8000 / Tape & Reel

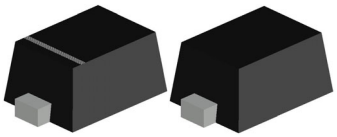
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

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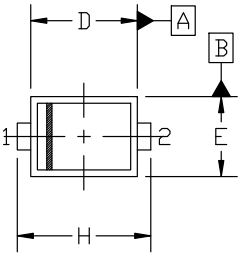
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PACKAGE DIMENSIONS

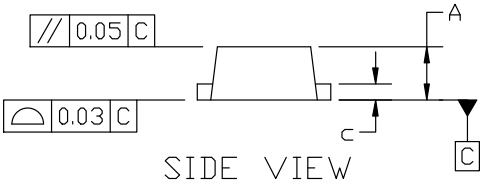


SOD−923 0.80x0.60x0.37
CASE 514AB
ISSUE E

DATE 08 FEB 2024

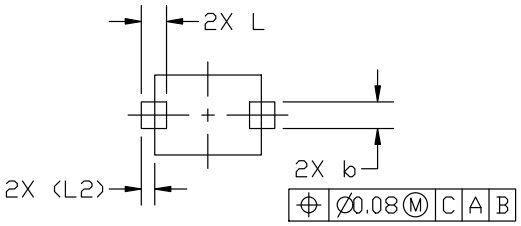


TOP VIEW



SEATING PLANE

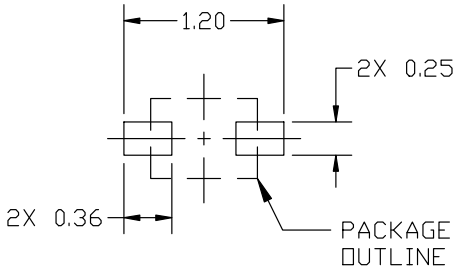
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSION L WILL NOT EXCEED 0.30mm.

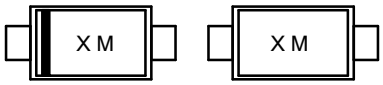
MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.15	0.20	0.25
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

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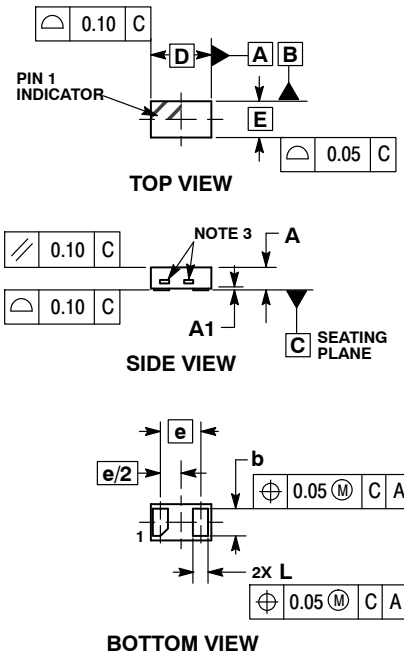
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PACKAGE DIMENSIONS

X2DFN2 1.0x0.6, 0.65P
CASE 714AB
ISSUE B

SCALE 8:1

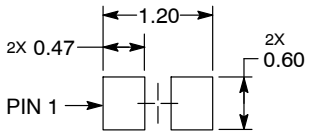
DATE 21 NOV 2017



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	---	0.03	0.05
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30

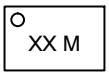
RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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