# 2.5V to 4.5V, 0.6A 1ch Synchronous Buck Converter with Integrated FET

## BD9161FVM

### General Description

The BD9161FVM is ROHM's high efficiency step-down switching regulator designed to produce a voltage as low as 1.2V from a supply voltage of 3.3V. It offers high efficiency by using pulse skip control technology and synchronous switches and provides fast transient response to sudden load changes by implementing current mode control.

### Features

- Fast Transient Response because of Current Mode Control System.
- High Efficiency for All Load Ranges because of Synchronous Switches (Nch/Pch FET)
- 100% Duty Function.
- Soft-Start Function.
- Thermal Shutdown and ULVO Functions.
- Short-Circuit Protection with Time Delay Function.
- Shutdown Function.

### Applications

Power Supply for LSI including HDD, DVD, CPU and ASIC

### Key Specifications

- Input Voltage Range: 2.5V to 4.5V
- Output Voltage Range: 1.0V to 3.3V
- Output Current: 0.6A(Max)
- Switching Frequency: 1MHz(Typ)
- Pch FET ON-Resistance: 0.35Ω(Typ)
- Nch FET ON-Resistance: 0.37Ω(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -25°C to +85°C

### Package

W(Typ) x D(Typ) x H(Max)




**MSOP8**
2.90 mm x 4.00 mm x 0.90 mm

### Typical Application Circuit

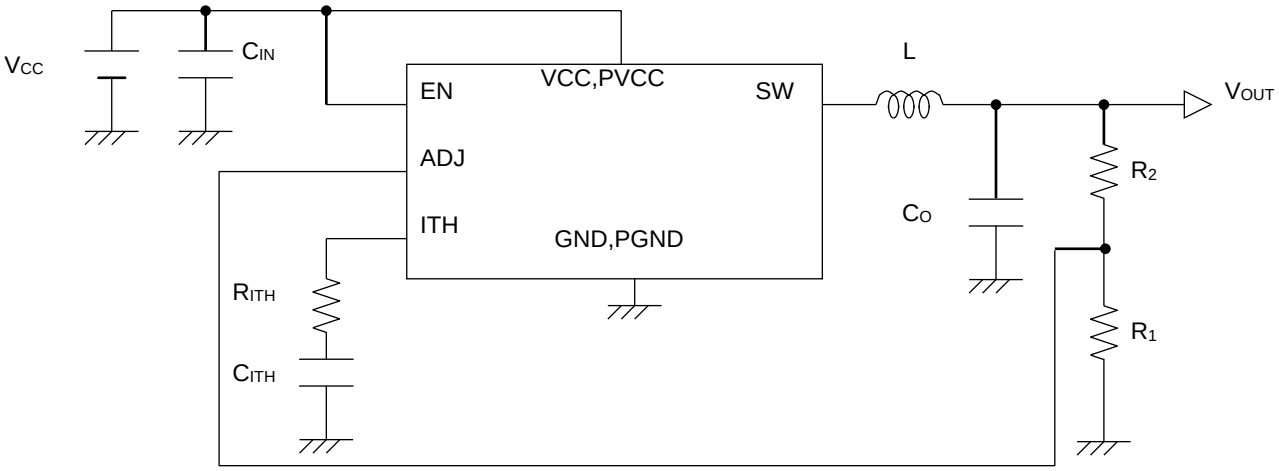



Figure 1. Typical Application Circuit


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## Pin Configuration

(TOP VIEW)

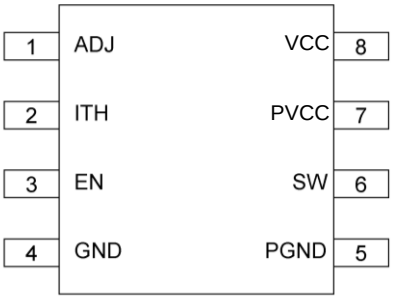



Figure 2. Pin Configuration

## Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | ADJ | Output voltage detection pin |
| 2 | ITH | GmAmp output pin/connected to phase compensation capacitor |
| 3 | EN | Enable pin (active high) |
| 4 | GND | Ground pin |
| 5 | PGND | Power switch ground pin |
| 6 | SW | Power switch node |
| 7 | PVCC | Power switch supply pin |
| 8 | VCC | Power supply input pin |

## Block Diagram

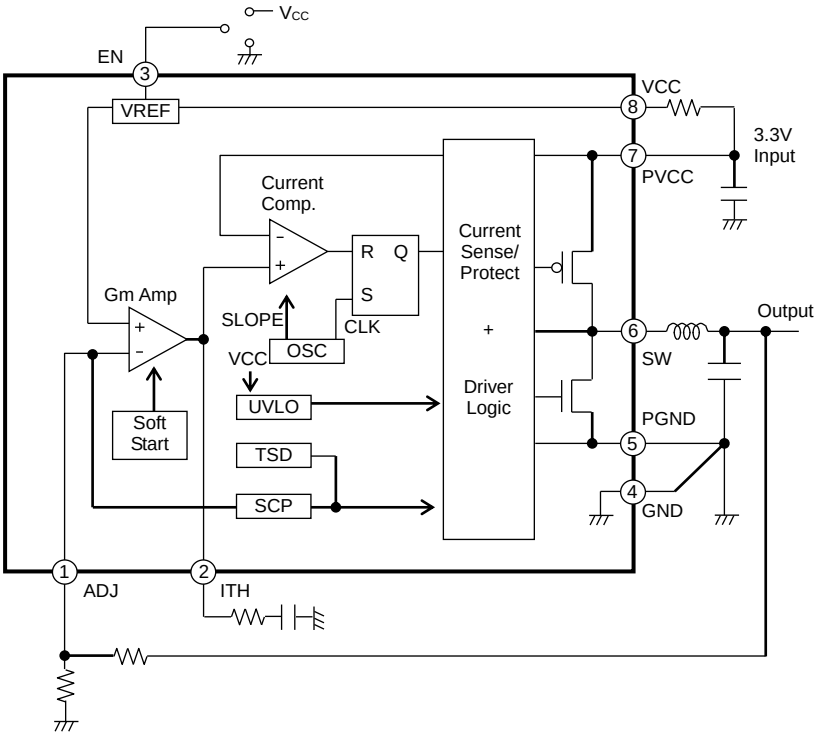



Figure 3. Block Diagram


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## Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| VCC Voltage | $V_{CC}$ | -0.3 to +7 (Note 1) | V |
| PVCC Voltage | $PV_{CC}$ | -0.3 to +7 (Note 1) | V |
| EN Voltage | $V_{EN}$ | -0.3 to +7 | V |
| SW, ITH Voltage | $V_{SW}$,$V_{ITH}$ | -0.3 to +7 | V |
| Power Dissipation 1 | Pd1 | 0.38(Note 2) | W |
| Power Dissipation 2 | Pd2 | 0.58(Note 3) | W |
| Operating Temperature Range | Topr | -25 to +85 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Maximum Junction Temperature | Tjmax | +150 | °C |

(Note 1) Pd should not be exceeded.
(Note 2) Reduced by 7.2mW/°C for Ta over 25°C
(Note 3) Reduced by 31.2mW/°C for Ta over 25°C. Mounted on 70mm x 70mm x 1.6mm Glass Epoxy PCB.
**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions (Ta=25°C)

| Parameter | Symbol | Limit | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| VCC Voltage | $V_{CC}$(Note 4) | 2.5 | 3.3 | 4.5 | V |
| PVCC Voltage | $PV_{CC}$(Note 4) | 2.5 | 3.3 | 4.5 | V |
| EN Voltage | $V_{EN}$ | 0 | - | $V_{CC}$ | V |
| Output Voltage Setting Range | $V_{SW}$,$V_{ITH}$ | 1.0 | - | 3.3 | V |
| SW, ITH Average Output Current | $I_{SW}$(Note 4) | - | - | 0.6 | A |

(Note 4 ) Pd should not be exceeded.

## Electrical Characteristics (Ta=25°C,$V_{CC}$ =$PV_{CC}$ =3.3V, $V_{EN}$=$V_{CC}$, unless otherwise specified.)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Standby Current | $I_{STB}$ | - | 0 | 10 | μA | EN=GND |
| Bias Current | $I_{CC}$ | - | 200 | 400 | μA | |
| EN Low Voltage | $V_{ENL}$ | - | GND | 0.8 | V | Standby mode |
| EN High Voltage | $V_{ENH}$ | 2.0 | $V_{CC}$ | - | V | Active mode |
| EN Input Current | $I_{EN}$ | - | 1 | 10 | μA | $V_{EN}$=3.3V |
| Oscillation Frequency | $f_{OSC}$ | 0.8 | 1 | 1.2 | MHz | |
| Pch FET ON Resistance | $R_{ONP}$ | - | 0.35 | 0.6 | Ω | $PV_{CC}$=3.3V |
| Nch FET ON Resistance | $R_{ONN}$ | - | 0.37 | 0.68 | Ω | $PV_{CC}$=3.3V |
| Output Voltage | $V_{OUT}$ | 0.784 | 0.8 | 0.816 | V | |
| ITH Sink Current | $I_{THSI}$ | 10 | 20 | - | μA | $V_{OUT}$ =H |
| ITH Source Current | $I_{THSO}$ | 10 | 20 | - | μA | $V_{OUT}$ =L |
| UVLO Threshold Voltage | $V_{UVLO1}$ | 2.2 | 2.3 | 2.4 | V | $V_{CC}$=H to L |
| UVLO Hysteresis Voltage | $V_{UVLO2}$ | 2.22 | 2.35 | 2.5 | V | $V_{CC}$=L to H |
| Soft Start Time | $t_{SS}$ | 0.5 | 1 | 2 | ms | |
| Timer Latch Time | $t_{LATCH}$ | 1 | 2 | 3 | ms | SCP/TSD operated |
| Output Short Circuit Threshold Voltage | $V_{SCP}$ | - | 0.4 | 0.56 | V | $V_{OUT}$ = H to L |


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## Typical Performance Curves

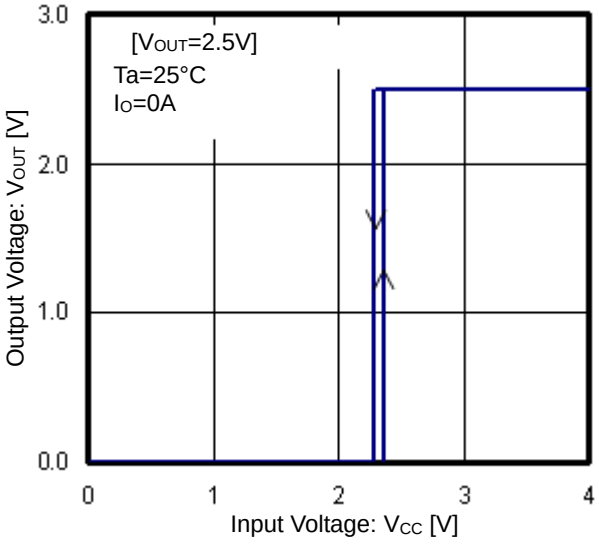



Figure 4. Output Voltage vs Input Voltage

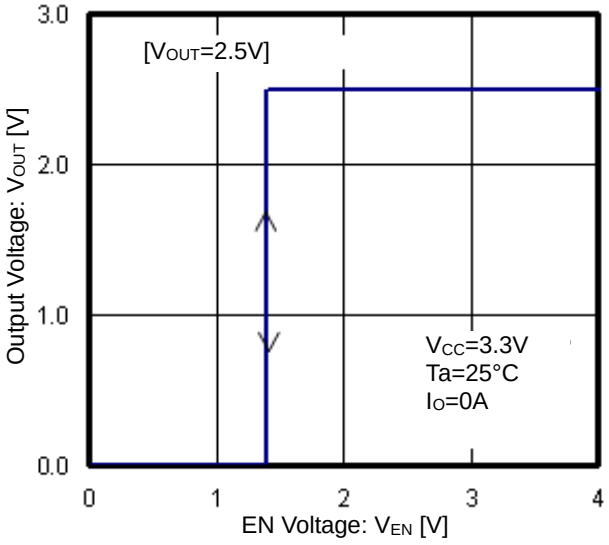



Figure 5. Output Voltage vs EN Voltage

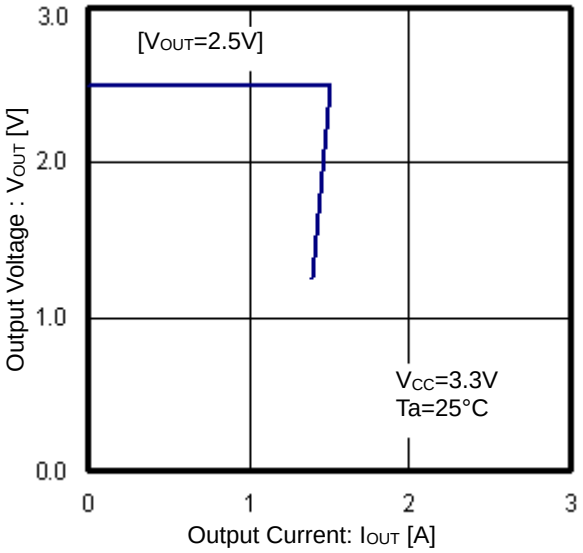



Figure 6. Output Voltage vs Output Current

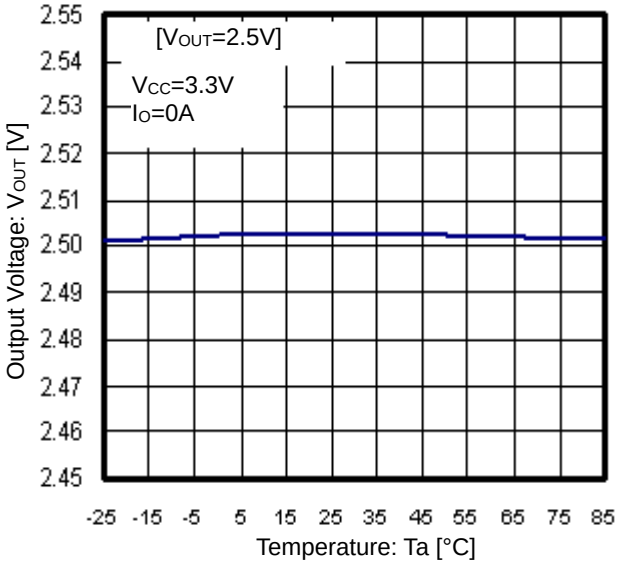



Figure 7. Output Voltage vs Temperature


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**Typical Performance Curves - continued**

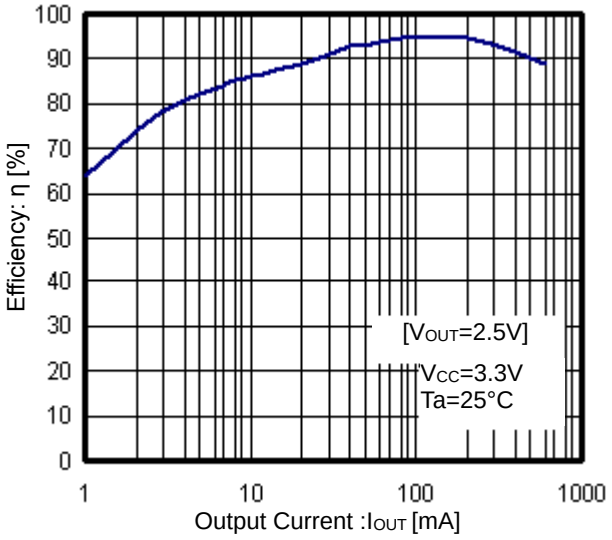



Figure 8. Efficiency vs Output Current

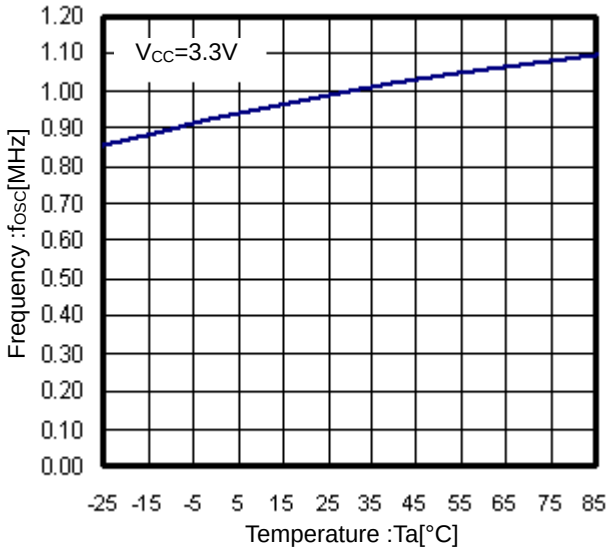



Figure 9. Frequency vs Temperature

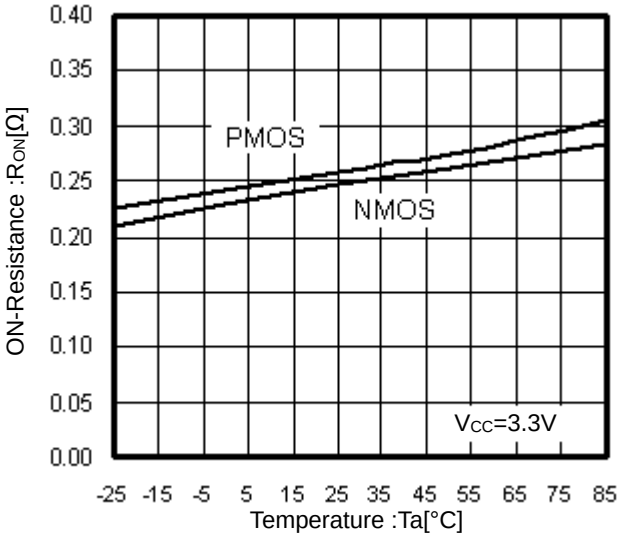



Figure 10. ON-Resistance vs Temperature

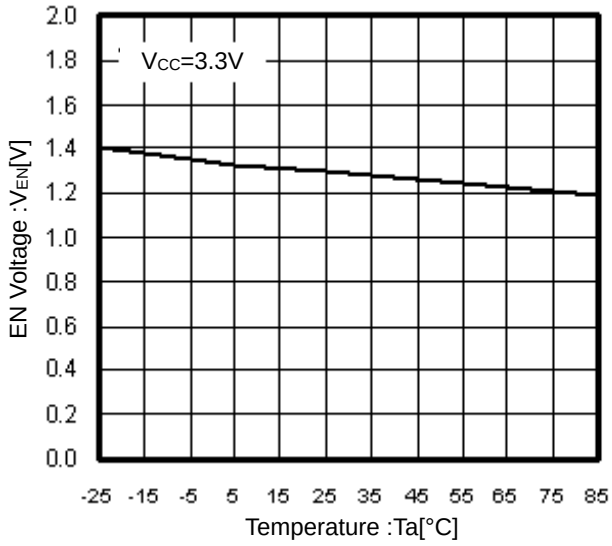



Figure 11. EN Voltage vs Temperature


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## Typical Performance Curves - continued

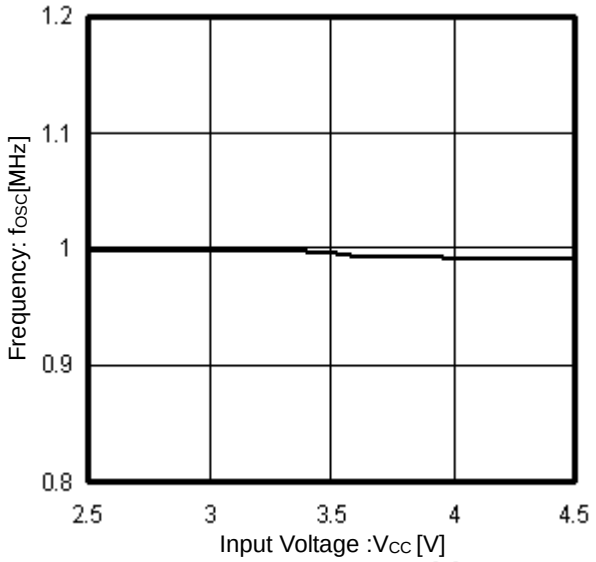



Figure 12. Frequency vs Input Voltage

## Typical Waveforms

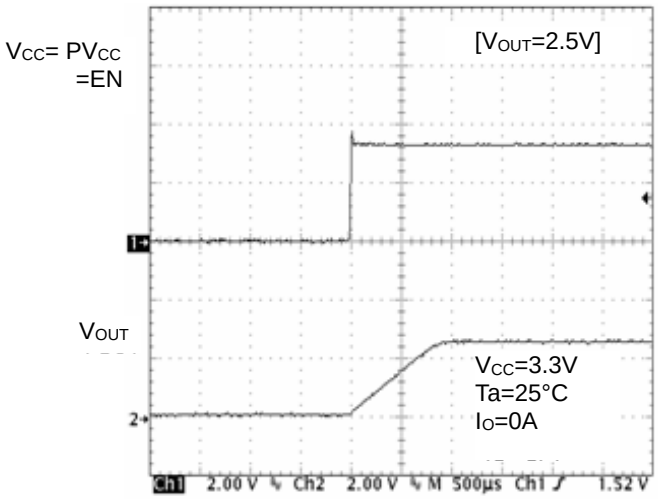



Figure 13. Soft Start Waveform

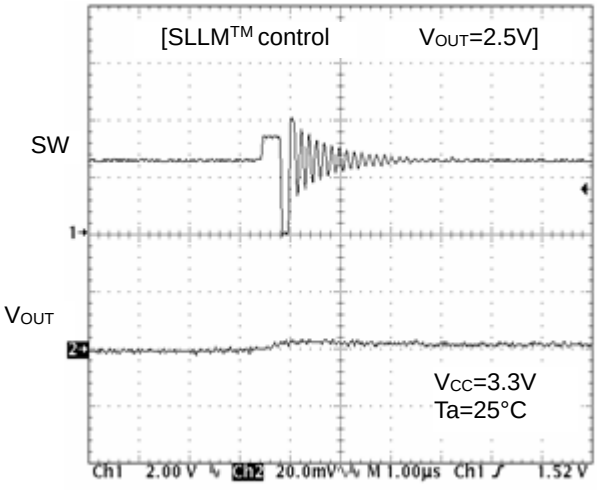



Figure 14. SW Waveform
($I_O$=10mA)


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**Typical Waveforms – continued**

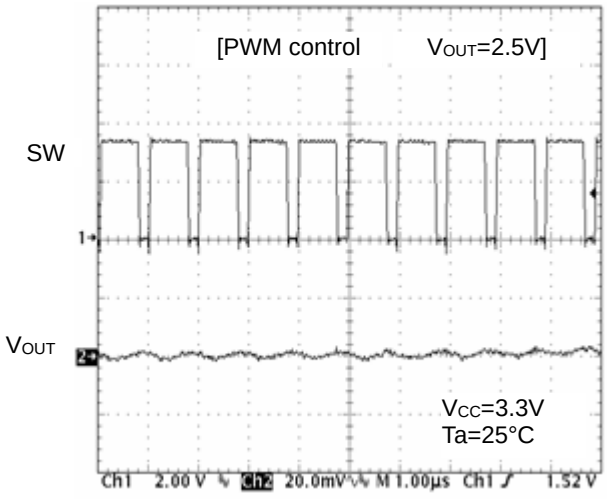



Figure 15. SW Waveform
($I_O$=500mA)

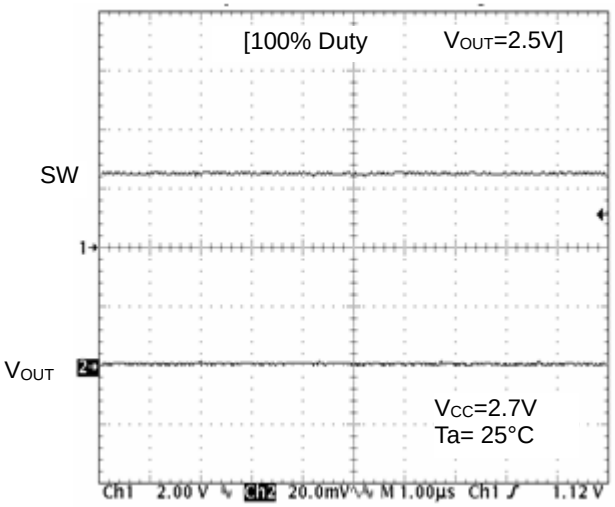



Figure 16. SW Waveform
($I_O$ =600mA)

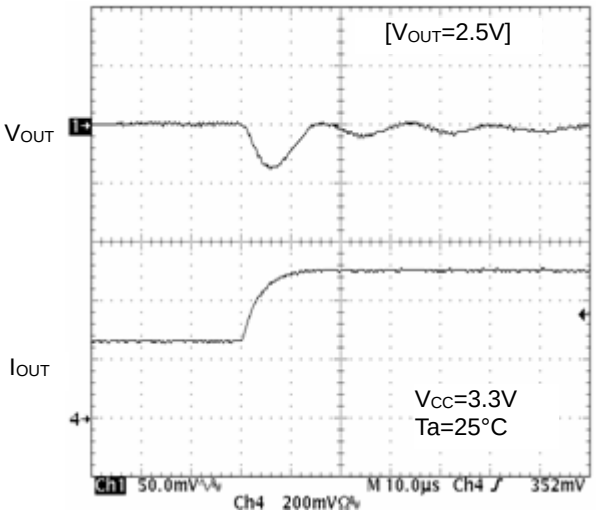



Figure 17. Transient Response
($I_O$=250mA to 500mA, 10µs)

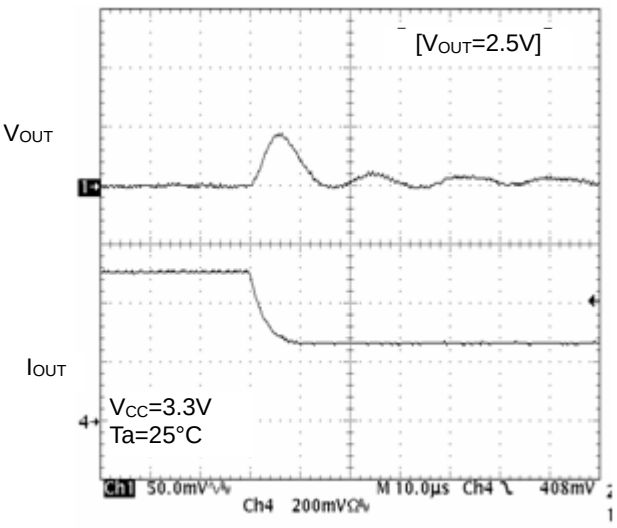



Figure 18. Transient Response
($I_O$=500mA to 250mA, 10µs)


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## Application Information

### 1. Operation

BD9161FVM is a synchronous step-down switching regulator that achieves fast transient response by employing current mode PWM control system. It utilizes switching operation through PWM (Pulse Width Modulation) mode for heavier load, and operates on SLLM™ (Simple Light Load Mode) operation for lighter load to improve efficiency.

(1) Current mode PWM Control

The PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

(a) PWM (Pulse Width Modulation) Control

The clock signal coming from OSC has a frequency of 1Mhz. When OSC sets the RS latch, the P-channel MOSFET is turned ON and the N-Channel MOSFET is turned OFF. The opposite happens when the current comparator (Current Comp) resets the RS latch. That is, i.e. the P-Channel MOSFET is turned off and the N-Channel MOSFET is turned ON. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE", which is a voltage proportional to the current sense $I_L$, and the voltage feedback control signal, FB.

(b) SLLM™ (Simple Light Load Mode) Control

When control mode is shifted due to load change, the switching pulse is designed to turn OFF with the device held in normal PWM control loop. This allows linear operation without voltage drop or deterioration in transient response during sudden load changes.

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is designed such that the RESET signal is kept constant when shifted to light load mode where the switching is turned OFF and the switching pulses disappear. Activating the switching occasionally reduces the switching dissipation and improves efficiency.

(c) 100% Duty Control

During PWM control, when output voltage becomes unstable, oscillation frequency decreases up to a point where duty cycle is 100%.

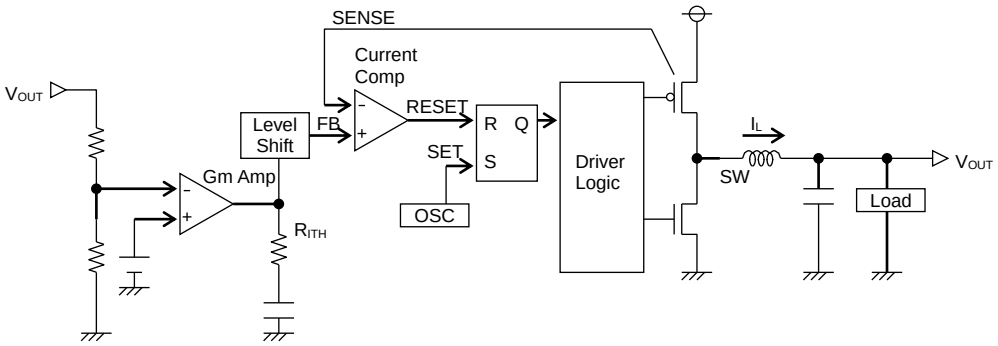



Figure 19. Diagram of Current Mode PWM Control

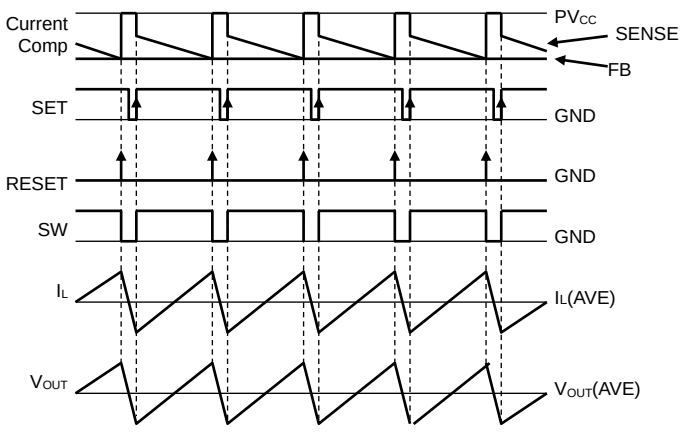



Figure 20. PWM Switching Timing Chart

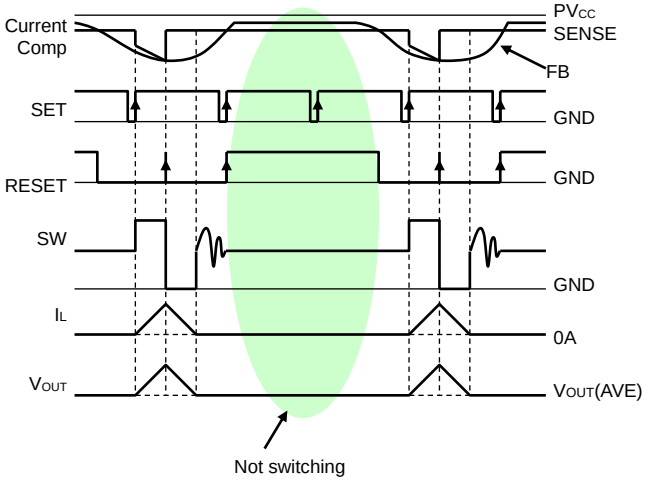



Figure 21. SLLM™ Switching Timing Chart


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## 2. Description of Functions

(1) Soft-Start Function
During start-up, the soft-start circuit gradually establishes the output voltage to limit the input current. This prevents the overshoot in the output voltage and inrush current.

(2) Shutdown Function
When the EN terminal is “Low”, the device operates in Standby Mode and all function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0μA (Typ).

(3) UVLO Function
The UVLO circuit detects whether the supplied input voltage is sufficient to obtain the output voltage of this IC. The UVLO threshold, which has a hysteresis of 50 mV (Typ), prevents output bouncing.

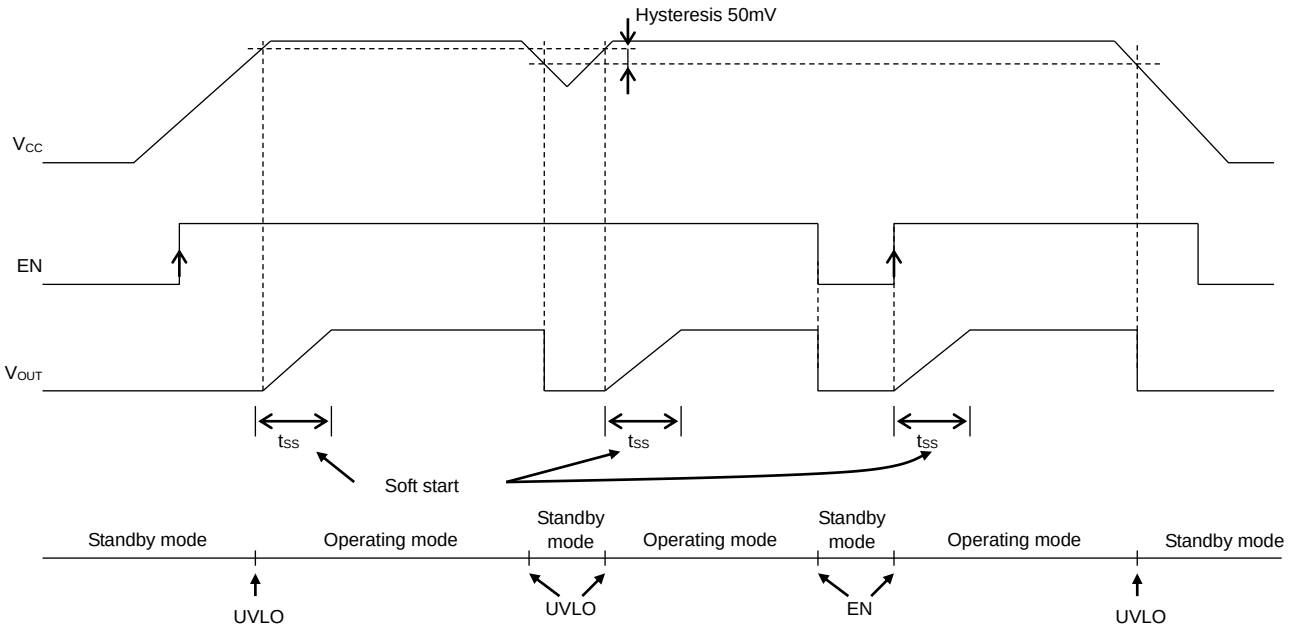



Figure 22. Soft Start, Shutdown, UVLO Timing Chart

(4) Short-Circuit Protection Circuit with Time Delay Function
To protect the IC from breakdown, the short-circuit protection circuit turns the output OFF when the internal current limiter is activated continuously for a fixed time ($t_{LATCH}$) or more. The output that is kept off may be turned ON again by restarting EN or by re-setting UVLO.

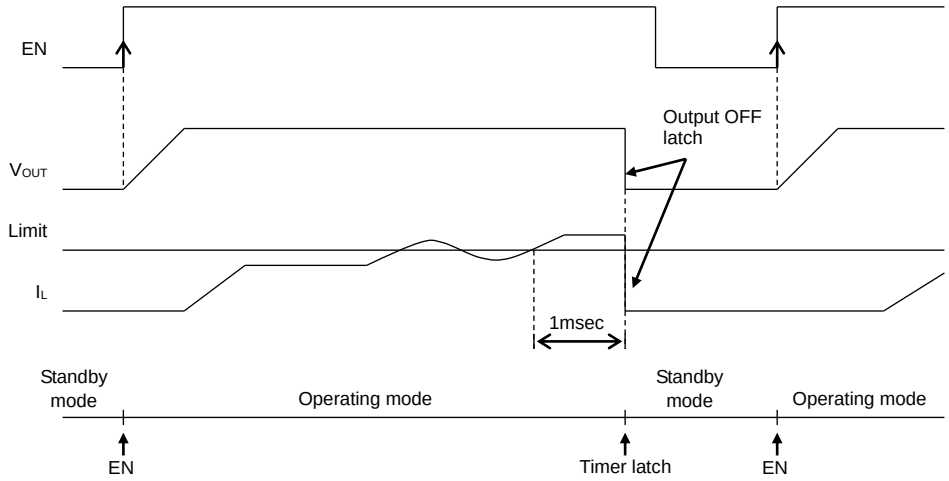



Figure 23. Short-Current Protection Circuit with Time Delay Timing Chart

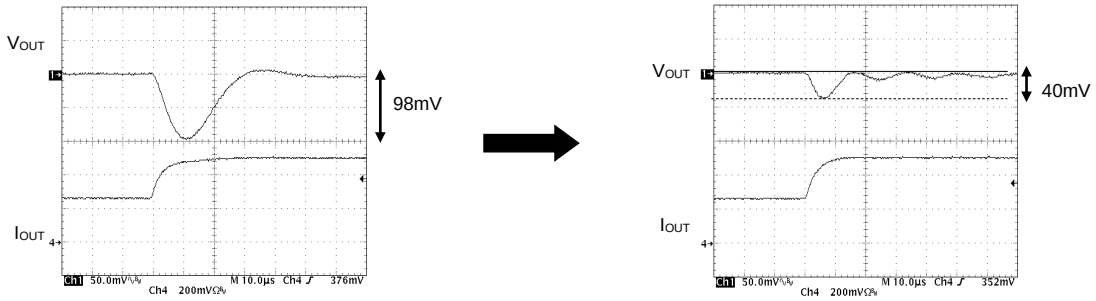

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### 3. Information on Advantages

Advantage 1 : Offers fast transient response by using current mode control system.

Conventional product ($V_{OUT}$ of which is 2.5V) BD9161FVM (Load response $I_O$=250mA to 500mA)




Voltage drop due to sudden change in load was reduced by about 50%.

Figure 24. Comparison of Transient Response

Advantage 2 : Offers high efficiency for all load range.

(a) For lighter load:
This IC utilizes the current controlled system called SLLM™, which reduces various dissipation such as switching dissipation ($P_{SW}$), gate charge/discharge dissipation, ESR dissipation of output capacitor ($P_{ESR}$) and ON-Resistance dissipation ($P_{RON}$) that may otherwise cause reduction in efficiency.

↓

Achieves efficiency improvement for lighter load.

(b) For heavier load:
This IC utilizes the synchronous rectifying mode and uses low ON-Resistance MOS-FET power transistor.

{ ON-Resistance of P-Channel MOS FET: 0.35 Ω (Typ)
ON-Resistance of N-Channel MOS FET: 0.37 Ω (Typ)

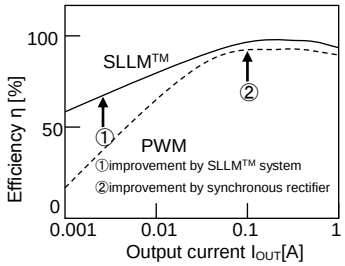



Figure 25. Efficiency

↓

Achieves efficiency improvement for heavier load.

Offers high efficiency for all load ranges with the improvements mentioned above.

Advantage 3: ・Supplied in smaller package due to small-sized power MOS-FETs.
・Allows reduction in size of application products

↓

Reduces mounting area required.

・Output capacitor Co required for current mode control: 10 µF ceramic capacitor
・Inductance L required for the operating frequency of 1 MHz: 4.7 µH inductor

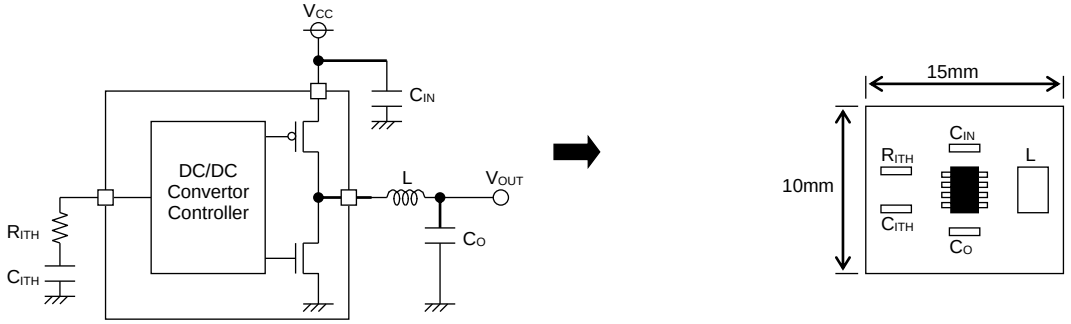



Figure 26. Example Application


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**4. Switching Regulator Efficiency**

Efficiency ŋ may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{P_{OUT}}{P_{OUT} + Pd\alpha} \times 100 \quad [\%$$

Efficiency may be improved by reducing the switching regulator power dissipation factors Pdα as follows:

Dissipation factors:

(1) ON-Resistance Dissipation of Inductor and FET：Pd($I^2R$)

$$Pd(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$$

where:
$R_{COIL}$ is the DC resistance of inductor.
$R_{ON}$ is the ON-Resistance of FET.
$I_{OUT}$ is the Output current.

(2) Gate Charge/Discharge Dissipation：Pd(Gate)

$$Pd(Gate) = C_{gs} \times f \times V^2$$

where:
$C_{gs}$ is the Gate capacitance of FET.
$f$ is the Switching frequency.
$V$ is the Gate driving voltage of FET.

(3) Switching Dissipation：Pd(SW)

$$Pd(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

where:
$C_{RSS}$ is the Reverse transfer capacitance of FET.
$I_{DRIVE}$ is the Peak current of gate.

(4) ESR Dissipation of Capacitor：Pd(ESR)

$$Pd(ESR) = {I_{RMS}}^2 \times ESR$$

where:
$I_{RMS}$ is the Ripple current of capacitor.
$ESR$ is the Equivalent series resistance.

(5) Operating Current Dissipation of IC：Pd(IC)

$$Pd(IC) = V_{IN} \times I_{CC}$$

where:
$I_{CC}$ is the Circuit current.


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**5. Consideration on Permissible Dissipation and Heat Generation**

Since this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON-Resistance of FET are considered. This is because conduction losses are the most significant among other dissipations mentioned above, such as gate charge/discharge dissipation and switching dissipation.

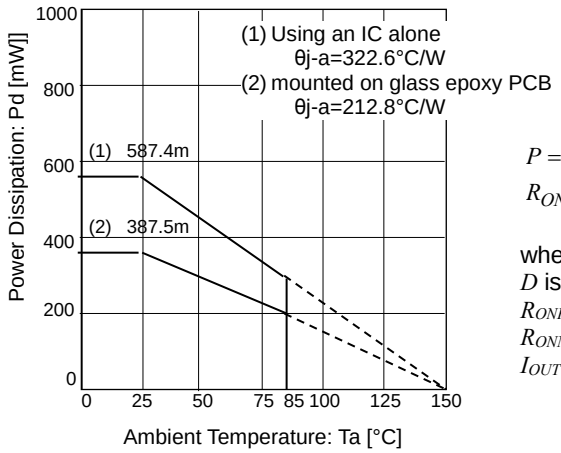



Figure 27. Thermal Derating Curve (MSOP8)

$$P = I_{OUT}{}^2 \times (R_{ON})$$
$$R_{ON} = D \times R_{ONP} + (1 - D) \times R_{ONN}$$

where:
$D$ is theON duty (=$V_{OUT}$/$V_{CC}$).
$R_{ONP}$ is the ON-Resistance of P-Channel MOS FET.
$R_{ONN}$ is the ON-Resistance of N-Channel MOS FET.
$I_{OUT}$ is the Output current.

If $V_{CC}$=3.3V, $V_{OUT}$=2.5V $R_{ONP}$ =0.35Ω, $R_{ONN}$ =0.37Ω
$I_{OUT}$=0.6A, for example,

$$D = V_{OUT} / V_{CC} = 2.5 / 3.3 = 0.758$$
$$R_{ON} = 0.758 \times 0.35 + (1 - 0.758) \times 0.758$$
$$= 0.2653 + 0.08954$$
$$= 0.35484 \quad [\Omega]$$

$$P = 0.6^2 \times 0.35484$$
$$\approx 127.7 \quad [mV]$$

Since $R_{ONP}$ is greater than $R_{ONN}$ in this IC, the dissipation increases as the ON duty becomes greater. Taking into consideration the dissipation shown above, thermal design must be carried out with allowable sufficient margin.


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## 6. Selection of Components Externally Connected

(1) Selection of Inductor (L)

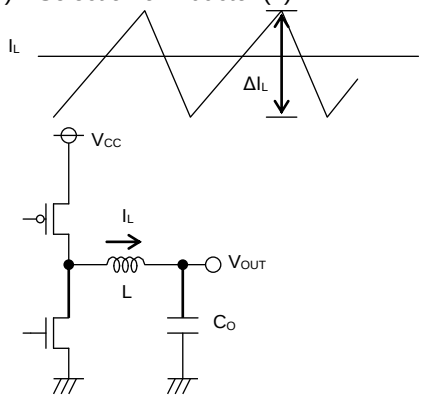



Figure 28. Output Ripple Current

The inductance significantly depends on output ripple current. As shown in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \quad [A] \cdots (1)$$

Appropriate ripple current at output should be +/-20% to +/-30% of the maximum output current.

$$\Delta I_L = 0.25 \times I_{OUTMax} \quad [A] \cdots (2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \quad [H] \cdots (3)$$

where:
$\Delta I_L$ is the Output ripple current.
$f$ is the Switching frequency.

Note: Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If $V_{CC}$=3.3V, $V_{OUT}$=2.5V, f=1MHz, $\Delta I_L$=0.25x0.6A=0.15A

$$L \geq \frac{(3.3 - 2.5) \times 2.5}{0.15 \times 3.3 \times 1M} \geq 4.04\mu$$

Note: Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

(2) Selection of Output Capacitor ($C_O$)

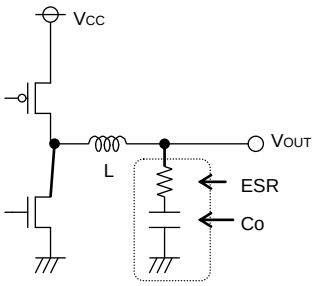



Figure 29. Output Capacitor

Output capacitor should be selected with the consideration of the stability region and the equivalent series resistance required to minimize ripple voltage.
Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \cdots (4)$$

where:
$\Delta I_L$ is the Output ripple current.
$ESR$ is the Equivalent series resistance of output capacitor.

Note: Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 10μF to 100μF ceramic capacitor is recommended. Less ESR allows reduction in output ripple voltage.

(3) Selection of Input Capacitor ($C_{IN}$)

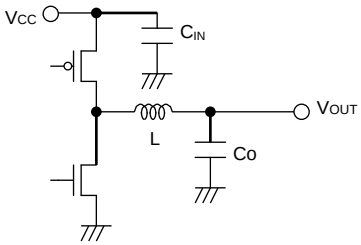



Figure 30. Input Capacitor

Input capacitor selected must be a low ESR capacitor with a capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current $I_{RMS}$ is given by the equation (5):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \quad [A] \cdots (5)$$

< Worst case > $I_{RMSMax}$

When $V_{CC}$ is twice the $V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

If $V_{CC}$=3.3V, $V_{OUT}$=2.5V, and $I_{OUTMax}$=0.6A

$$I_{RMS} = 0.6 \times \frac{\sqrt{2.5(3.3 - 2.5)}}{3.3} = 0.257 \quad [A_{RMS}]$$

A low ESR 10μF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.


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(4) Calculating $R_{ITH}$, $C_{ITH}$ for Phase Compensator

As the Current Mode Control is designed to limit the inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of an output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

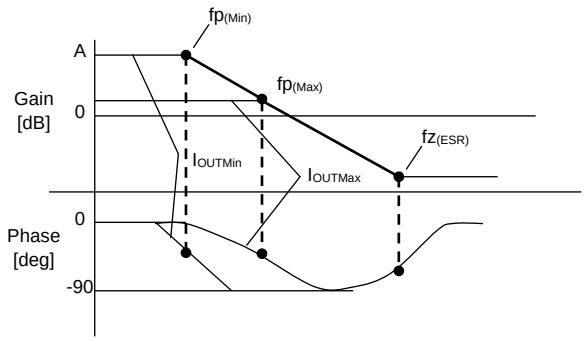



Figure 31. Open loop gain characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$fz(ESR) = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency decreases.

$$fp_{(Min)} = \frac{1}{2\pi \times R_{OMax} \times C_O}$$ [Hz] ←with lighter load

$$fp_{(Max)} = \frac{1}{2\pi \times R_{OMin} \times C_O}$$ [Hz] ←with heavier load

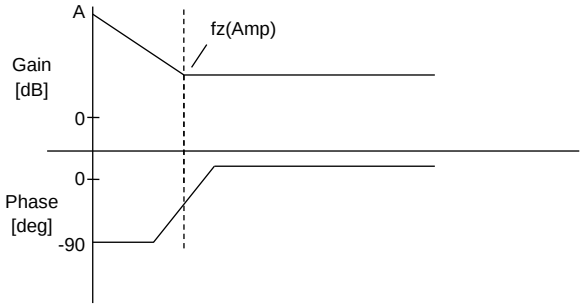



Figure 32. Error amp phase compensation characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$f_{Z(Amp)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

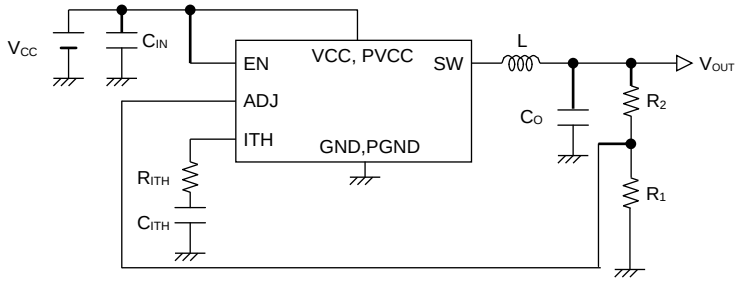



Figure 33. Typical Application

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz_{(Amp)} = fp_{(Min)}$$

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax} \times C_O}$$


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(5) Setting the Output Voltage

The output voltage $V_{OUT}$ is determined by the equation (6):

$$V_{OUT} = (R_2 / R_1 + 1) \times V_{ADJ} \quad \cdot \cdot \cdot (6)$$

Where:

$V_{ADJ}$ is the Voltage at ADJ terminal (0.8V Typ)

The required output voltage may be determined by adjusting $R_1$ and $R_2$.
(Adjustable output voltage range : 1.0V to 3.3V )

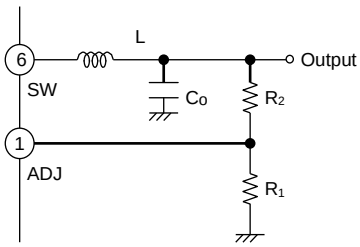



Figure 34. Determination of Output Voltage

Use 1 kΩ to 100 kΩ resistor for $R_1$. If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

## 7. BD9161FVM Cautions on PC Board Layout

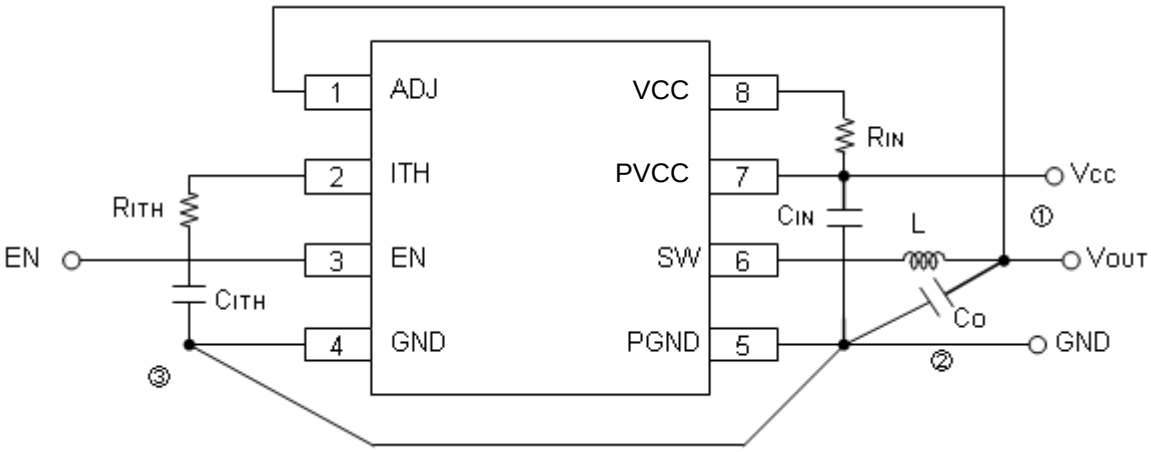



Figure 35. Board Layout

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.

② Lay out the input ceramic capacitor $C_{IN}$ closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.

③ Lay out $C_{ITH}$ and $R_{ITH}$ between the pins ITH and GND as neat as possible with least necessary wiring.

## 8. Recommended Component Lists On Above Applications

| Symbol | Part | Value | | Manufacturer | Series |
|---|---|---|---|---|---|
| L | Coil | 4.7μH | | TDK | VLF5014AT-4R7M1R1 |
| | | | | Sumida | CMD6D11B |
| $R_{IN}$ | Resistance | 10Ω | | Rohm | MCR03 Series |
| $C_{IN}$ | Ceramic Capacitor | 10μF | | Kyocera | CM316X5R106K10A |
| Co | Ceramic Capacitor | 10μF | | Kyocera | CM316X5R106K10A |
| $C_{ITH}$ | Ceramic Capacitor | $V_{OUT}$=1.0V | 820pF | Murata | GRM18 Series |
| | | $V_{OUT}$=1.2V | 560pF | Murata | GRM18 Series |
| | | $V_{OUT}$=1.5V | 470pF | Murata | GRM18 Series |
| | | $V_{OUT}$=1.8V | 470pF | Murata | GRM18 Series |
| | | $V_{OUT}$=2.5V | 330pF | Murata | GRM18 Series |
| $R_{ITH}$ | Resistance | $V_{OUT}$=1.0V | 6.8kΩ | Rohm | MCR03 Series |
| | | $V_{OUT}$=1.2V | 8.2Ω | Rohm | MCR03 Series |
| | | $V_{OUT}$=1.5V | 12kΩ | Rohm | MCR03 Series |
| | | $V_{OUT}$=1.8V | 12kΩ | Rohm | MCR03 Series |
| | | $V_{OUT}$=2.5V | 15kΩ | Rohm | MCR03 Series |

Note: The parts list presented above is an example of recommended parts. Although the parts are standard, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins


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## I/O Equivalent Circuit

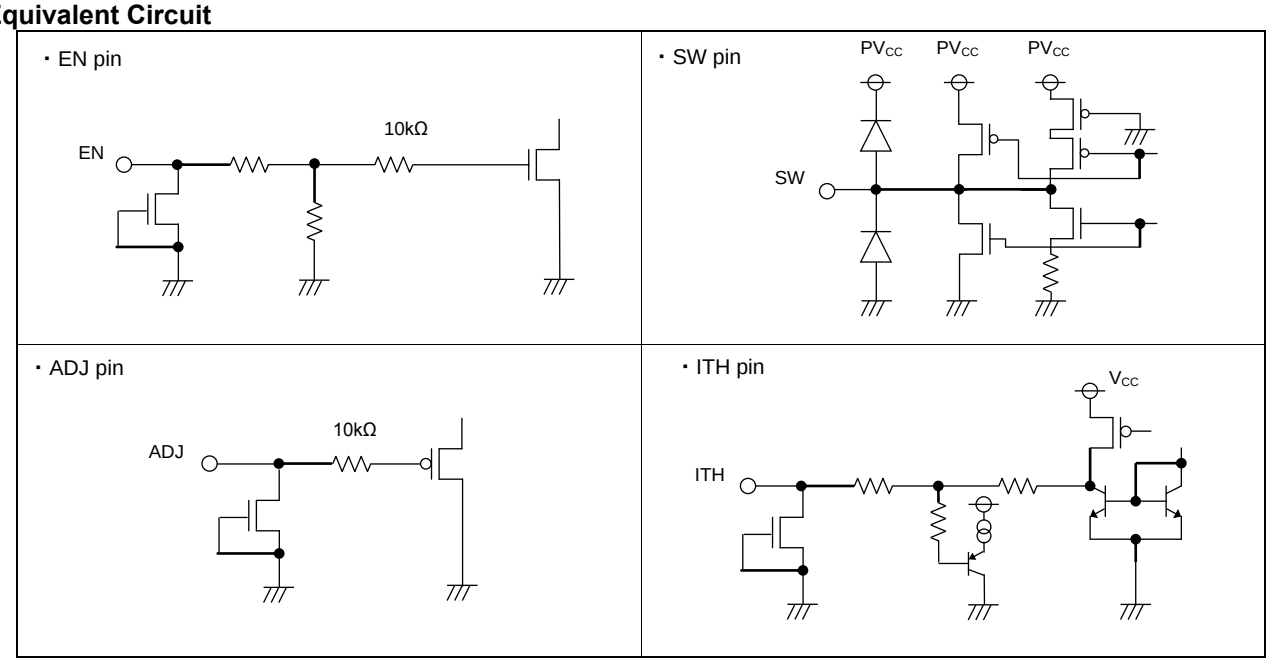



Figure 36. I/O Equivalent Circuit


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## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.


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## Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

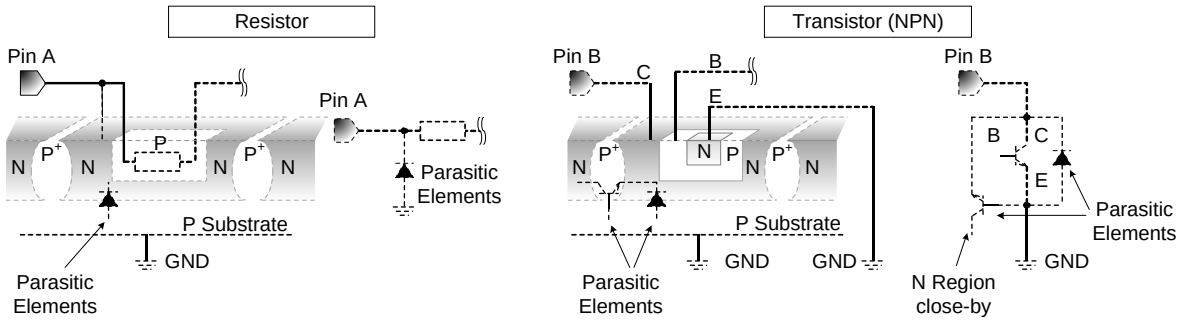



Figure 37. Example of monolithic IC structure

13. **Thermal Shutdown Circuit(TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

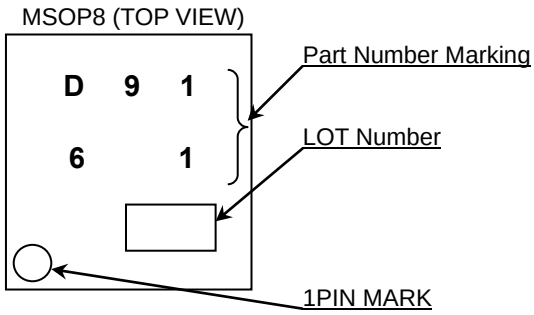

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### Ordering Information

| B D 9 1 6 1 F V M | - | T R |
|---|---|---|
| Part Number | Package<br>FVM: MSOP8 | Packaging and forming specification<br>TR: Embossed tape and reel |

### Marking Diagram



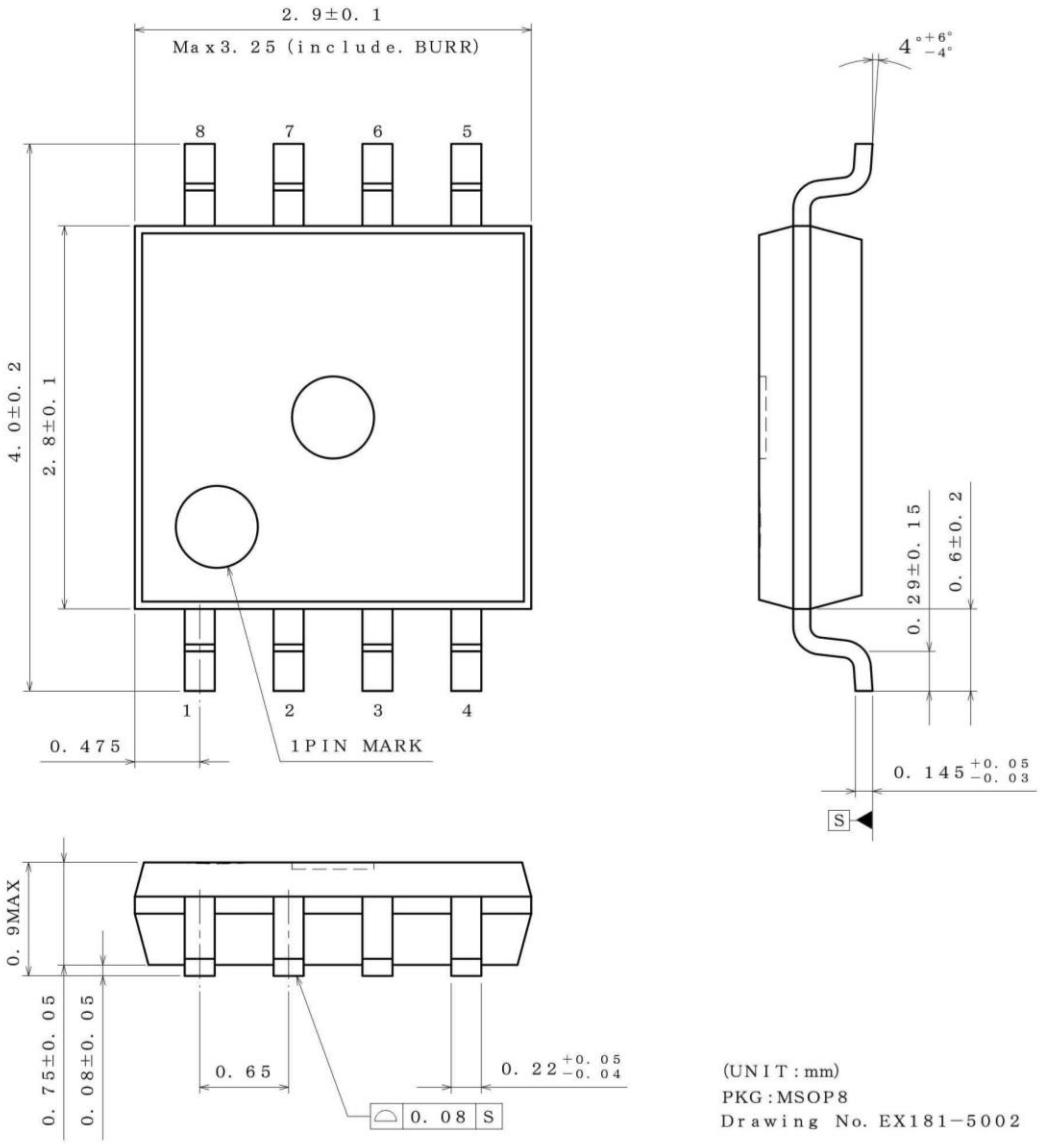


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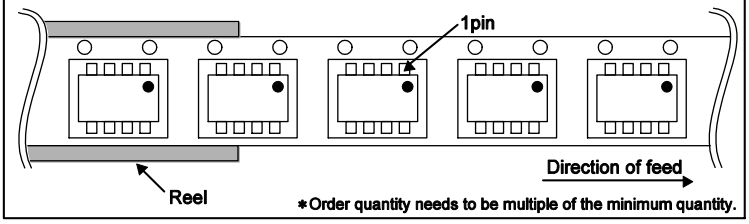
**Physical Dimension, Tape and Reel information**

| Package Name | MSOP8 |
|---|---|




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




*Order quantity needs to be multiple of the minimum quantity.


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## Revision History

| Date | Revision | Changes |
|---|---|---|
| 02.Mar.2012 | 001 | New Release |
| 06.Oct.2014 | 002 | Applied the ROHM Standard Style and improved understandability. |


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|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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   [h] Use of the Products in places subject to dew condensation

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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

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8. Confirm that operation temperature is within the specified range described in the product specification.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

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