



High-Speed Quad Monolithic SPST CMOS Analog Switch

FEATURES

- Fast Switching t_{ON} : 55 ns
- Low Charge Injection: 5 pC
- Low $r_{DS(on)}$: 32 Ω
- TTL/CMOS Compatible
- Low Leakage: 50 pA

BENEFITS

- Fast Settling Times
- Reduced Switching Glitches
- High Precision

APPLICATIONS

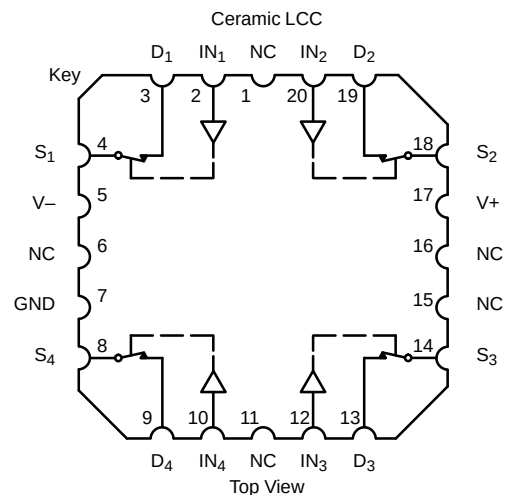
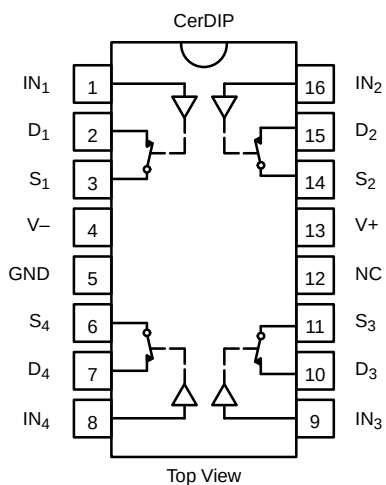
- High-Speed Switching
- Sample/Hold
- Digital Filters
- Op Amp Gain Switching
- Flight Control Systems
- Automatic Test Equipment
- Choppers
- Communication Systems

DESCRIPTION

The DG271 high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

The military version of the DG271 is manufactured using the Vishay Siliconix high voltage metal gate wafer fabrication process. The military version of the DG271 shares the same performance of the commercial DG271B, which uses the high voltage silicon gate process.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-55 to 125°C	16-Pin CerDIP	DG271AK
		DG271AK/883
		5962-8671602MEA
	LCC-20	DG271AZ/883
		5962-8671602M2A

ABSOLUTE MAXIMUM RATINGS

V+ to V-	44 V
GND to V-	25 V
Digital Inputs ^a V _S , V _D	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current, Any Terminal	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (AK and AZ Suffix)	-65 to 150°C

Power Dissipation (Package) ^b	
16-Pin CerDIP ^c	900 mW
LCC-20 ^d	750 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 12 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

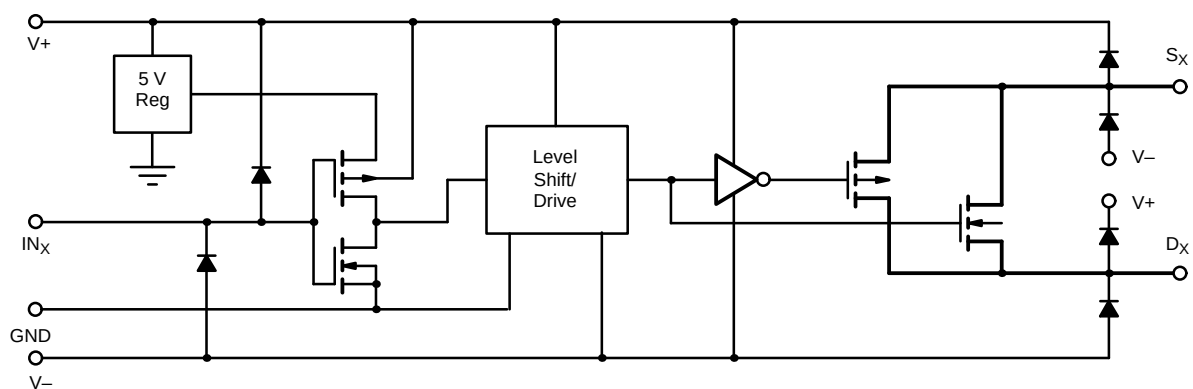


FIGURE 1.



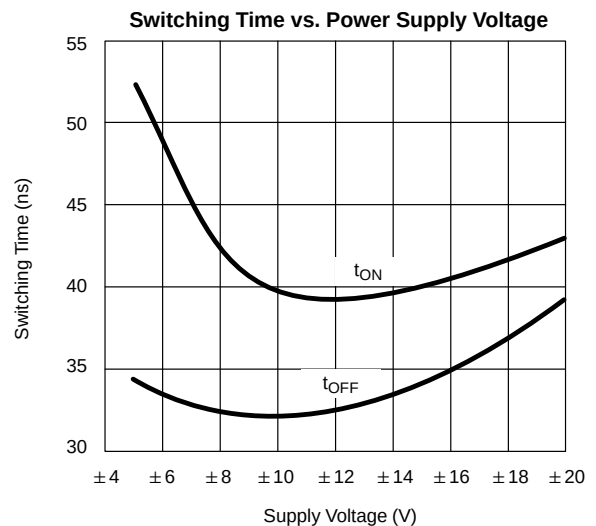
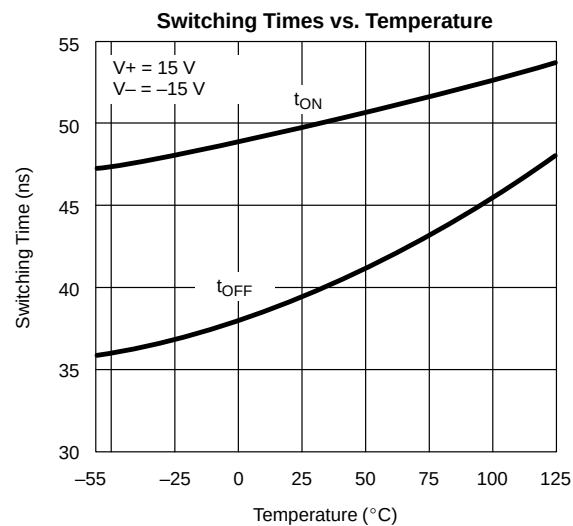
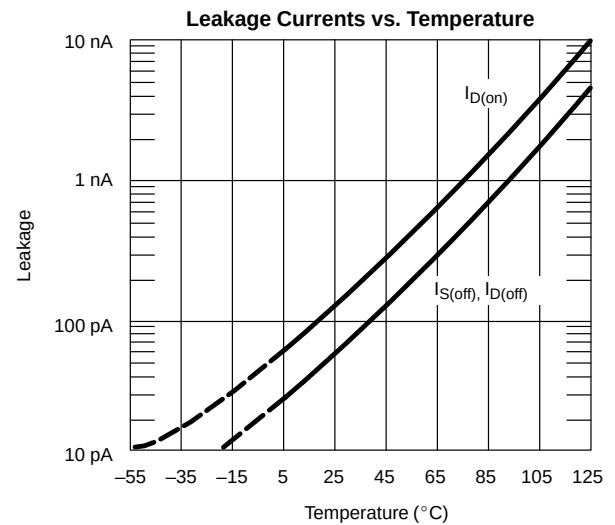
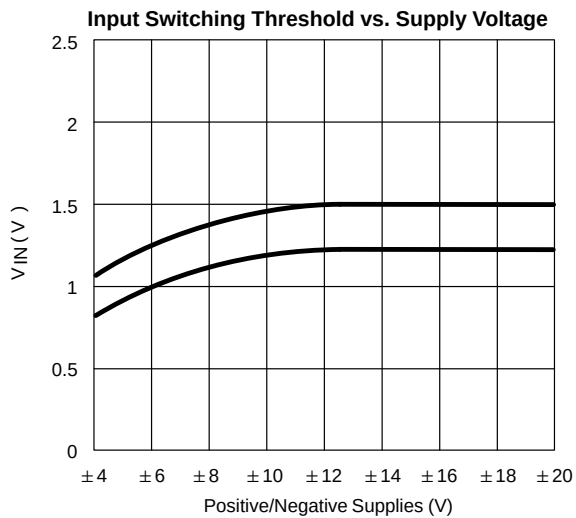
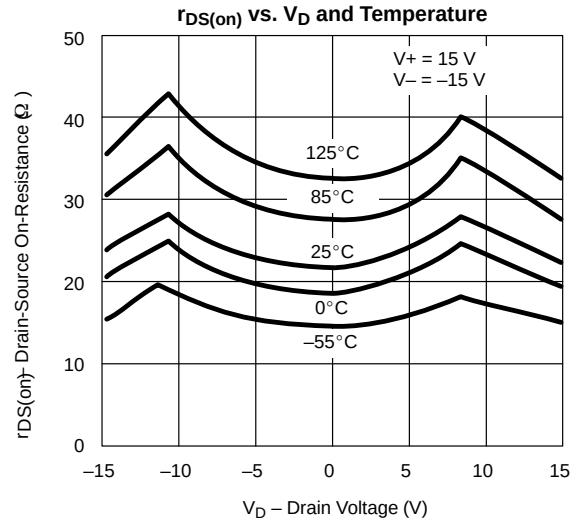
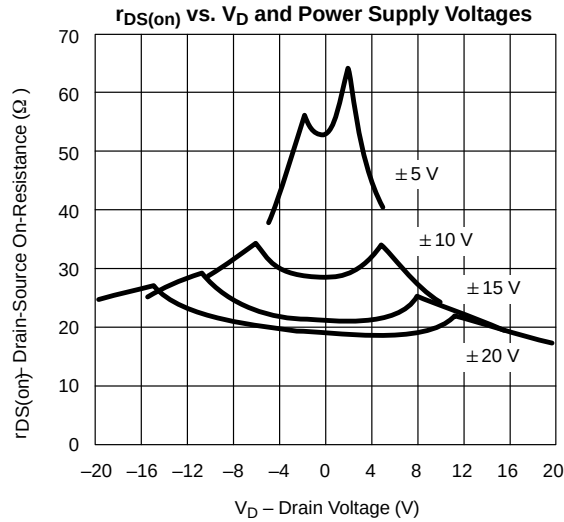
SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Specified V ⁺ = 15 V, V [–] = –15 V V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	A Suffix –55 to 125°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V _{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	r _{DS(on)}	I _S = 1 mA, V _D = ±10 V	Room Full		32	50 75	Ω
Switch Off Leakage Current	I _{S(off)}	V _D = ±14 V, V _S = ∓14 V	Room Full	–1 –60	±0.05	1 60	nA
	I _{D(off)}		Room Full	–1 –60	±0.05	1 60	
Channel On Leakage Current	I _{D(on)} + I _{S(on)}	V _S = V _D = ±14 V	Room Full	–1 –60	±0.05	1 60	
Digital Control							
Input Current with Voltage High	I _{INH}	V _{IN} = 2 V	Full	–1	0.010	1	μA
		V _{IN} = 15 V	Full	–1	0.010	1	
Input Current with Voltage Low	I _{INL}	V _{IN} = 0 V	Full	–1	0.010	1	
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _S = ±10 V See Figure 3	Room Full		55	65 80	ns
Turn-Off Time	t _{OFF}		Room Full		50	65 80	
Charge Injection	Q	C _L = 1 nF, V _S = 0 V V _{gen} = 0 V, R _{gen} = 0 Ω See Figure 3	Room		–5		pC
Source Off Capacitance	C _{S(off)}	V _S = 0 V, V _{IN} = 5 V f = 1 MHz	Room		8		pF
Drain Off Capacitance	C _{D(off)}		Room		8		
Channel On Capacitance	C _{D(on)}	V _D = V _S = 0 V, V _{IN} = 0 V	Room		30		
Off Isolation	OIRR	C _L = 10 pF, R _L = 1 kΩ f = 100 kHz See Figures 4 and 5	Room		85		dB
Crosstalk	X _{TALK}		Room		100		
Supply							
Positive Supply Current	I ⁺	All Channels On or Off V _{IN} = 5 V or 0 V	Room Full		5.5	7.5 9	mA
Negative Supply Current	I [–]		Room Full	–6 –8	–3.4		

Notes:

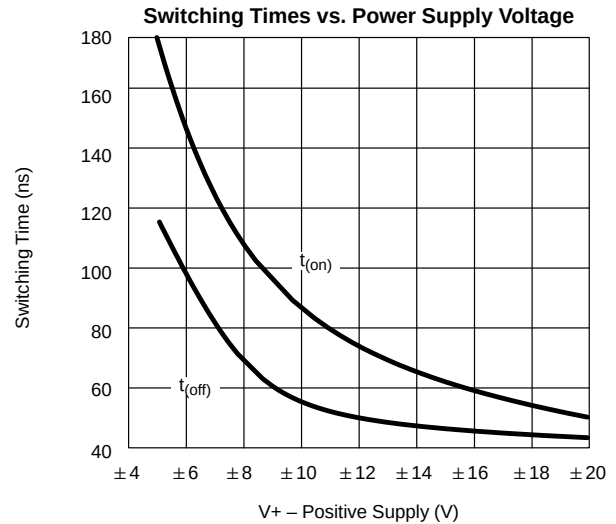
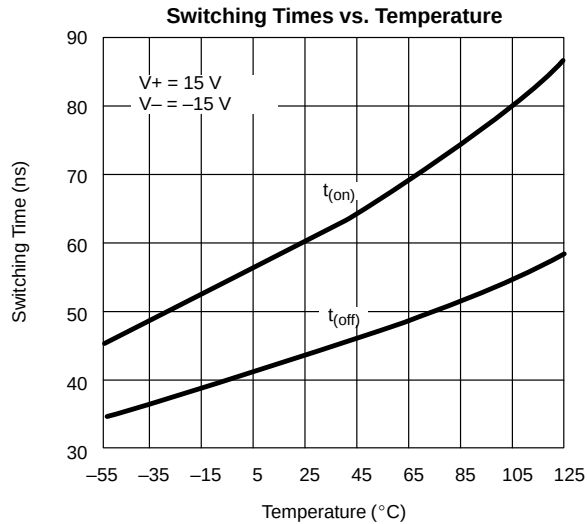
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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TEST CIRCUITS

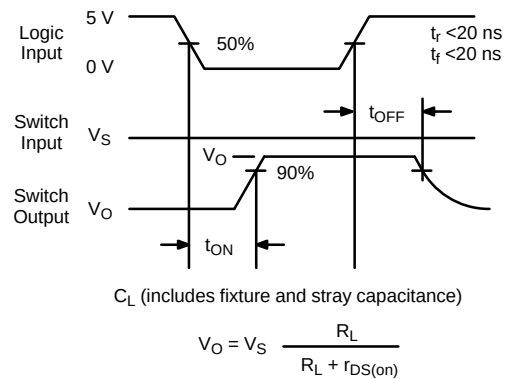
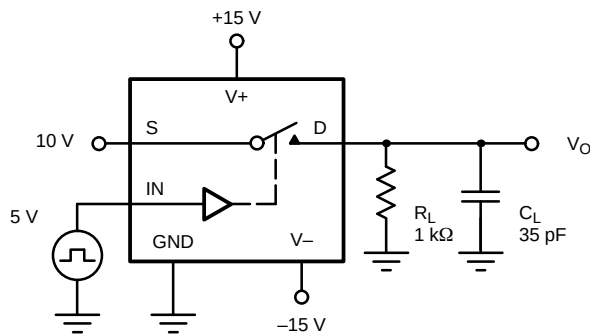


FIGURE 2. Switching Time