REV	DESCRIPTION	DATE	PREP	APPD
I	EC20247	4/21/23	SM	LT/AJ

MICROCHIP

Vectron Oscillators

MOUNT HOLLY SPRINGS, PA 17065

Oscillator Specification, Hybrid Clock

For

Hi-Rel Standard, LVDS Output

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CODE IDENT NO	SIZE	DWG. NO.	REV
00136	A	DOC203679	I

UNSPECIFIED TOLERANCES: N/A

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1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid clock oscillators produced by Vectron. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented, and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC203679 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military or Ruggedized COTS environments.

2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Standards

MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Other

DOC203986	Test Specification, Hybrid Clock, Hi-Rel Standard, LVDS Output
QSP-90100	Quality Systems Manual, Vectron
DOC011627	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions
DOC208191	Enhanced Element Evaluation for Space Level Hybrid Oscillators
DOC220429	Packaging Standards, Hi-Rel Series

3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310 and have a Class 1C ESDS rating per MIL-PRF-38534. Primarily developed as a Class S equivalent specification, options are imbedded within it to also produce Class B, Engineering Model and Ruggedized COTS devices.

3.2 Item Identification. Unique Model Number Series' are utilized to identify device package configurations as listed in Table 1.

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3.3 Absolute Maximum Ratings.

a. Supply Voltage Range (V_{CC}):	-0.3Vdc to +4.0Vdc
b. Storage Temperature Range (T_{STG}):	-65°C to +125°C
c. Junction Temperature (T_J):	+150°C
d. Lead Temperature (soldering, 10 seconds):	+300°C
e. Weight	5 grams

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. Designs utilize 4-point crystal mounting in combination with Established Reliability (MIL-ER) components. When specified, radiation tolerant active devices up to 100krad(Si) (RHA level R) can be included without altering the device's internal topography.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without notification.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:
a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three-minute duration in each of three mutually perpendicular directions.)
c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.
a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.
g. 'getter' materials

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on radiation hardened part numbers to further verify lot pedigree. Devices are handled in accordance with Vectron document QSP-91502 (Procedure for Electrostatic Discharge Precautions). Element replacement will be as specified in MIL-PRF-38534, Rev L.

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3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 derived, System of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 5 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310. In addition, when devices are identified with laser marking, the Resistance to Solvents test specified in MIL-PRF-55310 Group C, Mil-PRF-55310 Qualification or MIL-PRF-38534 Group B Inspection will not be performed.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree "D" devices (see ¶ 5.2) use the same robust designs, component type and construction, found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified components noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. The optional use of Premium Q swept quartz can, because of its processing to remove impurities, be specified to minimize frequency drift when operating in radiation environments. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

4.1.2 Passive Components.

4.1.2.1 For Design Pedigree E, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Enhanced Element Evaluation of DOC208191 which meets the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.2.2 For Design Pedigrees R, V and X, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Class K Element Evaluation of Mil-PRF-38534 Revision K for Class K.

4.1.2.3 For Design Pedigrees B and C, all passive elements shall comply with the Element Evaluation requirements of Mil-PRF-55310 Class B as a minimum.

4.1.2.4 For Design Pedigree D, the passive elements will be COTs level or higher.

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4.1.2.5 When used, inductors will be open construction and may use up to 47-gauge wire.

4.1.3 Microcircuits.

4.1.3.1 The LVDS microcircuit die is sourced in accordance with Standard Microcircuit Drawing 5962R9865105V9A or 5962F9865107V9A, Class V (MIL-PRF-38535) qualified device.

4.1.3.2 For Design Pedigree D, microcircuits can be COTs level or higher.

4.1.4 Semiconductors

4.1.4.1 For Design Pedigree E, the semiconductors shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191.

4.1.4.2 For Design Pedigree R, V and X, semiconductors shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K devices as a minimum.

4.1.4.3 For Design Pedigree B, and C, semiconductors are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B devices as a minimum.

4.1.4.4 For Design Pedigree D, semiconductors can be COTs level or higher.

4.1.5 Radiation. When optionally specified, further testing is performed on the bipolar transistor for radiation hardness assurance up to 100krad (Si) total ionizing dose (TID) and for Enhanced Element Evaluation as specified in DOC208191. In addition, for frequencies greater than 50 MHz, the bi-polar transistor was tested to an LET greater than 83 MeV-cm2/mg and did not have any transients that perturbated to the differential output of the oscillator. The differential driver circuitry, after the transistor, was able to mitigate any transients generated as the transients were either too short or non-existent from the transistor. The LVDS output buffer (5962R) is rated to $1x10^{13}$ N/cm^2 Neutron Fluence, SEL immune to 100 MeV-cm^2/mg and SET to a threshold of 84.96 MeV-cm^2/mg. The LVDS output buffer (5962F) is SEL immune to 120 MeV-cm^2/mg and SET/SEU to a threshold of 67 MeV-cm^2/mg.

4.1.6 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are up screened in accordance with the requirements of MIL-PRF-38534 as applicable. Vectron will not perform Salt Spray testing as part of MIL-PRF-55310 Group C/Qualification. In accordance with MIL-PRF-55310, package evaluation results for salt atmosphere will be substituted for Salt Spray testing during MIL-PRF-55310 Group C/Qualification.

4.1.7 Traceability and Homogeneity. All design pedigrees except option D have active device lots that are traceable to the manufacturer's individual wafer; all other elements and materials are traceable to their manufacturer and incoming inspection lots. Design pedigrees E, R, V and X have homogeneous material. In addition, swept quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot. A production lot, as defined by Microchip, is all oscillators that have been kitted and built as a single group. The maximum deliverable quantity with a single lot date code is 150 units. Order quantities that exceed 150 units will be

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delivered in multiple lot date codes with deliveries separated by 3 weeks. If applicable, each production lot will be kitted with homogeneous material which is then allocated across multiple lot date code builds to satisfy the deliverable order quantity. When ordered, Group C Inspection, lot qualifications, and/or DPA will be performed on the first build lot within the production lot unless otherwise stated on the purchase order.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.

4.2.2 Thermal Characteristics. The calculated thermal resistance and resulting junction temperature rise is found in Table 4.

4.2.3 Lead Forming. When lead forming option is specified, the applicable leak test specified in screening will be performed after forming.

4.3 Electrical.

4.3.1 Input Power. Devices are designed for standard +3.3 volt dc operation, ±5%. Current is measured, no load, at maximum rated operating Voltage.

4.3.2 Temperature Range. Operating range is -55°C to +125°C.

4.3.3 Frequency Tolerance. Initial accuracy at +23°C is ±15 ppm maximum. Frequency-Temperature Stability is ±50 ppm maximum from +23°C reference. Frequency-Voltage Tolerance is ±4 ppm maximum.

4.3.4 Frequency Aging. Aging limits, and when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1.5 ppm the first 30 days, ±5 ppm Year 1 and ±2 ppm per year thereafter.

4.3.4.1 Frequency Aging Duration Option. The Aging test may be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-Day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time. Vectron's automated aging systems take about 6 data points per day, so a lot of data is available to do very accurate projections, much more data than what is required by MIL-PRF-55310. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit, then they would continue to full 30-Day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.5 Operating Characteristics. Symmetrical square wave limits are dependent on the device frequency and are in accordance with Table 2 and Figure 1. Start-up time is 10.0 msec. maximum.

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4.3.6 Output Load. See Figure 2.

4.4 Enable/Disable (E/D). E/D function shall be tested for the applicable model at nominal conditions only. Outputs are enabled when Pin 13 is left floating or 0V to 0.8V is applied. Outputs are disabled when 2.0V to Vcc is applied.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 15th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

- A Modified MIL-PRF-38534 Class K
- B Modified MIL-PRF-55310 Class B Screening & Group A Quality Conformance Inspection (QCI)
- C Modified MIL-PRF-55310 (Rev E) Class S Screening & Group A QCI
- D Modified MIL-PRF-38534 Class K with Group B Aging
- E Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
- F Modified MIL-PRF-55310 (Rev E) Class S Screening, Groups A & B QCI
- G Modified MIL-PRF-55310 Class B Screening & Post Burn-in Nominal Electricals
- S MIL-PRF-55310 (Rev F) Class S Screening & Groups A & B QCI
- X Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection, and test options that can be selected or added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):
   (E) Enhanced Element Evaluation, (MIL-PRF-38534 Rev L for Class K components as specified in DOC208191)100krad die, Premium Q Swept Quartz
   (R) Hi-Rel design w/ 100krad Class K die, Premium Q Swept Quartz
   (V) Hi-Rel design w/ 100krad Class K die, Non-Swept Quartz
   (X) Hi-Rel design w/ Non-Swept Quartz, Class K die
   (B) Hi-Rel design w/ Swept Quartz, Class B die
   (C) Hi-Rel design w/ Non-Swept Quartz, Class B die
   (D) Hi-Rel design w/ Non-Swept Quartz and commercial grade components
b. Input Voltage, (B) for +3.3V as the 14th character
c. Not Used
d. Radiographic Inspection
e. Group C Inspection: In accordance with MIL-PRF-55310, Rev E (requires 8 destruct specimens)
f. Group C Inspection: MIL-PRF-55310, Rev F (requires 8 destruct specimens, includes Random Vibration, MIL-STD-883, Method 1014 Leak Test and Life Test)

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g. Group C Inspection: In accordance with MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA) Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Test Condition C.
h. Internal Water-Vapor Content (RGA) samples and test performance
i. MTBF Reliability Calculations
j. Worst Case Analysis (unless otherwise specified, MIL-HDBK-1547)
k. Derating and Thermal Analysis (unless otherwise specified, MIL-HDBK-1547 with Tj Max = +105°C; Derated Maximum Operating Temp = Tj Max – ΔTj)
l. Process Identification Documentation (PID)
m. Customer Source Inspection (pre-crystal mount pre-cap, post-crystal mount pre-cap and final). Due to components being mounted underneath the crystal blank, pre-crystal mount pre-cap inspection should be considered.
n. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982.
o. Qualification: In accordance with MIL-PRF-55310, Rev F, Table IV (requires 16 destruct specimens). Includes Group III, SG1 through SG6 only. ESD (SG7) not performed.
p. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)
q. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum)
r. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.
s. As Designed Parts, Materials and Processes List

5.2.1 NASA EEE-INST-002. A combination of Design Pedigree R, Option S Screening, and Qualification per EEE-INST-002, Section C4, Table 3, meet the requirements of Level 1 and Level 2 device reliability.

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions, and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.3.1 When MIL-PRF-55310, Revision F was being reviewed for release by manufacturers and users, Vectron and other organizations recommended that burn-in delta limits not be applied to logic level measurements due to the inconsistency in attempting to measure small changes in logic levels which inherently have ringing in the signal. This is especially true in higher frequency oscillators measured in automated test systems that are affected by cable length that is not representative of the user's application and contact resistance in test fixtures that do not provide a consistent Vcc or Ground connection. The exact test setup conditions may vary slightly from pre-burn-in to post-burn-in and cause small artificial deltas in logic level measurements that are not indicative of an issue. Any significant changes in logic levels will be reflected in supply current deltas and/or logic levels that exceed the min/max limits. As a result, we take exception to MIL-PRF-55310, Revision F, Para. 4.4.5 and the delta limit for Output Low Level as specified in 4.4.5(c) shall not be applied to Burn-in PDA.

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5.4 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices (except devices with Screening Option X):

a. Completed assembly and screening lot travelers and screening data, including radiographic images, rework history and Certificate of Conformance.
b. Electrical test variables data, identified by unique serial number.
c. Special items when required by purchase order such as Group C, DPA, and RGA data.
d. Traceability, component LAT, enclosure LAT, and wafer lot specific RLAT data for non-SMD active devices (if applicable and available).

5.5 Discrepant Material. All MRB authority resides with the procuring activity.

5.6 Failure Analysis. Any failure during Qualification or Group C Inspection will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with MIL-STD-1686 for Class 1 devices. Devices will be packaged for transport in accordance with DOC220429. Please note that “one unit per package” is available for a fee; however, this service must be requested as part of the official RFQ.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 15 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

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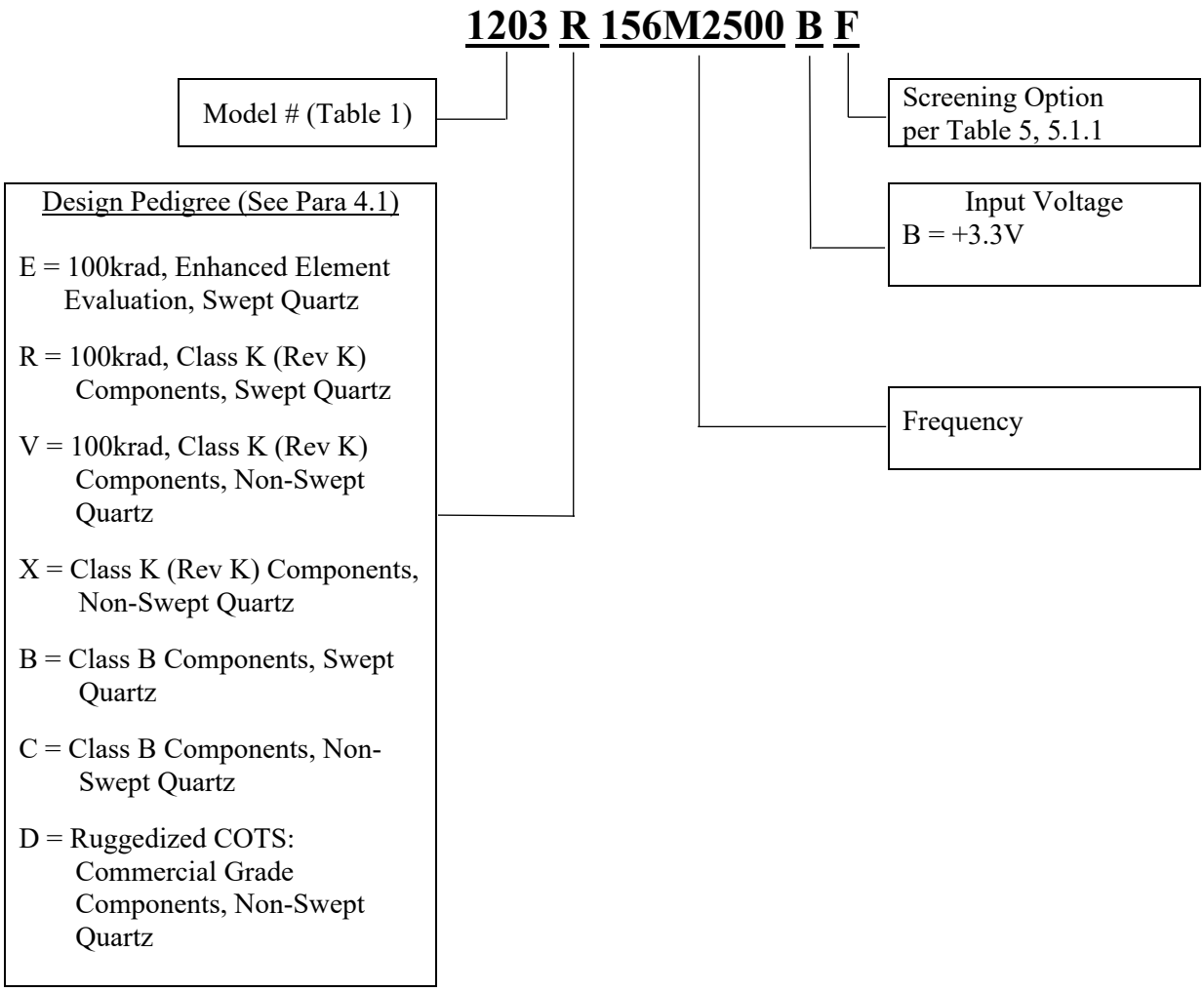
The Part Number breakdown is described as:



7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S variants correspond to either letter “E”, “R”, “V” or “X” and are described in paragraph 5.2a. Class B variants correspond to either letter “B” or “C” and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, corresponds to letter “D”.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Input Voltage. Voltage is the 14th character, letter “B” represents +3.3V.

7.1.5 Screening Options. The 15th character is the Screening Option (letter A thru G, S or X) selected from Table 5.

7.2 Optional Design, Test and Data Parameters. Optional test and documentation requirements shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru s).

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MODEL #	PACKAGE	OUTPUT (LVDS)	MECHANICAL OUTLINE AND I/O CONNECTIONS
1203	16 Lead Flatpack	Single Pair	Figure 5
1219 1/	16 Lead Flatpack	Single Pair	Figure 6
1204	20 Lead Flatpack	Single Pair	Figure 3
1220 1/	20 Lead Flatpack	Single Pair	Figure 4
1208	20 Lead Flatpack	Dual Pairs	Figure 3
1240 1/	20 Lead Flatpack	Dual Pairs	Figure 4
1216	20 Lead Flatpack	Quad Pairs	Figure 3
1280 1/	20 Lead Flatpack	Quad Pairs	Figure 4

1/. Models 1219, 1220, 1240 and 1280 are lead formed versions of Models 1203, 1204, 1208 and 1216 respectively. See Appendix A for recommended land pattern.

TABLE 1 - Item Identification and Package Outline

Frequency Range: 12MHz to 200MHz 1/					
Temperature Range: -55°C to +125°C					
Frequency Tolerance, Initial Accuracy @ +23°C: ±15 ppm max.					
Frequency-Temperature Stability from +23°C ref.: ±50 ppm max.					
Frequency-Voltage Tolerance: ±4 ppm max. (Vcc ± 5%)					
Frequency Aging: ±1.5 ppm max. 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+ (Estimated maximum aging for 20 years will be <10 ppm due to the non-linear characteristics of crystal aging)					
Start-up Time: 10.0 ms max.					
Differential Output Voltage VOD: 250mV to 450mV					
Offset Voltage VOS: 1.125V to 1.450V					
Frequency Range (MHz)	Single Pair Current 2/ (mA max)	Dual Pairs Current 2/ (mA max)	Quad Pairs Current 2/ (mA max)	Rise/Fall Times (ps max)	Duty Cycle (%)
12 – 50	15	28	35	500	40 to 60
> 50 – 100	20	30	40	500	40 to 60
> 100 – 160	25	40	45	500	40 to 60
> 160 – 200	30	45	45	500	40 to 60

1/. Waveform measurement points and logic limits are in accordance with Figure 1.
2/. Current measurements are taken with no load at maximum supply voltage.

TABLE 2 - Electrical Performance Characteristics

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Frequency Range (MHz)	Period Jitter 1 sigma (ps)	Period Jitter peak-to-peak (ps)	Phase Jitter 12kHz to 20MHz (ps)
12	3.5	30	2.652
30	3.5	30	0.752
40	3.5	30	0.448
60	3.5	30	0.269
80	3.5	30	0.212
100	2.5	22	0.200
125	2.5	22	0.145
156.25	2.5	22	0.115
200	2.5	22	0.090

TABLE 2a – Typical Jitter Performance

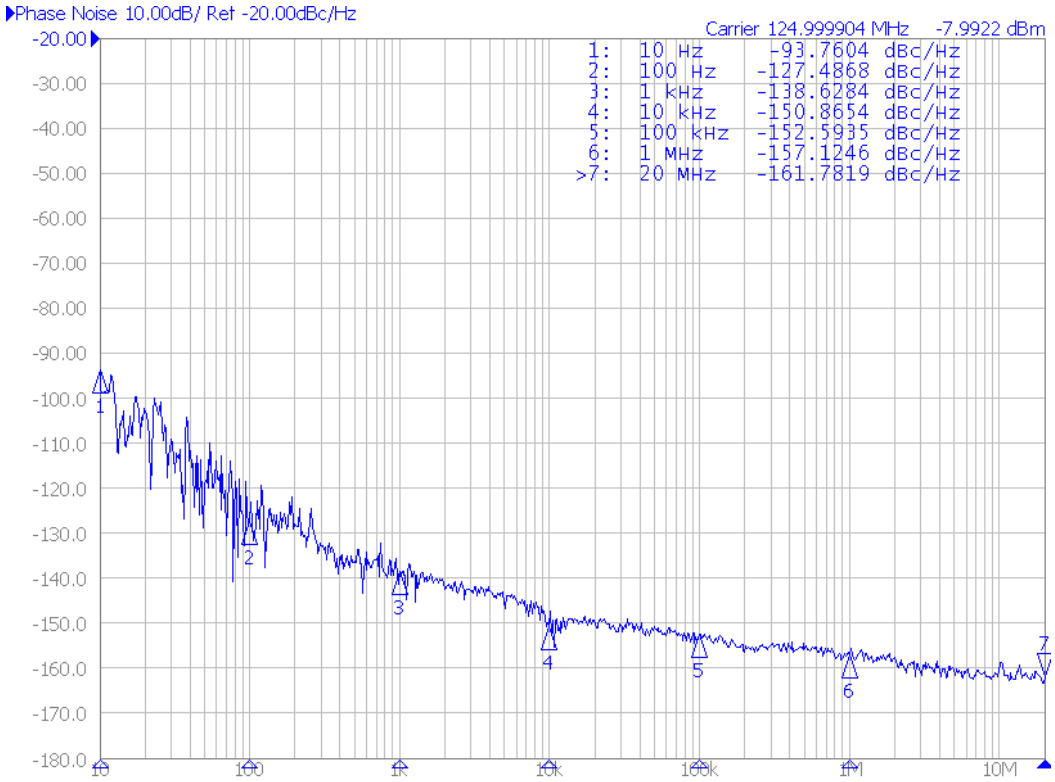

TABLE 2b – Typical Phase Noise Performance at 125 MHz

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**DOC203679**	I	**12**

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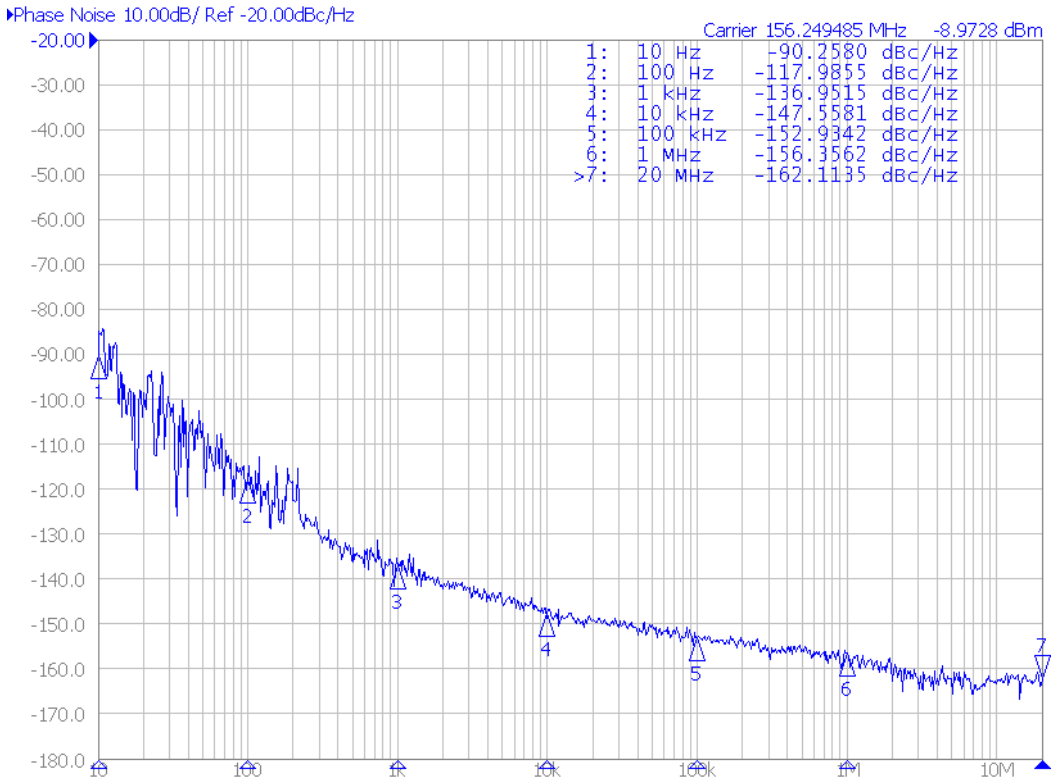

TABLE 2c – Typical Phase Noise Performance at 156.25 MHz

OPERATION LISTING	REQUIREMENTS AND CONDITIONS 1/
@ all Electrical tests	
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
@ Post Burn-In Electrical only	
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4 2/
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29
Enable/Disable, when applicable (verify only)	Nominal conditions only (Par. 4.4 herein)

1/. Waveform measurement points and logic limits are in accordance with Figure 1.
2/. The overvoltage specified for the LVDS oscillator shall be 3.6V.

TABLE 3 - Electrical Test Parameters

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Model #	Thermal Resistance Junction to Case θ_{jc} (°C / W)	Δ Junction Temp. T_j (°C @ max. power)	Weight (Grams)
1203/1219	15.40	2.40	1.5
All Others	16.22	2.53	3.0

Note: The maximum power from Table 2 is used to calculate the worst case Δ junction temperature.

TABLE 4 – Typical Thermal Characteristics and Weight

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OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option S	Option X
	SCREENING	MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)	K 100%	B- 100%	S- 100%	K+ 100%	B 100%	S (Rev E) 100%	100%	S (Rev F) 100%	EM 100%
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	NR	X	X	NR	X	NR	X	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K, Meth 2032 Class K	X	X	X	X	X	X	X	X	X
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.
4	Random Vibration	MIL-STD-883, Meth 2026, Cond I-B, 15 mins in each axis	NR	NR	NR	NR	NR	NR	NR	X	NR
5	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	NR	NR	X	NR	NR	X	NR	X	NR
6	Temperature Cycle	MIL-STD-883, Meth 1010, Cond. B (except Option S), 10 cycles min.	X	X	X	X	X	X	X	X Cond. C	NR
7	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	X	X	X	NR
8	Particle Impact Noise Detection	MIL-STD-883, Meth 2020, Cond B (except Option S)	X	X	X	X	X	X	NR	X Cond. A	X
9	Electrical Testing, Pre Burn-In	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	X	X	X	X	X	X	X	X
10	1st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 240 hrs.	NR
11	Electrical Testing, Intermediate	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	NR	NR	X	NR	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In (Group A) 4/	Perform tests in Table 3. Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X	X	X	X nom. Vcc	X	NR
14	Seal: Fine Leak Seal: Gross Leak	MIL-STD-202, Meth 112, Cond C (5 x 10^{-8} atm cc/sec max) MIL-STD-202, Meth 112, Cond D	X	X	X	X	X	X	X	NR	X
15	Seal: Fine Leak Seal: Gross Leak	MIL-STD-883, Meth 1014, Cond A2 or B1 MIL-STD-883, Meth 1014, Cond B2 or B3	NR	NR	NR	NR	NR	NR	NR	X	NR
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	AR	AR	X	AR	X	NR	X	NR
17	Solderability	MIL-STD-883, Meth 2003	1/	1/	1/	1/	1/	1/	1/	1/	NR
18	External Visual & Mechanical	MIL-STD-883, Meth 2009	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/
19	Aging, 30 Day 3/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	X	13 pcs.	X	NR	X	NR
20	Group C Inspection (optional)	See Para 5.2 herein for details of supplier recommended Group C Inspection options	5.2(g)	5.2(e)	5.2(e)	5.2(g)	5.2(e)	5.2(e)	5.2(e)	5.2(f)	NR

LEGEND: X = Required, NR = Not Required, AR = As Required

TABLE 5 - Test Matrix

1/ Performed at package LAT. Include LAT data sheet.
2/ When specified, RGA samples will be removed from the lot after completion of this operation. Use of Screening failures require customer concurrence.
3/ See paragraph 4.3.4.1 herein.
4/ See paragraph 5.3.1 herein.

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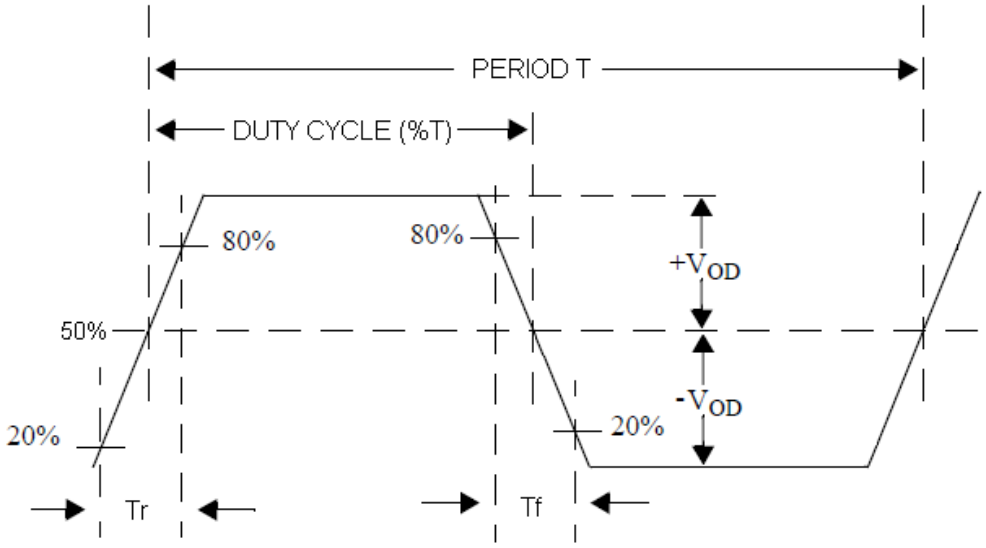

FIGURE 1
Differential Output Waveform

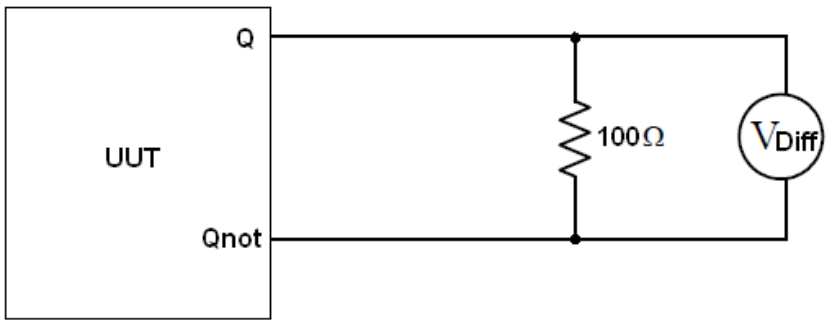

FIGURE 2
Output Load, 100Ω between outputs

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**DOC203679**	I	**16**

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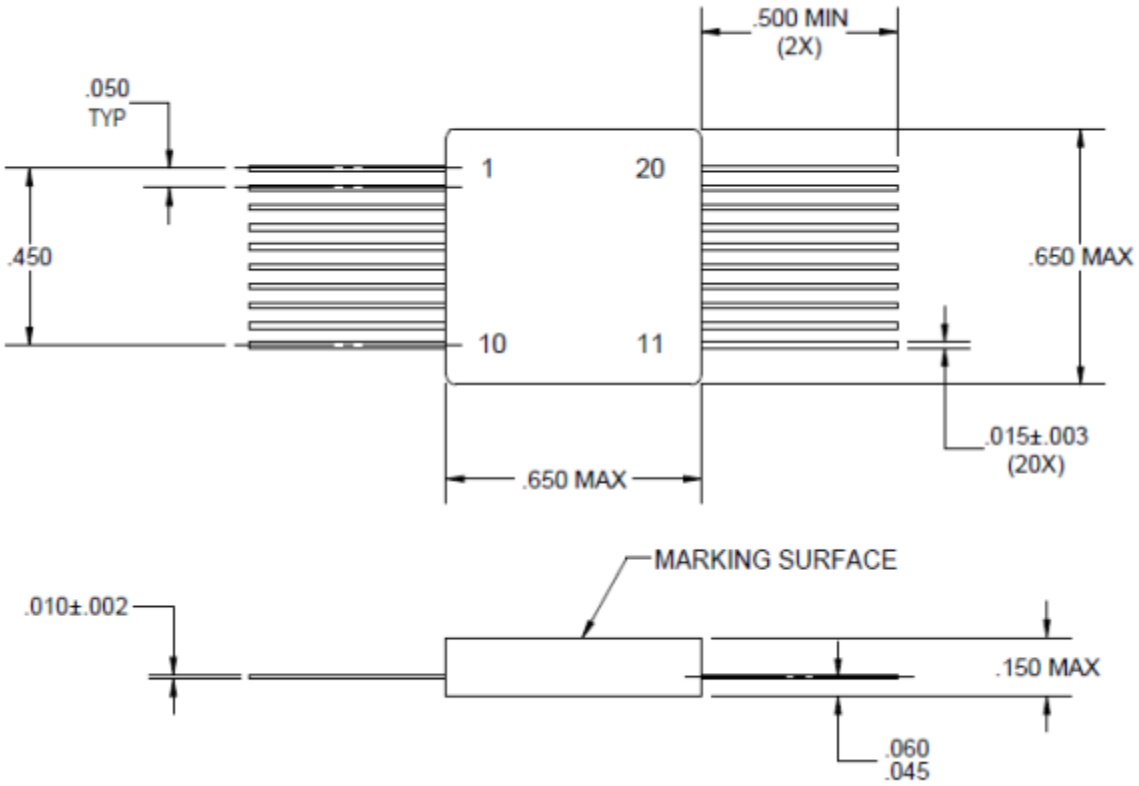

Model #	I/O Connections										
	Vcc	Q1	$\overline{Q}$ 1	Q2	$\overline{Q}$ 2	Q3	$\overline{Q}$ 3	Q4	$\overline{Q}$ 4	Enable 1/	Gnd/Case
1204	13,20	11	12	-	-	-	-	-	-	-	10
1208	20	11	12	14	15	-	-	-	-	13	10
1216	20	7	8	10	9	11	12	14	13	-	6,15

1/ Outputs are enabled when Pin 13 is left floating or 0V to 0.8V is applied. Outputs are disabled (high impedance) when 2.0V to Vcc is applied.

FIGURE 3
Model 1204/1208/1216 Package Outline and I/O Connections

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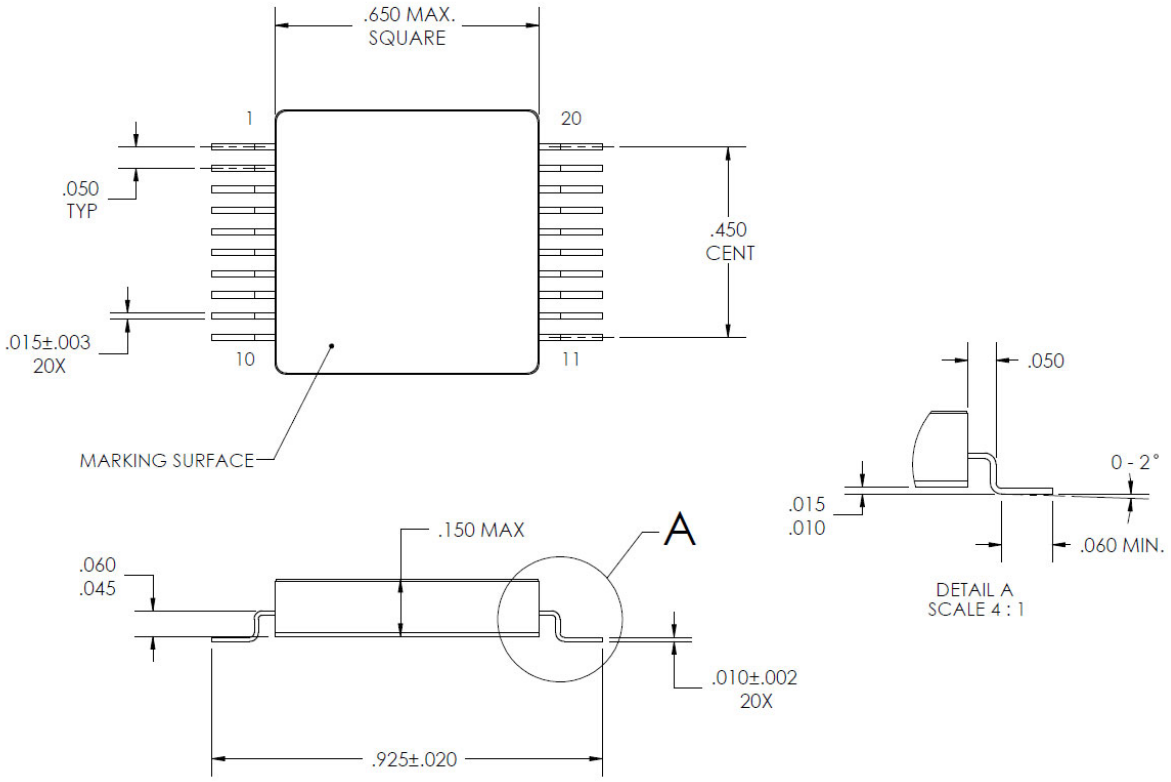

Model #	I/O Connections										
	Vcc	Q1	$\overline{Q}$ 1	Q2	$\overline{Q}$ 2	Q3	$\overline{Q}$ 3	Q4	$\overline{Q}$ 4	Enable 1/	Gnd/Case
1220	13,20	11	12	-	-	-	-	-	-	-	10
1240	20	11	12	14	15	-	-	-	-	13	10
1280	20	7	8	10	9	11	12	14	13	-	6,15

1/ Outputs are enabled when Pin 13 is left floating or 0V to 0.8V is applied. Outputs are disabled (high impedance) when 2.0V to Vcc is applied.

FIGURE 4
Model 1220/1240/1280 Package Outline and I/O Connections

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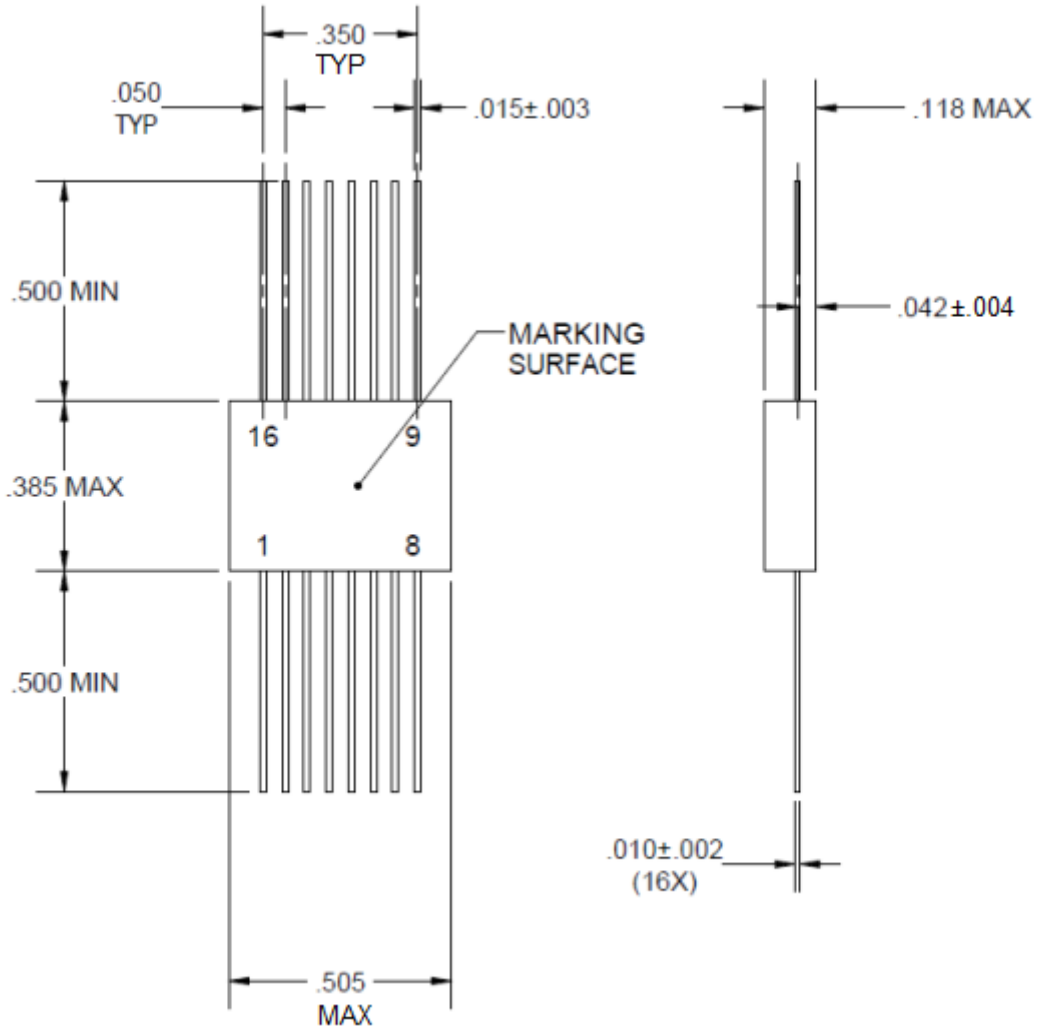

Model #	I/O Connections			
	Vcc	Q1	$\overline{Q}$ 1	Gnd/Case
1203	8	10	11	9

FIGURE 5
Model 1203 Package Outline and I/O Connections

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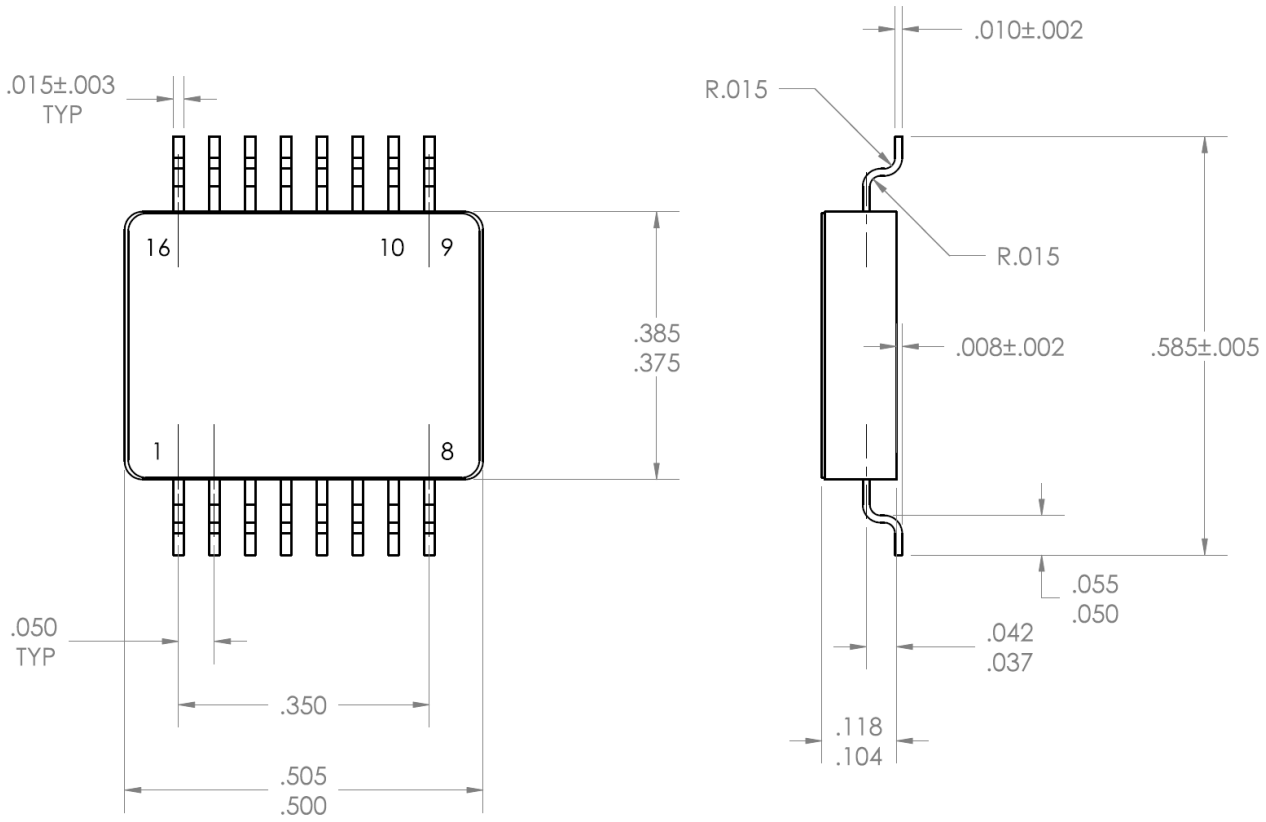

Model #	I/O Connections			
	Vcc	Q1	$\overline{Q}$ 1	Gnd/Case
1219	8	10	11	9

FIGURE 6
Model 1219 Package Outline and I/O Connections

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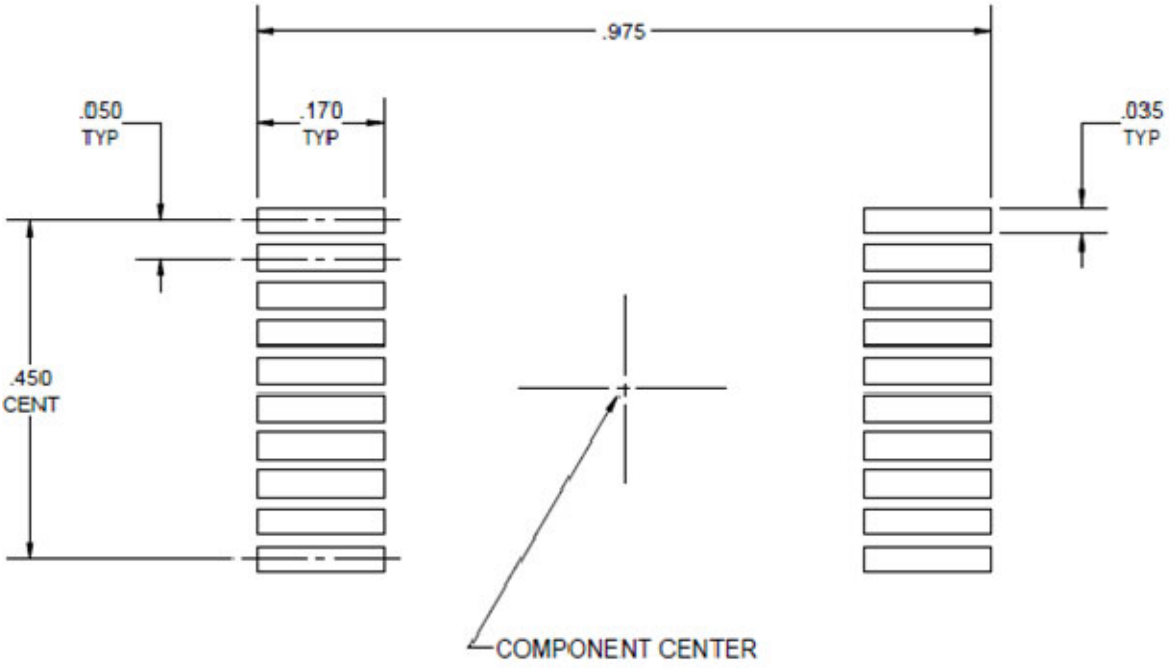
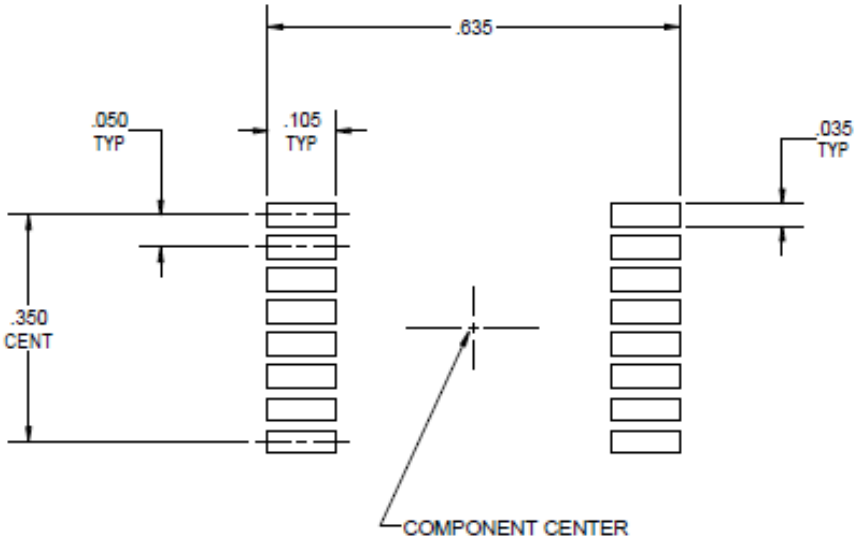
APPENDIX A

Recommended Land Pattern



Models 1220, 1240 and 1280



Model 1219

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**DOC203679**	I	**21**

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