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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD™

December 2014

FDPF041N06BL1

N-Channel PowerTrench® MOSFET

60 V, 77 A, 4.1 mΩ

Features

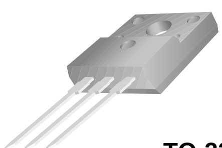
- $R_{DS(on)}$ = 3.5 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 77 A
- Low FOM $R_{DS(on)}$*Q_G
- Low Reverse Recovery Charge, Q_{rr}
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



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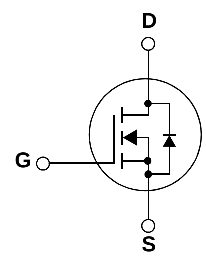
TO-220F



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FDPF041N06BL1	Unit
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited)	77	A
		- Continuous (T_C = 100°C, Silicon Limited)	55	
I_{DM}	Drain Current	- Pulsed (Note 1)	308	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		365	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	44.1	W
		- Derate above 25°C	0.29	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FDPF041N06BL1	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Packaging Type	Quantity
FDPF041N06BL1	FDPF041N06BL1	TO-220F	Tube	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.03	-	V/^{o}C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48V$, $V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 77A$	-	3.5	4.1	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 77A$	-	125	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 30V$, $V_{GS} = 0V$ f = 1MHz	-	4280	5690	pF
C_{oss}	Output Capacitance		-	1050	1400	pF
C_{rss}	Reverse Transfer Capacitance		-	23	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 30V$, $V_{GS} = 0V$	-	1787	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30V$, $I_D = 100A$ $V_{GS} = 10V$ (Note 4)	-	53	69	nC
Q_{gs}	Gate to Source Gate Charge		-	23	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	8	-	nC
$V_{plateau}$	Gate Plateau Volatge		-	5.7	-	V
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0V$, $I_D = 50A$ (Note 5)	-	48.6	-	nC
Q_{oss}	Output Charge	$V_{DS} = 30V$, $V_{GS} = 0V$	-	63.8	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30V$, $I_D = 100A$ $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	29	68	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	38	86	ns
t_f	Turn-Off Fall Time		-	11	32	ns
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	0.8	-	Ω
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	77	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	308	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 77A$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 100A$ $dI_F/dt = 100A/\mu s$	-	65	-	ns
Q_{rr}	Reverse Recovery Charge		-	63	-	nC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3mH, $I_{AS} = 15.6A$, Starting $T_J = 25°C$
3. $I_{SD} \le 100A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics
5. See the test circuit in page 8

Typical Performance Characteristics

Figure 1. On-Region Characteristics

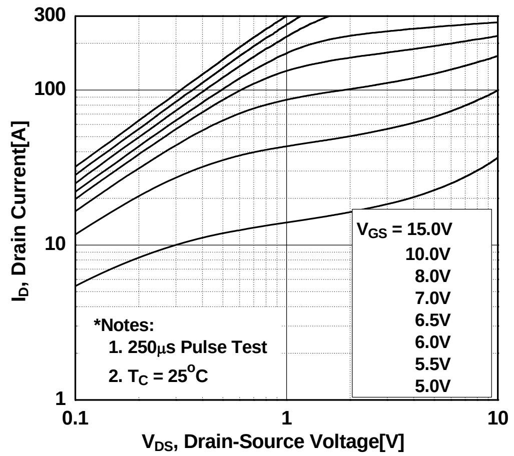


Figure 2. Transfer Characteristics

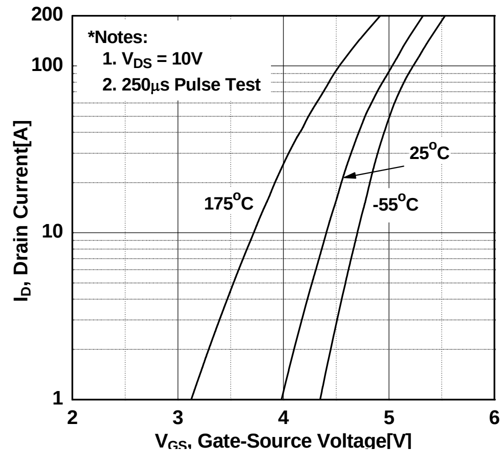


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

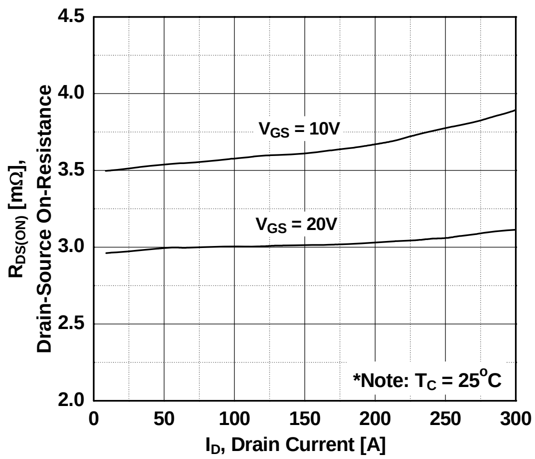


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

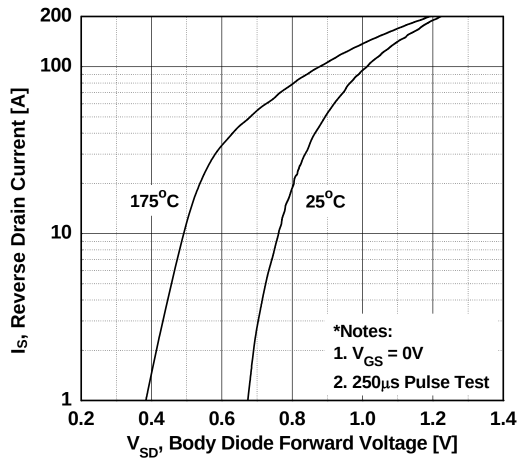


Figure 5. Capacitance Characteristics

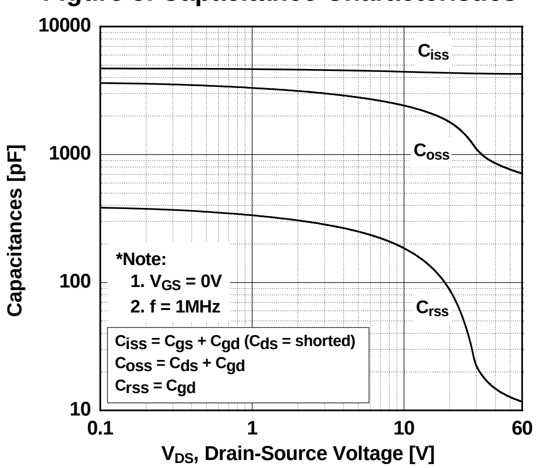
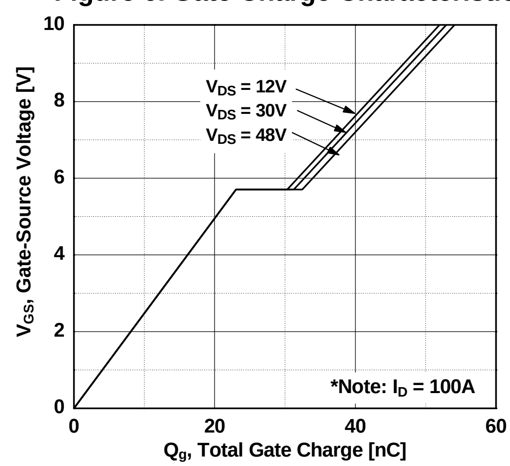


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

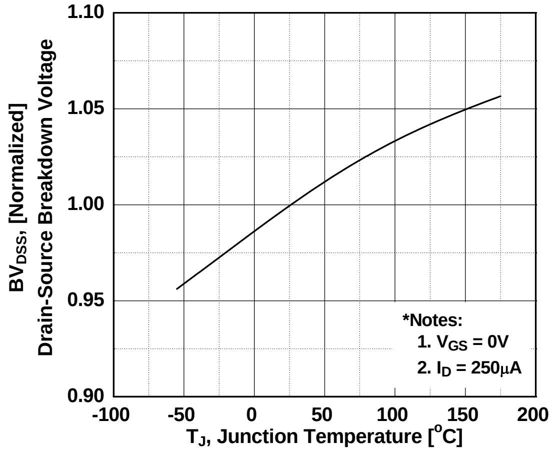


Figure 8. On-Resistance Variation vs. Temperature

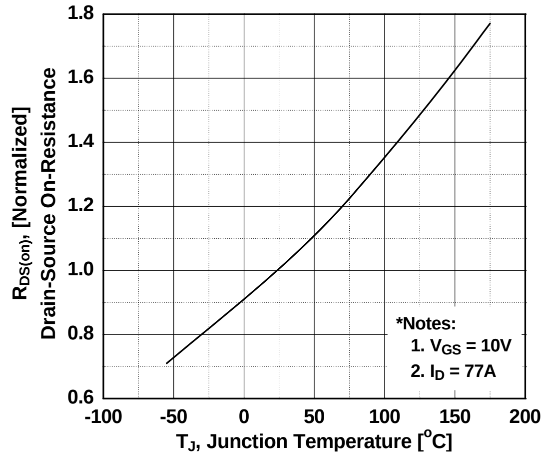


Figure 9. Maximum Safe Operating Area vs. Case Temperature

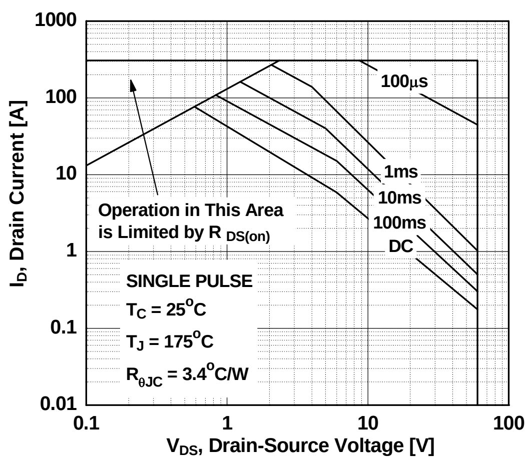


Figure 10. Maximum Drain Current

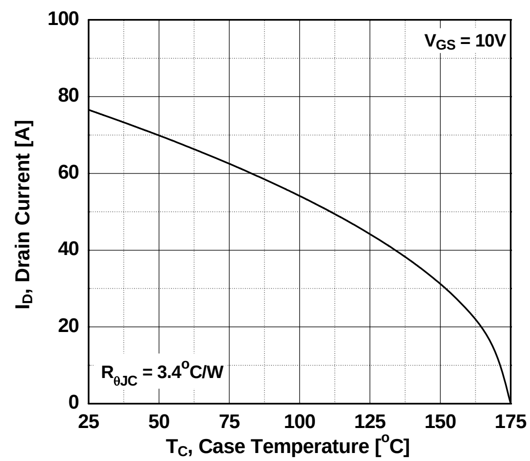


Figure 11. Eoss vs. Drain to Source Voltage

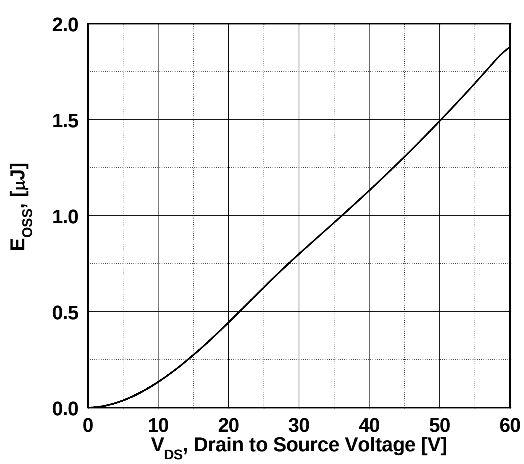
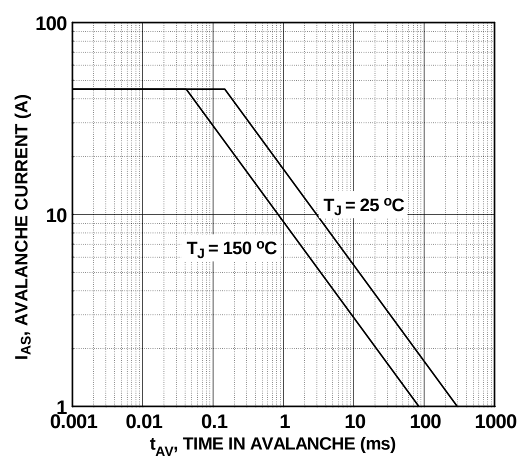
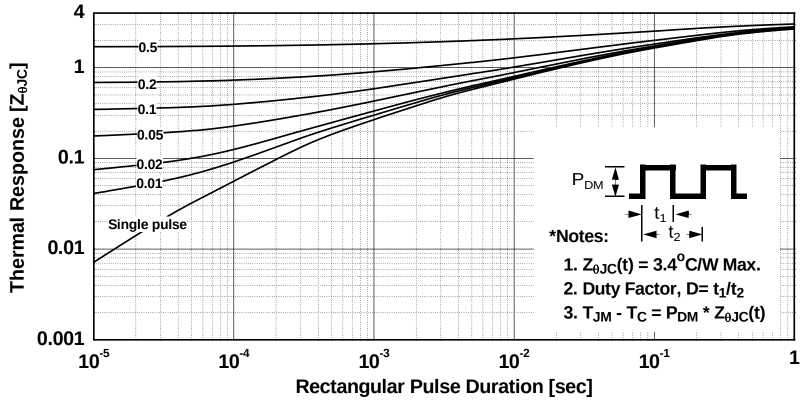


Figure 12. Unclamped Inductive Switching Capability

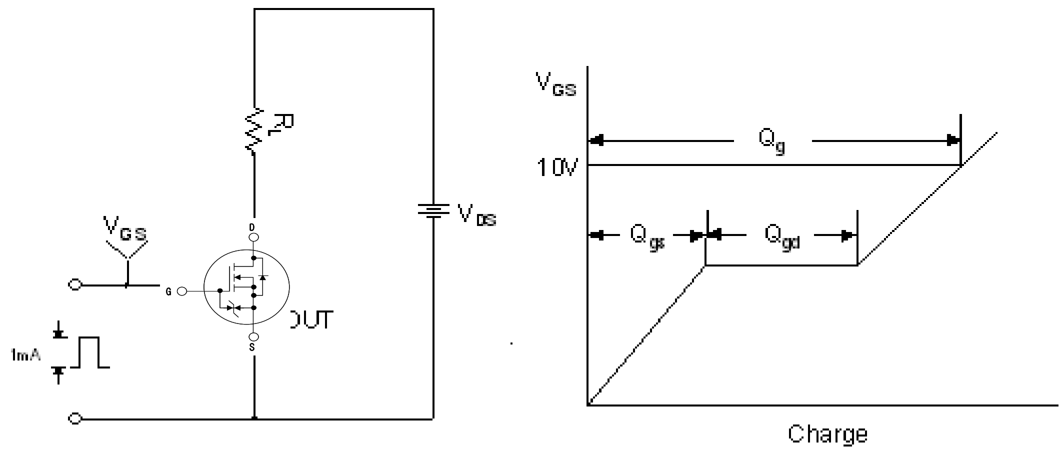


Typical Performance Characteristics (Continued)

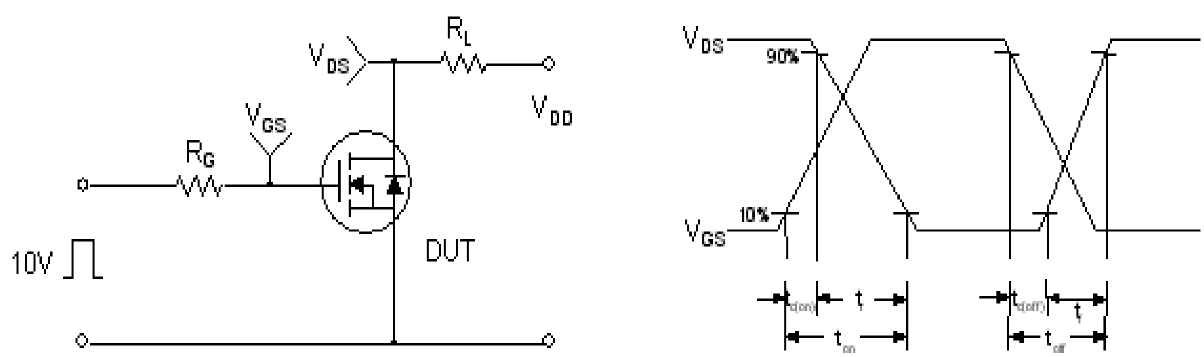
Figure 13. Transient Thermal Response Curve



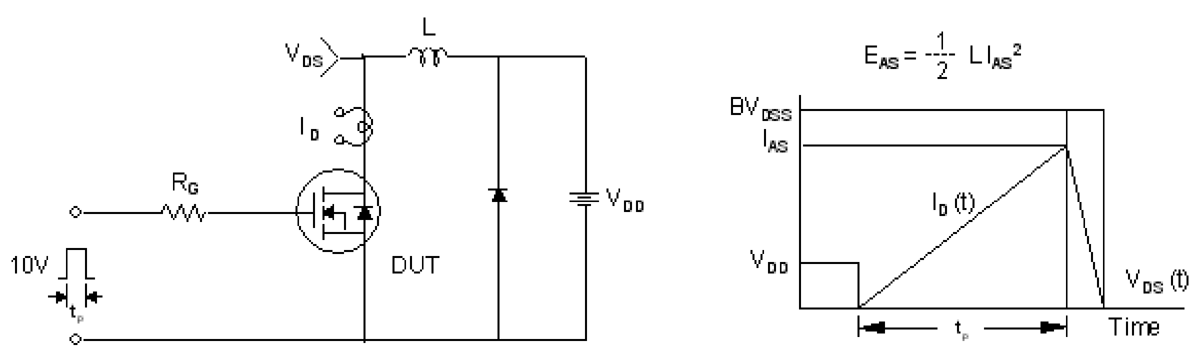
Gate Charge Test Circuit & Waveform



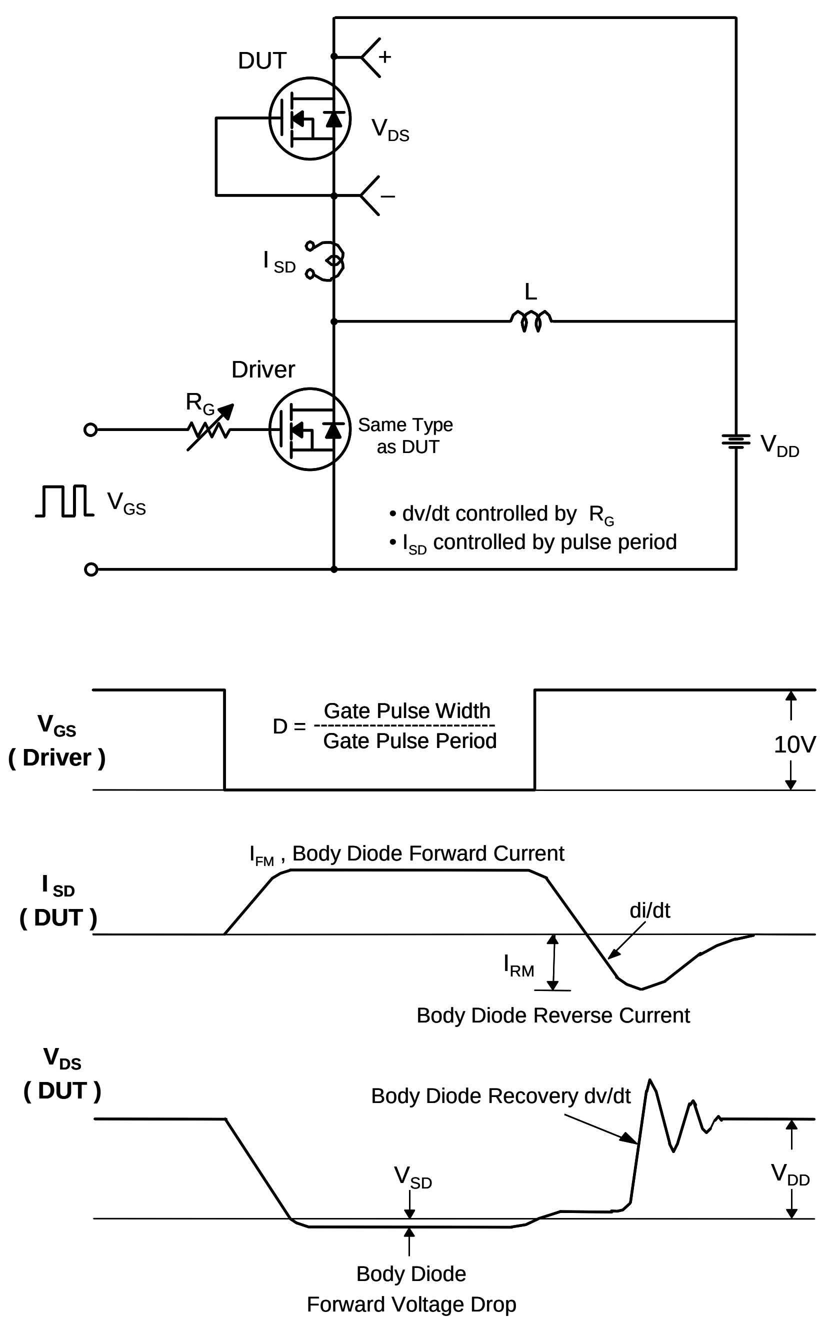
Resistive Switching Test Circuit & Waveforms



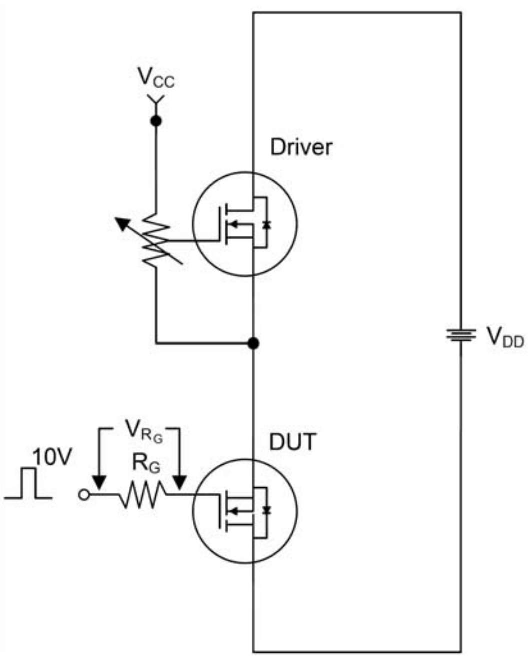
Unclamped Inductive Switching Test Circuit & Waveforms

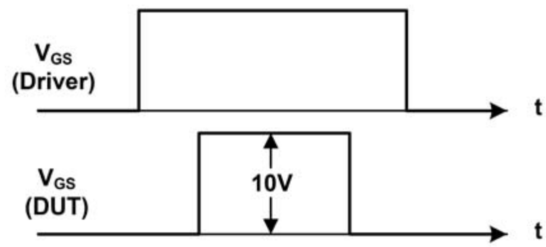


Peak Diode Recovery dv/dt Test Circuit & Waveforms

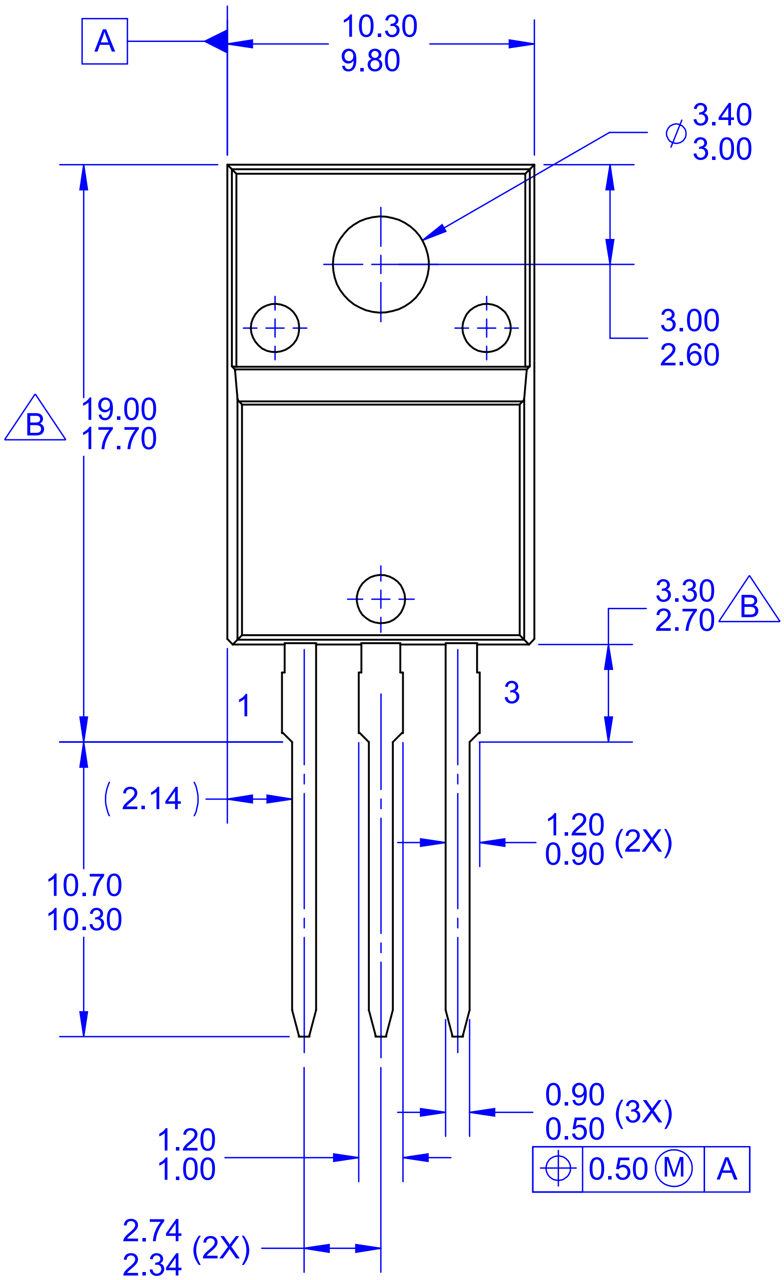


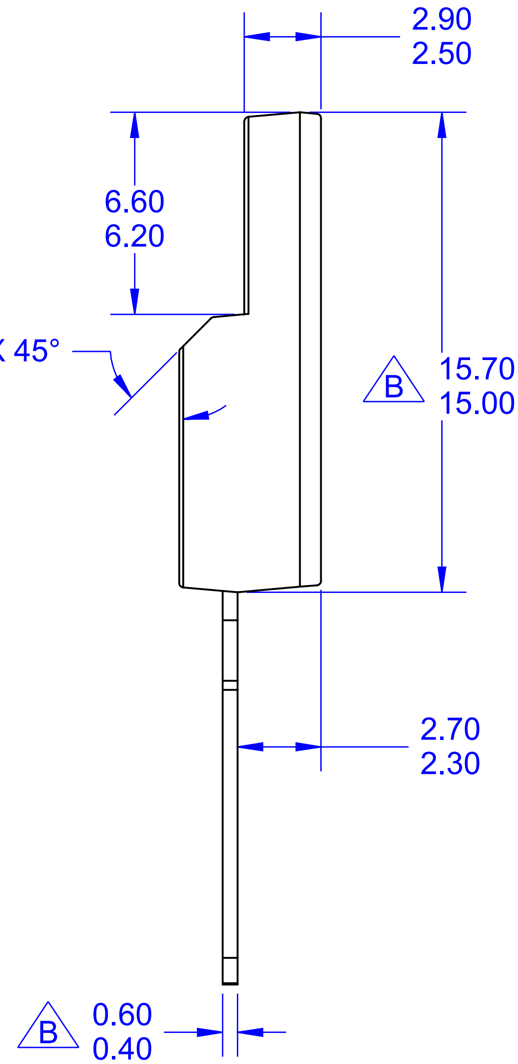
Total Gate Charge Qsync. Test Circuit & Waveforms

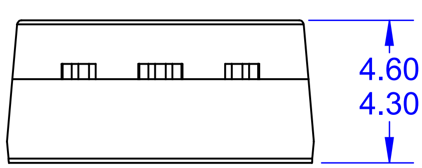




$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t)\ dt$$







NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
F. DRAWING FILE NAME: TO220V03REV1
G. FAIRCHILD SEMICONDUCTOR

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