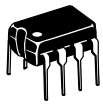
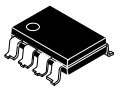
# Green Mode onsemi Buck Switch

# FSL336LR

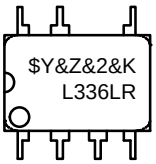


**PDIP−7 (PDIP−8 LESS PIN 6)**
**CASE 626A**



**PDIP7 MINUS PIN 6 GW**
**CASE 707AA**

## MARKING DIAGRAM




$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
LR336LR = Specific Device Code

## ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

### Description

The FSL336LR integrated Pulse Width Modulator (PWM) and SENSEFET® is specifically designed for high−performance offline buck, buck−boost, and non−isolation flyback Switched Mode Power Supplies (SMPS) with minimal external components. This device integrates a high−voltage power regulator that enables operation without auxiliary bias winding. An internal transconductance amplifier reduces external components for the feedback compensation circuit.

The integrated PWM controller includes: 10 V regulator for no external bias circuit, Under−Voltage Lockout (UVLO), Leading−Edge Blanking (LEB), an optimized gate turn−on / turn−off driver, EMI attenuator, Thermal Shutdown (TSD), temperature−compensated precision current sources for loop compensation, and fault−protection circuitry. Protections include: Overload Protection (OLP), Over−Voltage Protection (OVP), and Feedback Open Loop Protection (FB_OLP). FSL336LR offers good soft−start performance during startup.

The internal high−voltage startup switch and the Burst−Mode operation with very low operating current reduce the power loss in Standby Mode. As the result, it is possible to reach power loss of 120 mW without external bias and 25 mW with external bias when input voltage is 230 $V_{AC}$.

### Features

- Built−in Avalanche−Rugged SENSEFET: 650 V
- Fixed Operating Frequency: 50 kHz
- No−Load Power Consumption:
  <25 mW at 230 $V_{AC}$ with External Bias;
  <120 mW at 230 $V_{AC}$ without External Bias
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Pulse−by−Pulse Current Limiting
- Ultra−Low Operating Current: 250 μA
- Built−in Soft−Start and Startup Circuit
- Adjustable Peak Current Limit
- Built−in Transconductance (Error) Amplifier
- Various Protections: Overload Protection (OLP), Over−Voltage Protection (OVP), Feedback Open−Loop Protection (FB_OLP), Thermal Shutdown (TSD)
- Fixed 650 ms Restart Time for Safe Auto−Restart of All Protections
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

### Applications

- SMPS for Home Appliances and Industrial Applications
- SMPS for Auxiliary Power

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## APPLICATION DIAGRAMS

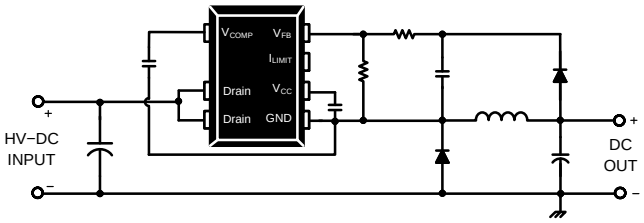


**Figure 1. Buck Converter Application**

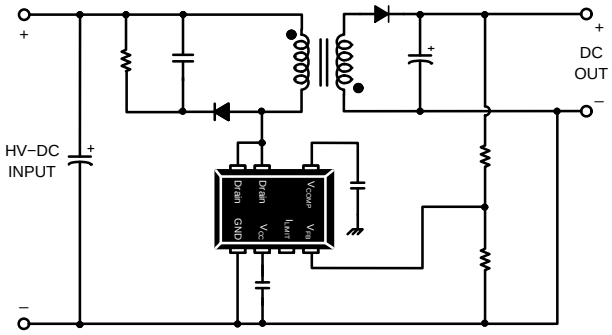


**Figure 2. Non−Isolation Flyback Converter Application**

## BLOCK DIAGRAM

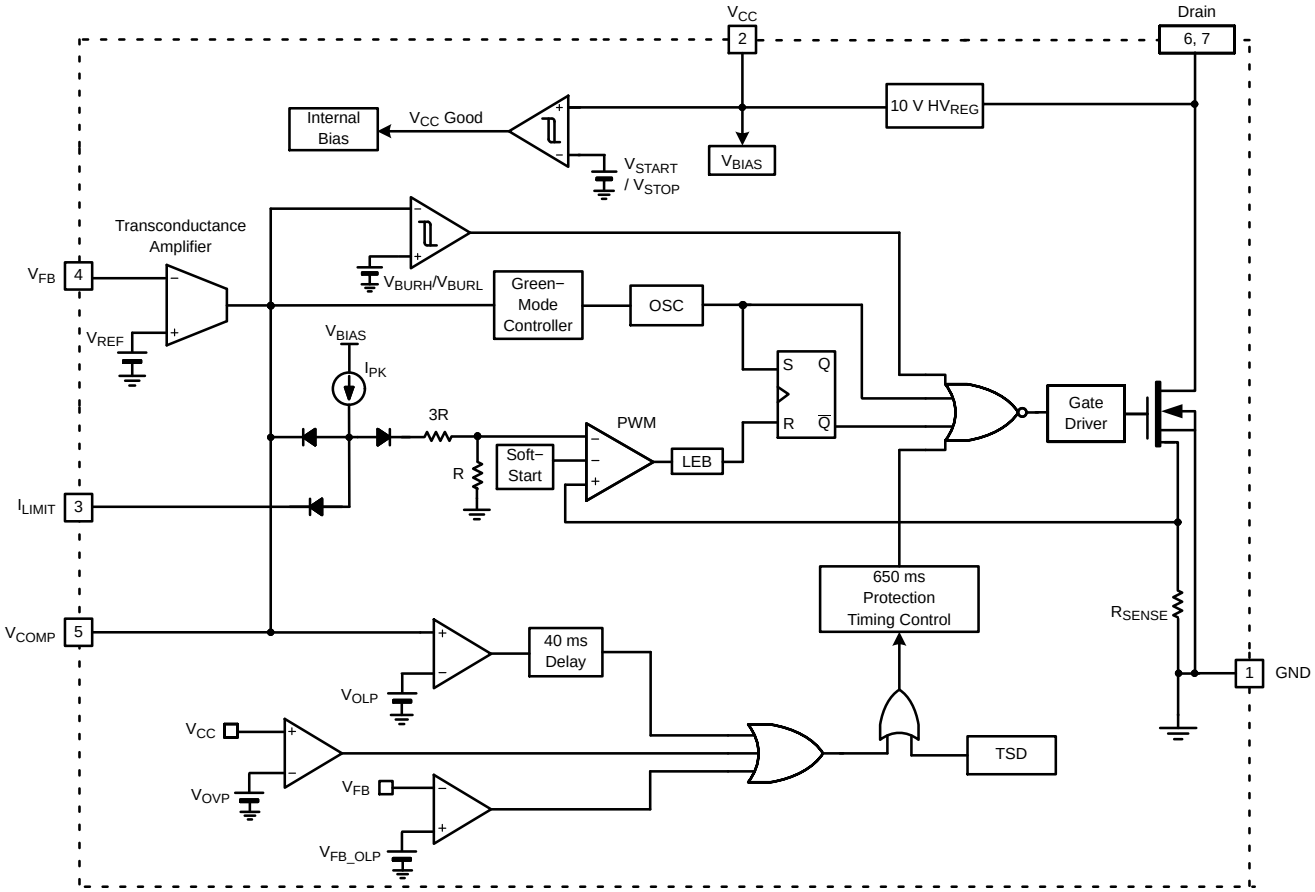


**Figure 3. Internal Block Diagram**



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## PIN CONFIGURATION

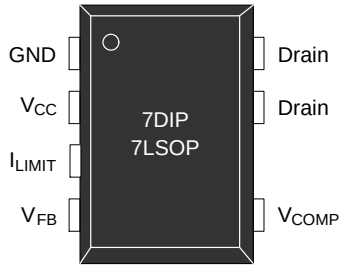


**Figure 4. Pin Configuration**

### PIN DEFINITIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | GND | *Ground*. SENSEFET source terminal on the primary side and internal control ground. |
| 2 | $V_{CC}$ | *Positive Supply Voltage Input*. This pin is the positive supply input that provides the internal operating current for startup and steady−state operation. This pin voltage is regulated to 10 V, without the external bias circuit, via an internal 10−V HVREG *(see Figure 3)*. When the external bias voltage is >10 V, it disables the internal high−voltage regulator to reduce power consumption. |
| 3 | $I_{LIMIT}$ | *Peak Current Limit*. Adjusts the peak current limit of the SENSEFET. The internal 50 μA current source is diverted to the parallel combination of an internal 46 kΩ (3R + R) resistor and any external resistor to GND on this pin to determine the peak current limit. |
| 4 | $V_{FB}$ | *Feedback Voltage*. Inverting input of the transconductance amplifier. This pin controls the converter output voltage by outputting a VCOMP−pin current proportional to the difference between the reference voltage and the output voltage divided by external resistor divider. |
| 5 | $V_{COMP}$ | *Comp Voltage*. Output of the transconductance amplifier. The compensation networks are placed between the $V_{COMP}$ and GND pins to achieve stability and good dynamic performance. |
| 6, 7 | Drain | *Drain*. High−voltage power SENSEFET drain connection. In addition, during startup and steady−state operation; the internal high−voltage current source supplies internal bias and charges the external capacitor connected to the $V_{CC}$ pin. Once $V_{CC}$ reaches 8 V, all internal blocks are activated. The internal high−voltage current source is enabled until $V_{CC}$ reaches 10 V. After that, the internal high−voltage regulator turns on and off regularly to maintain $V_{CC}$ at 10 V. |



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**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain Pin Voltage | −0.3 | 650.0 | V |
| $V_{CC}$ | Supply Voltage | −0.3 | 26.0 | V |
| $V_{COMP}$ | $V_{COMP}$ Pin Voltage | −0.3 | Internally Clamped Voltage (Note 1) | V |
| $V_{FB}$ | Feedback Voltage | −0.3 | 12.0 | V |
| $I_{LIMIT}$ | Current Limit Pin Voltage | −0.3 | 12.0 | V |
| $I_{DM}$ | Drain Current Pulsed (Note 2) | − | 12 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy (Note 3) | − | 230 | mJ |
| $P_D$ | Total Power Dissipation | − | 1.25 | W |
| $T_J$ | Operating Junction Temperature (Note 4) | −40 | 125 | °C |
| | Maximum Junction Temperature | − | 150 | °C |
| $T_{STG}$ | Storage Temperature | −55 | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{COMP}$ is clamped by internal clamping diode (11 V, $I_{CLAMP_MAX}$ < 100 μA).
2. Repetitive rating: pulse width is limited by maximum junction temperature.
3. L = 51 mH, starting $T_J$ = 25°C.
4. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

**THERMAL IMPEDANCE** ($T_A$ = 25°C unless otherwise specified)

| Symbol | Characteristic | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction−to−Ambient Thermal Impedance (Note 5) | 100 | °C/W |

5. JEDEC recommended environment, JESD51−2, and test board, JESD51−3, with minimum land pattern.

**ESD CAPABILITY**

| Symbol | Characteristic | Value | Unit |
|---|---|---|---|
| ESD | Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 6) | 4 | kV |
| | Charged Device Model, JESD22−C101 (Note 6) | 2 | |

6. Meets JEDEC standards ANSI/ESDA/JEDEC JS−001−2012 and JESD 22−C101.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SENSEFET SECTION** | | | | | | |
| $BV_{DSS}$ | Drain−Source Breakdown Voltage | $V_{CC}$ = 0 V, $I_D$ = 250 μA | 650 | − | − | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 520 V, $T_A$ = 125°C | − | − | 250 | μA |
| $R_{DS(ON)}$ | Drain−Source On−State Resistance | $V_{GS}$ = 10 V, $I_D$ = 1 A | − | 3.5 | 4.0 | Ω |
| $C_{ISS}$ | Input Capacitances | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | − | 290 | − | pF |
| $C_{OSS}$ | Output Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | − | 45 | − | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | − | 5.5 | − | pF |
| $t_r$ | Rise Time | $V_{DD}$ = 350 V, $I_D$ = 3.5 A | − | 22 | − | ns |
| $t_f$ | Fall Time | $V_{DD}$ = 350 V, $I_D$ = 3.5 A | − | 19 | − | ns |
| **CONTROL SECTION** | | | | | | |
| $f_{OSC}$ | Switching Frequency | $V_{COMP}$ = 2.5 V | 45 | 50 | 55 | kHz |
| $f_M$ | Frequency Modulation (Note 7) | $V_{COMP}$ = 2.5 V, Randomly | − | ±3 | − | kHz |
| $t_{on.max}$ | Maximum Turn−On Time | $V_{COMP}$ = 2.5 V | 11.2 | 13.3 | 15.4 | μs |



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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise specified) (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CONTROL SECTION** | | | | | | |
| $V_{START}$ | UVLO Threshold Voltage | $V_{COMP}$ = 0 V, $V_{CC}$ Sweep | 7.2 | 8.0 | 8.8 | V |
| $V_{STOP}$ | | After Turn On | 6.3 | 7.0 | 7.7 | V |
| $I_{PK}$ | Current Limit Source Current | $V_{COMP}$ = 2.5 V | 35 | 50 | 65 | μA |
| $t_{SS}$ | Soft−Start Time | $V_{COMP}$ = 2.5 V | 7 | 10 | 13 | ms |
| **BURST MODE SECTION** | | | | | | |
| $V_{BURH}$ | Burst−Mode HIGH Threshold Voltage | $V_{CC}$ = 15 V, $V_{COMP}$ Increase | 0.58 | 0.65 | 0.72 | V |
| $V_{BURL}$ | Burst−Mode LOW Threshold Voltage | $V_{CC}$ = 15 V, $V_{COMP}$ Decrease | 0.52 | 0.59 | 0.66 | V |
| $HYS_{BUR}$ | Burst−Mode Hysteresis | | − | 60 | − | mV |
| **PROTECTION SECTION** | | | | | | |
| $I_{LIM}$ | Peak Current Limit | $V_{COMP}$ = 2.5 V, di/dt = 1.2 A/μs | 1.6 | 1.8 | 2.0 | A |
| $t_{CLD}$ | Current Limit Delay (Note 7) | | − | 200 | − | ns |
| $V_{OLP}$ | Overload Protection | $V_{COMP}$ Increase | 2.7 | 3.0 | 3.3 | V |
| $t_{LEB}$ | Leading−Edge Blanking Time (Note 7) | | − | 200 | − | ns |
| $V_{FB_OLP}$ | FB Open−Loop Protection | $V_{FB}$ Decrease | 0.4 | 0.5 | 0.6 | V |
| $V_{OVP}$ | Over−Voltage Protection | $V_{CC}$ Increase | 23.0 | 24.5 | 26.0 | V |
| TSD | Thermal Shutdown Temperature (Note 7) | | 125 | 135 | 150 | °C |
| $HYS_{TSD}$ | TSD Hysteresis Temperature (Note 7) | | − | 60 | − | °C |
| $t_{DELAY}$ | Overload Protection Delay (Note 7) | $V_{COMP}$ > 3 V | − | 40 | − | ms |
| $t_{RESTART}$ | Restart Time After Protection (Note 7) | | − | 650 | − | ms |
| **TRANSCONDUCTANCE AMPLIFIER SECTION** | | | | | | |
| $G_m$ | Transconductance of Error Amplifier | | 380 | 480 | 580 | μmho |
| $V_{REF}$ | Voltage Feedback Reference | | 2.45 | 2.50 | 2.55 | V |
| $I_{EA.SR}$ | Output Sourcing Current | $V_{FB}$ = $V_{REF}$ − 0.025 V | − | −12 | − | μA |
| $I_{EA.SK}$ | Output Sink Current | $V_{FB}$ = $V_{REF}$ + 0.025 V | − | 12 | − | μA |
| **HIGH−VOLTAGE REGULATOR SECTION** | | | | | | |
| $V_{HVREG}$ | HV Regulator Voltage | $V_{COMP}$ = 0 V, $V_{DRAIN}$ = 40 V | 9 | 10 | 11 | V |
| **TOTAL DEVICE SECTION** | | | | | | |
| $I_{OP1}$ | Operating Supply Current (Control Part Only, without Switching) | 0 V < $V_{COMP}$ < $V_{BURL}$ | − | 0.25 | 0.35 | mA |
| $I_{OP2}$ | Operating Supply Current (While Switching) | $V_{BURL}$ < $V_{COMP}$ < $V_{OLP}$ | − | 0.8 | 1.3 | mA |
| $I_{CH}$ | Startup Charging Current | $V_{CC}$ = 0 V, $V_{DRAIN}$ > 40 V | − | 6 | − | mA |
| $I_{START}$ | Startup Current | $V_{CC}$ = Before $V_{START}$, $V_{COMP}$ = 0 V | − | 120 | 155 | μA |
| $V_{DRAIN}$ | Minimum Drain Supply Voltage | $V_{CC}$ = $V_{COMP}$ = 0 V, $V_{DRAIN}$ Increase | − | 35 | − | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Though guaranteed by design; not 100% tested in production.



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## TYPICAL PERFORMANCE CHARACTERISTICS

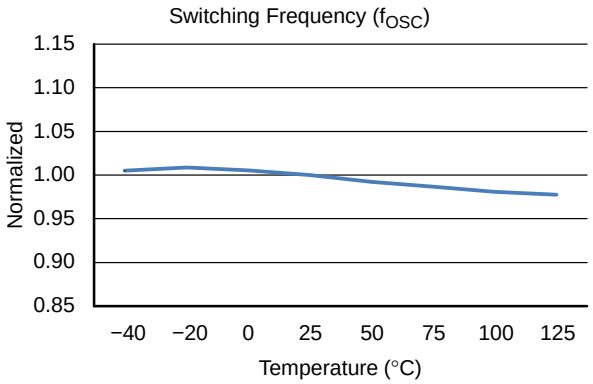


**Figure 5. Operating Frequency vs. Temperature**

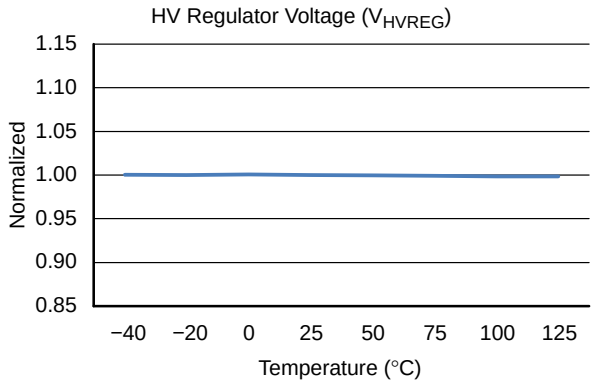


**Figure 6. HV Regulator Voltage vs. Temperature**

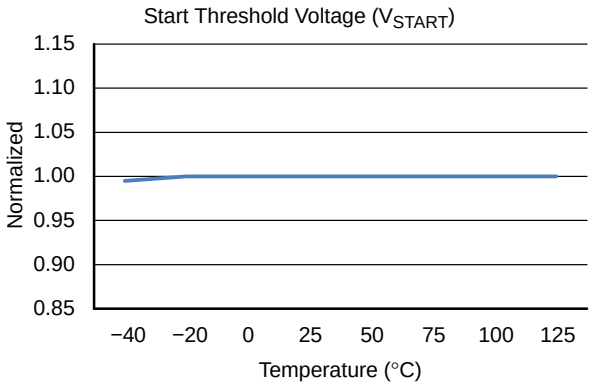


**Figure 7. Start Threshold Voltage vs. Temperature**

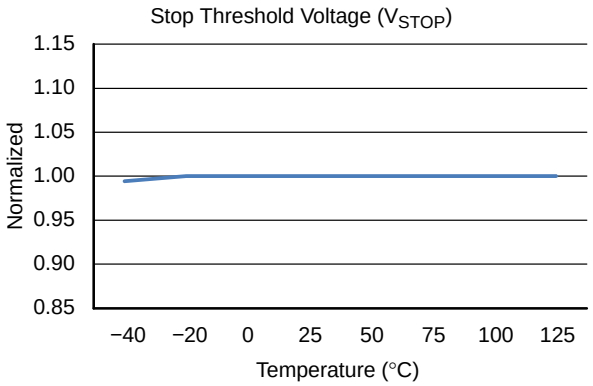


**Figure 8. Stop Threshold Voltage vs. Temperature**

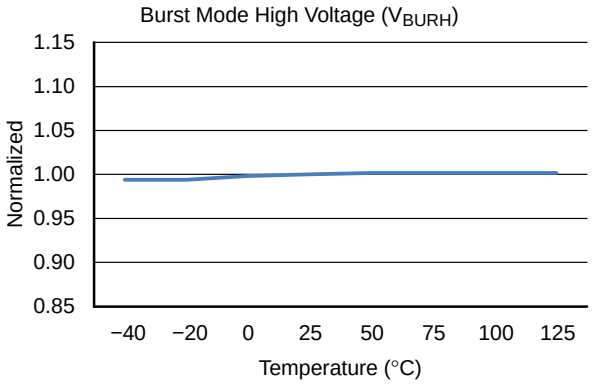


**Figure 9. Burst Mode High Voltage vs. Temperature**

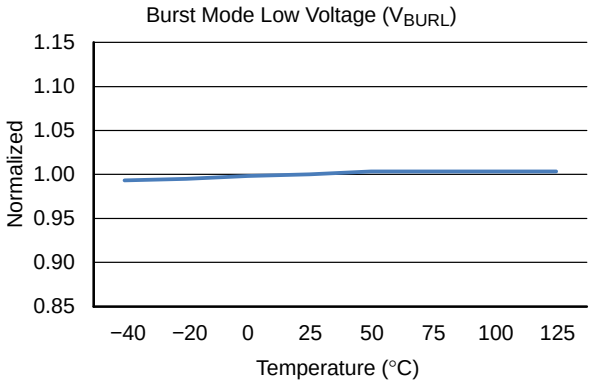


**Figure 10. Burst Mode Low Voltage vs. Temperature**



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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

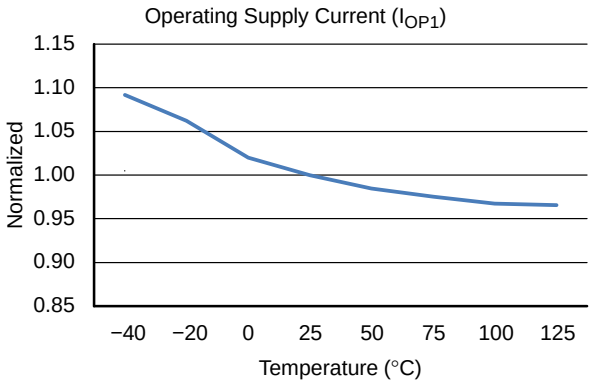


**Figure 11. Operating Supply Current 1 vs. Temperature**

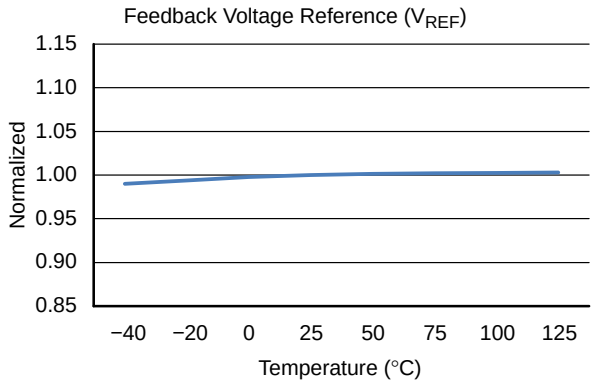


**Figure 12. Feedback Voltage Reference vs. Temperature**

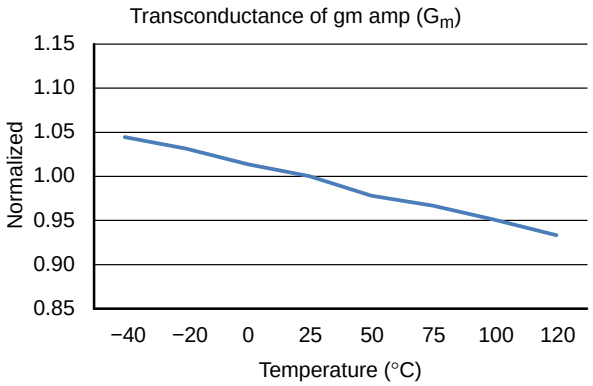


**Figure 13. Transconductance of gm Amplifier vs. Temperature**

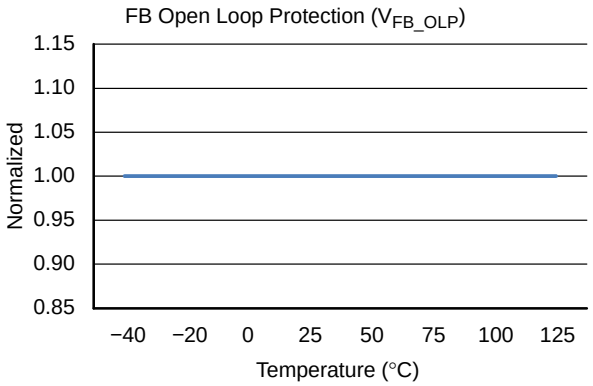


**Figure 14. FB Open−Loop Protection Voltage vs. Temperature**

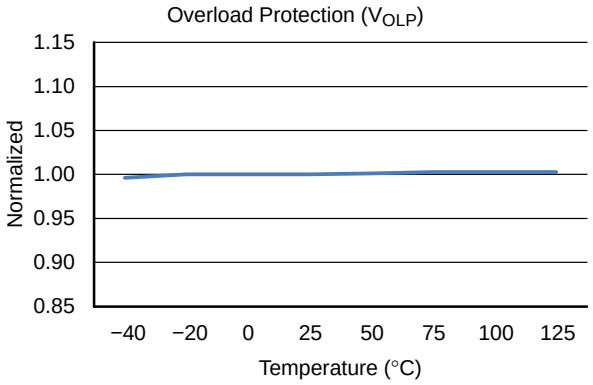


**Figure 15. Overload Protection vs. Temperature**

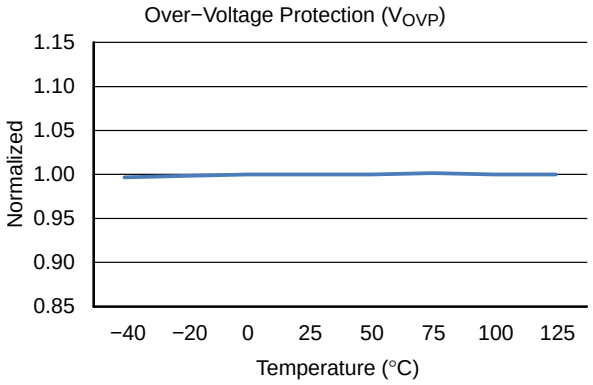


**Figure 16. Over−Voltage Protection vs. Temperature**



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## FUNCTIONAL DESCRIPTION

### Startup and High−Voltage Regulator

During startup, an internal high−voltage current source ($I_{CH}$) of the high−voltage regulator supplies the internal bias current ($I_{START}$) and charges the external capacitor ($C_A$) connected to the $V_{CC}$ pin, as illustrated in Figure 17. This internal high−voltage current source is enabled until $V_{CC}$ reaches 10 V. During steady−state operation, this internal high−voltage regulator ($HV_{REG}$) maintains the $V_{CC}$ with 10 V and provides operating current ($I_{OP}$) for all internal circuits. Therefore, no external bias circuit is necessary. The high−voltage regulator is disabled when the external bias is higher than 10 V.

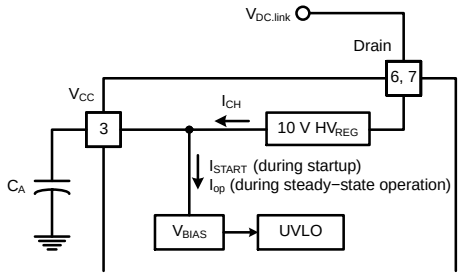


**Figure 17. Startup and $HV_{REG}$ Block**

### Oscillator Block

The oscillator frequency is set internally with a random frequency fluctuation function. Fluctuation of the switching frequency can reduce Electro−Magnetic Induction (EMI) by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the range of the frequency variation. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and an internal free−running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost−effective inductor instead of an AC input line filter to satisfy world−wide EMI requirements.

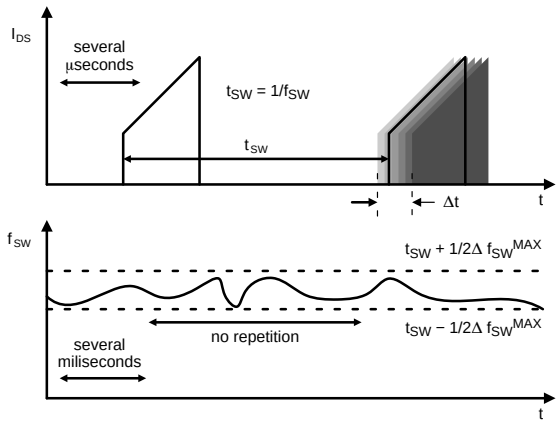


**Figure 18. Frequency Fluctuation Waveform**

### Feedback Control

The FSL336LR employs current−mode control with a transconductance amplifier for feedback control, as shown in Figure 19. Two resistors are typically used on the $V_{FB}$ pin to sense output voltage. An external compensation circuit is recommended on the $V_{COMP}$ pin to control output voltage. A built−in transconductance amplifier accurately controls output voltage without external components, such as Zener diode and transistor.

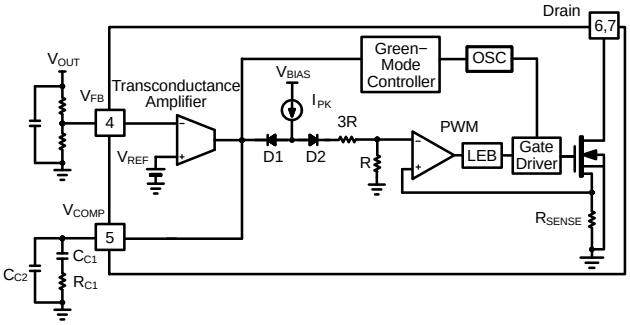


**Figure 19. Pulse Width Modulation (PWM) Circuit**

*Transconductance Amplifier (gm Amplifier)*

The output of the transconductance amplifier sources and sinks the current, respectively, to and from the compensation circuit connected on the $V_{COMP}$ pin *(see Figure 20)*. This compensated $V_{COMP}$ pin voltage controls the switching duty cycle by comparing with the voltage across the $R_{SENSE}$. When the feedback pin voltage exceeds the internal reference voltage ($V_{REF}$) of 2.5 V; the transconductance amplifier sinks the current from the compensation circuit, $V_{COMP}$ is pulled down, and the duty cycle is reduced. This typically occurs when input voltage is increased or output load is decreased. A two−pole and one−zero compensation network is recommended for optimal output voltage control and AC dynamics. Typically 220 nF, 75 kΩ, and 220 pF are used for $C_{C1}$, $R_{C1}$, and $C_{C2}$; respectively.

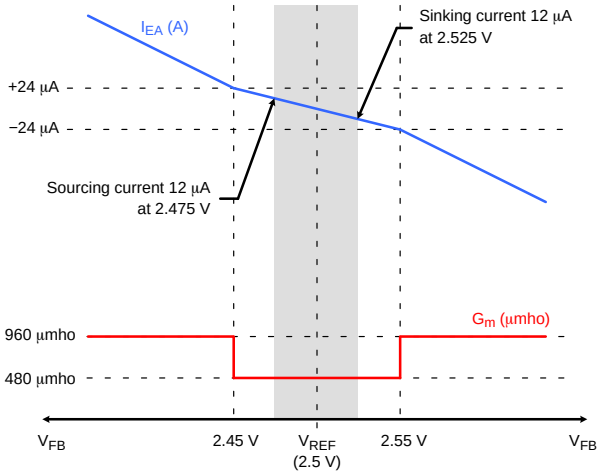


**Figure 20. Characteristics of gm Amplifier**



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*Pulse−by−Pulse Current Limit*

Because current−mode control is employed, the peak current flowing through the SENSEFET is limited by the inverting input of PWM comparator, as shown in Figure 19. Assuming that 50 μA current source flows only through the internal resistors (3R + R = 46 kΩ), the cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when $V_{COMP}$ exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current of the SENSEFET is limited.

*Leading Edge Blanking (LEB)*

At the instant the internal SENSEFET is turned on, a high−current spike through the SENSEFET is typically caused by: primary−side capacitance and secondary−side rectifier diode reverse recovery of flyback application, the freewheeling diode reverse recovery, and other parasitic capacitance of buck application. Excessive voltage across the sensing resistor ($R_{SENSE}$) leads to incorrect feedback operation in the current−mode control. To counter this effect, the FSL336LR has a Leading−Edge Blanking (LEB) circuit *(see Figure 19)*. This circuit inhibits the PWM comparator for a short time ($t_{LEB}$) after the SENSEFET is turned on.

## Protection Circuits

The protective functions include Overload Protection (OLP), Over−Voltage Protection (OVP), Under−Voltage Lockout (UVLO), Feedback Open−Loop Protection (FB_OLP), and Thermal Shutdown (TSD). All of the protections operate in Auto−Restart Mode. Since these protection circuits are fully integrated within the IC without external components, reliability is improved without increasing cost or PCB space. If a fault condition occurs, switching is terminated and the SENSEFET remains off. At the same time, internal protection timing control is activated to decrease power consumption and stress on passive and active components during Auto−Restart Mode. When internal protection timing control is activated, $V_{CC}$ is regulated with 10 V through the internal high−voltage regulator until switching is terminated. This internal protection timing control continues until the restart time (650 ms) expires. After 650 ms, the internal high−voltage regulator is disabled and $V_{CC}$ is decreased. When $V_{CC}$ reaches the UVLO stop voltage $V_{STOP}$ (7 V), the protection is reset and the internal high−voltage current source charges the $V_{CC}$ capacitor via the drain pin again. When $V_{CC}$ reaches the UVLO start voltage, $V_{START}$ (8 V), normal operation resumes. In this manner, Auto−Restart Mode can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated.

*Overload Protection (OLP)*

Overload is defined as the load current exceeding a preset level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, when the SMPS operates normally, the OLP circuit can be enabled during load transition or startup. To avoid this undesired operation, an internal fixed delay (40 ms) circuit determines whether it is a transient situation or a true overload situation *(see Figure 21)*. The current−mode feedback path limits the maximum power current and, when the output consumes more than this maximum power, the output voltage ($V_O$) decreases below its rated voltage. This reduces feedback pin voltage, which increases the output current of the internal transconductance amplifier. Eventually $V_{COMP}$ is increased. When $V_{COMP}$ reaches 3 V, the internal fixed OLP delay (40 ms) is activated. After this delay, the switching operation is terminated, as shown in Figure 22.

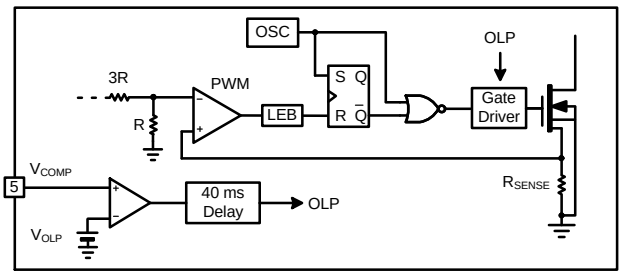


**Figure 21. Overload Protection Internal Circuit**

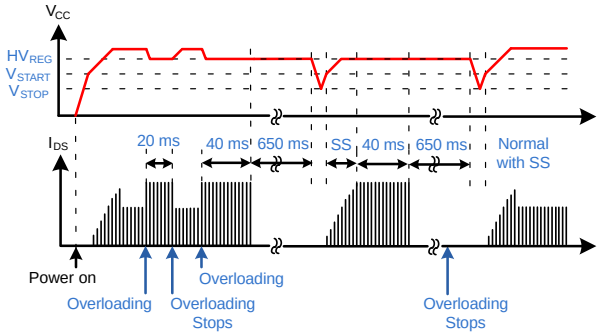


**Figure 22. Overload Protection (OLP) Waveform**

*Thermal Shutdown (TSD)*

The SENSEFET and control IC integrated on the same package makes it easier to detect the temperature of the SENSEFET. When the junction temperature exceeds 135°C, thermal shutdown is activated. The FSL336LR is restarted after the temperature decreases to 60°C.

*Over−Voltage Protection (OVP)*

If any feedback loop components fail due to a soldering defect, $V_{COMP}$ climbs up in manner similar to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the OLP is triggered. In this case, excessive energy is provided to the output and the output voltage may exceed the rated voltage before the OLP is activated. To prevent this situation, an Over−Voltage Protection (OVP) circuit is employed. In general, output voltage can be monitored through $V_{CC}$ and, when $V_{CC}$ exceeds 24.5 V, OVP is triggered, resulting in termination of switching operation. To avoid undesired activation of OVP during normal operation, $V_{CC}$ should be designed below 24.5 V *(see Figure 23)*.



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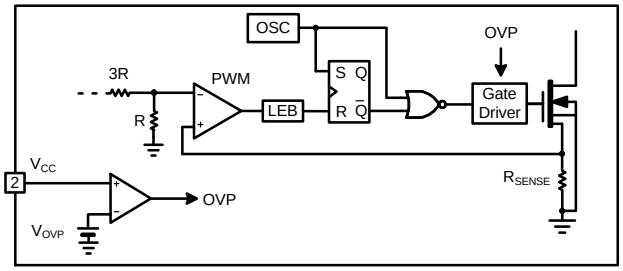


**Figure 23. Over−Voltage Protection Circuit**

*Feedback Open Loop Protection (FB_OLP)*

In the event of a feedback loop failure, especially a shorted lower−side resistor of the feedback pin; not only does $V_{COMP}$ rise in a similar manner to the overload situation, but $V_{FB}$ starts to drop to IC ground level. Although OLP and OVP also can protect the SMPS in this situation, FB_OLP can reduce stress on SENSEFET. If there is no FB_OLP, output voltage is much higher than the rated voltage before OLP or OVP triggers. When $V_{FB}$ drops below 0.5 V, FB_OLP is activated, switching off. To avoid undesired activation during startup, this function is disabled during soft−start time.

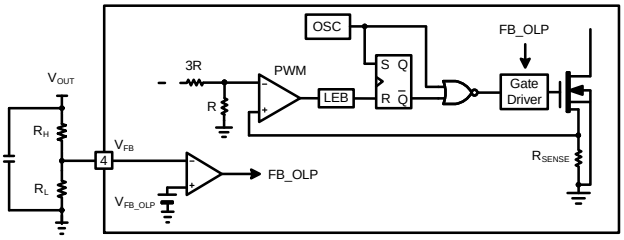


**Figure 24. Feedback Open−Loop Protection Circuit**

## Soft−Start

The internal soft−start circuit slowly increases the SENSEFET current after it starts. The typical soft−start time is 10 ms, as shown in Figure 25, where progressive increments of the SENSEFET current are allowed during startup. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is gradually increased to smoothly establish the required output voltage. Soft−start also helps to prevent transformer saturation and reduces stress on the secondary diode.

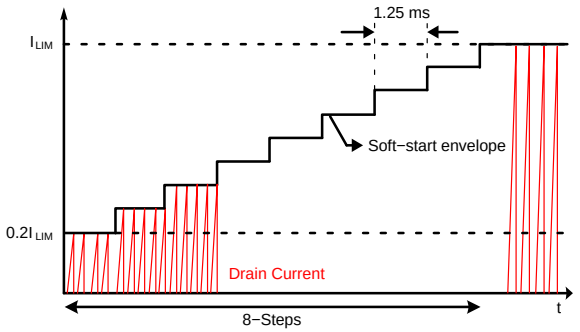


**Figure 25. Internal Soft−Start**

## Burst Mode Operation

To minimize power dissipation in Standby Mode, the FSL336LR enters Burst Mode. As the load decreases, the COMP pin voltage ($V_{COMP}$) decreases. As shown in Figure 26, the device automatically enters Burst Mode when the feedback voltage drops below $V_{BURL}$. At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes $V_{COMP}$ to rise. Once it passes $V_{BURH}$, switching resumes. $V_{COMP}$ then falls and the process repeats. Burst Mode alternately enables and disables switching of the SENSEFET and reduces switching loss in Standby Mode.

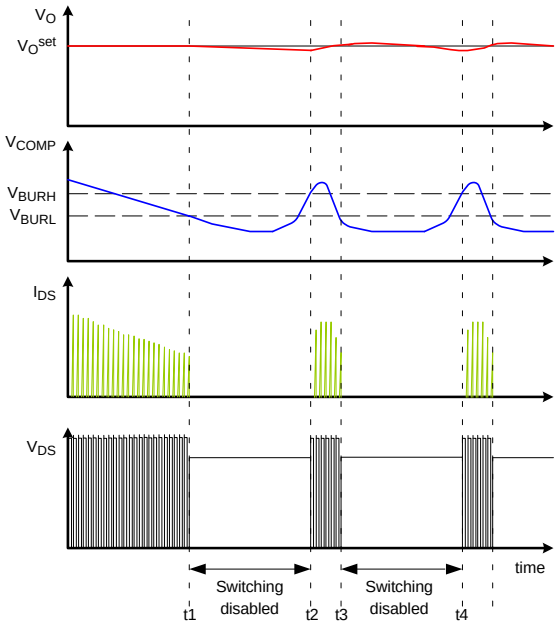


**Figure 26. Burst Mode Operation**

## Green Mode Operation

As output load condition is reduced, the switching loss becomes the largest power loss factor. FSL306LR uses the $V_{COMP}$ pin voltage to monitor output load condition. As output load decreases, $V_{COMP}$ decreases and switching frequency declines, as shown in Figure 27. Once $V_{COMP}$ falls to 0.8 V, the switching frequency varies between 21 kHz and 23 kHz before Burst Mode operation. At Burst Mode operation, random frequency fluctuation still functions.

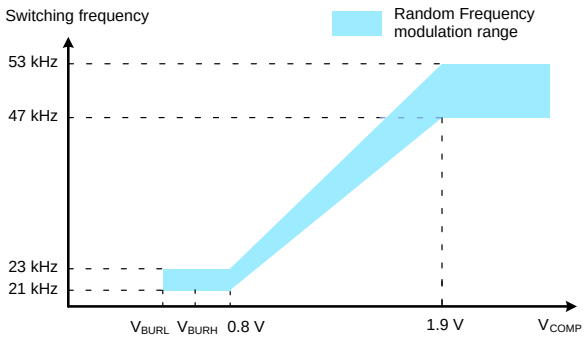


**Figure 27. Green Mode Operation**



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### Adjusting Current Limit

As shown in Figure 28, a combined 46 kΩ internal resistance (3R + R) is connected to the inverting lead on the PWM comparator. An external resistance of Rx on the $I_{LIMIT}$ pin forms a parallel resistance with the 46 kΩ when the internal diodes are biased by the main current source of 50 μA. For example, FSL336LR has a typical SENSEFET peak current limit of 1.8 A. Current limit can be adjusted to 1.2 A by inserting $R_X$ between the $I_{LIMIT}$ in and the ground. The value of the $R_X$ can be estimated by the following equation:

$$1.8\ A : 1.2\ A = (46\ k\Omega + R_x) : R_x \quad \text{(eq. 1)}$$

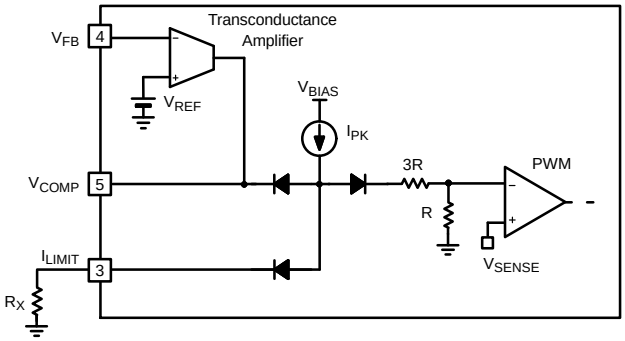


**Figure 28. Current Limit Adjustment**

## ORDERING INFORMATION

| Part Number | Operating Junction Temperature | PKG | Packing Method† | Typical Output Power (Note 8) | | | |
|---|---|---|---|---|---|---|---|
| | | | | Current Limit | $R_{DS(ON),MAX}$ | 85 $V_{AC}$~265 $V_{AC}$ & Open Frame (Note 9) | |
| | | | | | | Buck Application (Note 10) | Flyback Application |
| FSL336LRN | −40°C~125°C | 7−DIP | Rail | 1.8 A | 4 Ω | 9 W | 20 W |
| FSL336LRLX | | 7−LSOP | Tape & Reel | | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. The junction temperature can limit the maximum output power.
9. Maximum practical continuous power in an open−frame design at 50°C ambient.
10. Based on 15 V output voltage condition. Output voltage can limit the maximum output power.

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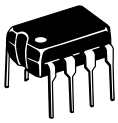

**PDIP−7 (PDIP−8 LESS PIN 6)**
CASE 626A
ISSUE C

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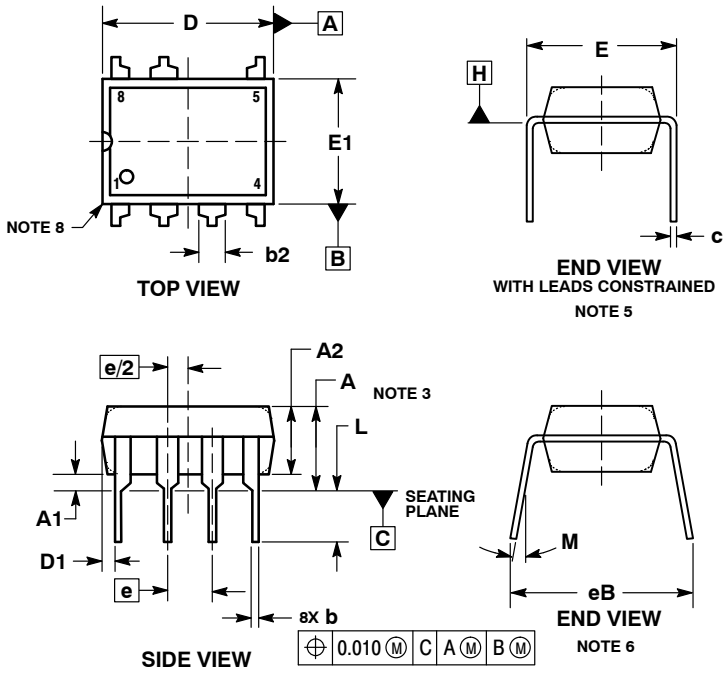


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2. CONTROLLING DIMENSION: INCHES.
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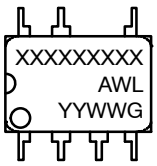
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | --- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.355 | 0.400 | 9.02 | 10.16 |
| D1 | 0.005 | ---- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | --- | 10° |

## GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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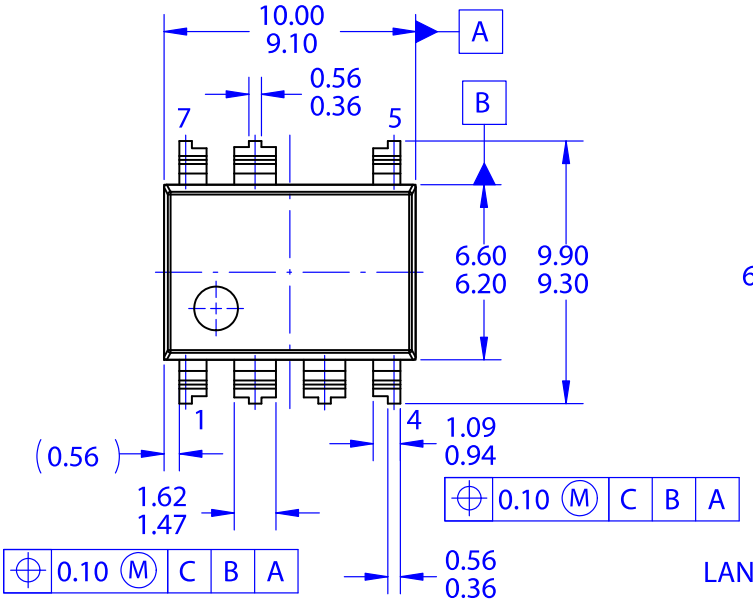


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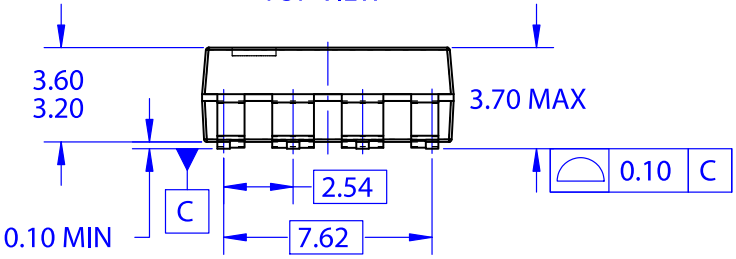


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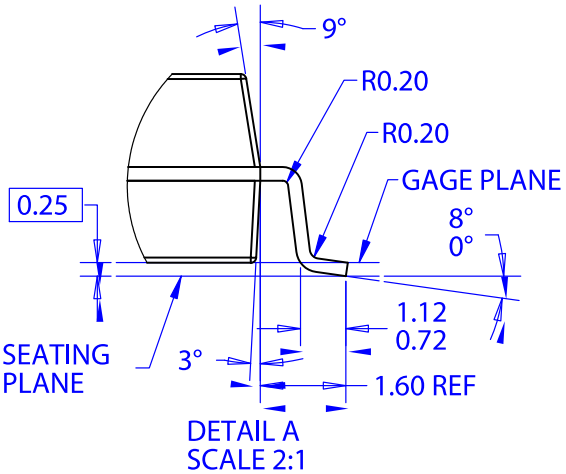


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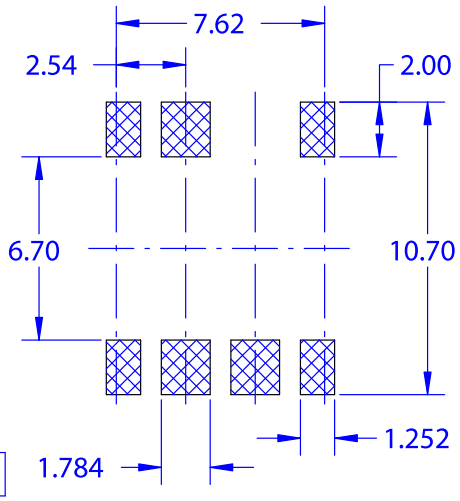


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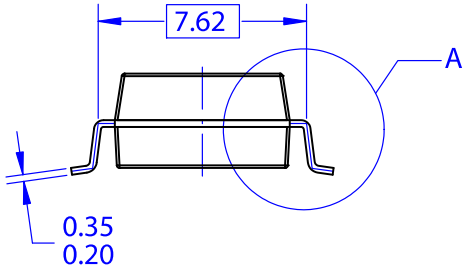


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