

Description

The ICS308 is a versatile serially programmable, quad PLL clock source. The ICS308 can generate any frequency from 250 kHz to 200 MHz, and up to 6 different output frequencies simultaneously. The outputs can be reprogrammed on the fly, and will lock to a new frequency in 10 ms or less. Smooth transitions (in which the clock duty cycle remains roughly 50%) are guaranteed if the output divider is not changed.

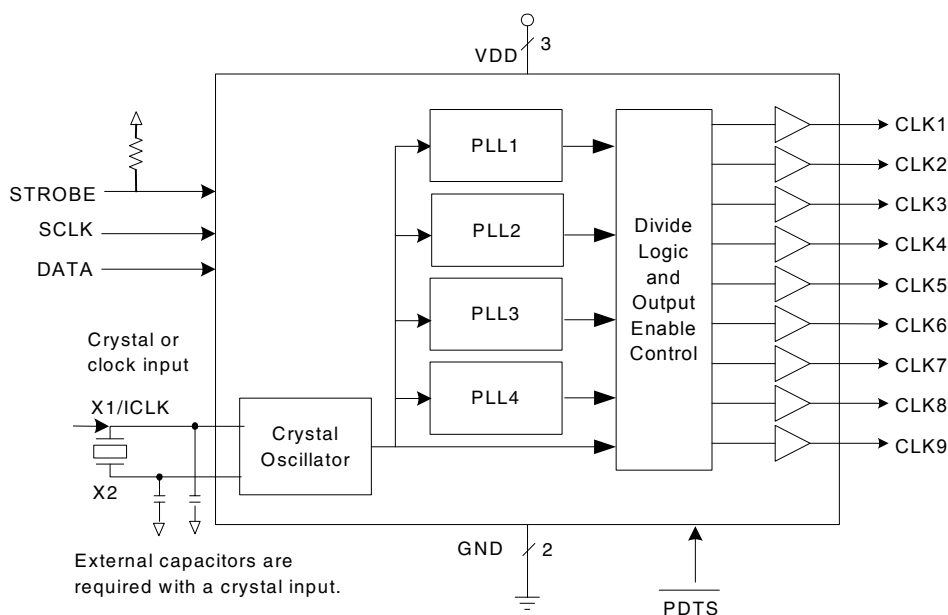
The device includes a $\overline{\text{PDT S}}$ pin which tri-states the output clocks and powers down the entire chip.

The ICS308 default for non-programmed start-up are buffered reference clock outputs on all clock output pins.

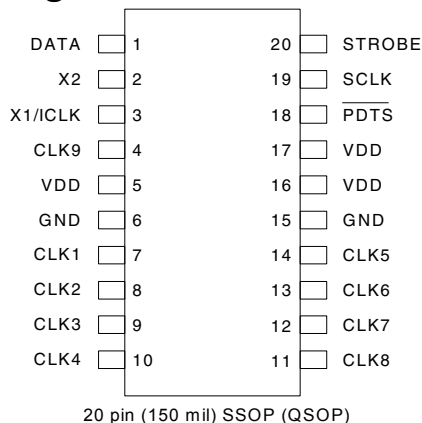
Features

- Packaged in 20-pin SSOP (QSOP) – Pb-free, RoHS compliant
- Operating voltage of 3.3 V
- Highly accurate frequency generation
 - M/N Multiplier PLL: $M = 1..2048$, $N = 1..1024$
- Serially programmable: user determines the output frequency via a 3-wire interface
- Eliminates need for custom quartz oscillators
- Input crystal frequency of 5 - 27 MHz
 - Optional programmable on-chip crystal capacitors
- Output clock frequencies up to 200 MHz
- Reference clock output
- Power down tri-state mode
- Very low jitter

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	DATA	Input	Serial data input.
2	X2	XO	Crystal Output. Connect this pin to a crystal. Float for clock input.
3	X1/ICLK	XI	Connect this pin to a crystal or external clock input.
4	CLK9	Output	Output clock 9. Default of Reference frequency output when unprogrammed.
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to Ground.
7	CLK1	Output	Output clock 1. Default of Reference frequency output when unprogrammed.
8	CLK2	Output	Output clock 2. Default of Reference frequency output when unprogrammed.
9	CLK3	Output	Output clock 3. Default of Reference frequency output when unprogrammed.
10	CLK4	Output	Output clock 4. Default of Reference frequency output when unprogrammed.
11	CLK8	Output	Output clock 8. Default of Reference frequency output when unprogrammed.
12	CLK7	Output	Output clock 7. Default of Reference frequency output when unprogrammed.
13	CLK6	Output	Output clock 6. Default of Reference frequency output when unprogrammed.
14	CLK5	Output	Output clock 5. Default of Reference frequency output when unprogrammed.
15	GND	Power	Connect to Ground.
16	VDD	Power	Connect to +3.3 V.
17	VDD	Power	Connect to +3.3 V.
18	PDS	Input	Powers down entire chip, tri-states all outputs when low. Internal pull-up.
19	SCLK	Input	Serial Shift register clock. See timing diagram.
20	STROBE	Input	Strobe to load data. See timing diagram. Use external 250 kOhm pull-up.

Configuring the ICS308

Initial State: The ICS308 may be configured to have up to nine frequency outputs, utilizing the four on-board PLLs. Unprogrammed, the part has the following outputs, related to the reference input clock:

Default Outputs	
Output	Frequency
Clock 1-9 (Pins 4, 10 - 14)	Reference Output

The STROBE pin must have an external 250 kOhm pull-up resistor to achieve the Initial State.

The input crystal range for the ICS308 is 5 MHz to 27 MHz.

The ICS308 can be programmed to set the output functions and frequencies. 160 data bits generated by the VersaClock™ software are written in DATA pin in this order: MSB (left most bit) first.

As show in Figure 2, after these 160 bits are clocked into the ICS308, taking STROBE high will send this data to the internal latch and the CLK output will lock within 10 ms.

Note: STROBE utilizes a transparent latch that is latched when in the high state. If STROBE is in the high state and SCLK is pulsed, DATA is clocked directly to the internal latch and the output conditions will change accordingly. Although this will not damage the ICS308, it is recommended that STROBE be kept low while DATA is being clocked into the ICS308 in order to avoid unintended changes on the output clocks.

All outputs may be turned off during initialization by bringing the $\overline{\text{PDTS}}$ pin to Ground. When $\overline{\text{PDTS}}$ is brought high, after the Strobe pin in brought high, the programmed output frequencies will be available.

AC Parameters for Writing to the ICS308

Parameter	Condition	Min.	Max.	Units
t_{SETUP}	Setup time	10		ns
t_{HOLD}	Hold time after SCLK	10		ns
t_w	Data wait time	10		ns
t_s	Strobe pulse width	40		ns
	SCLK Frequency		30	MHz

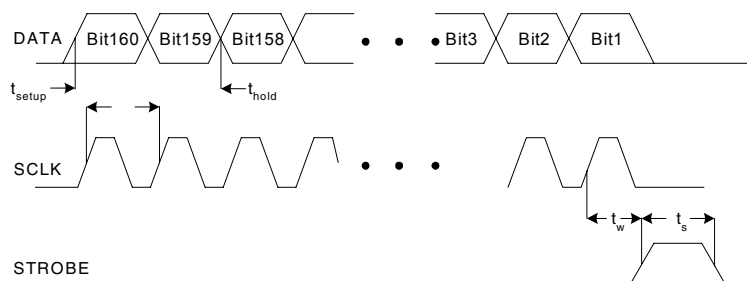


Figure 2. Timing Diagram for Programming the ICS308

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

STROBE Pull-up Resistor

In order for the device to start up in the default state, a 250 kΩ pull-up resistor is required.

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS308 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01μF must be connected between each VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 6 \text{ pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF $[(16 - 6) \times 2 = 20]$.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close

to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to each clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers.

ICS308 Configuration Capabilities

The architecture of the ICS308 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 2048 and N = 1 to 1024.

The ICS308 also provides separate output divide values, from 2 through 20, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$\text{Output Freq.} = (\text{Ref. Freq}) \times (\text{M/N}) / \text{Output Divide}$$

VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS308. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Item	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+ 0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (ICS308R)	0		+70	°C
Ambient Operating Temperature (ICS308RI)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

VDD=3.3 V \pm 10%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.00		3.60	V
Operating Supply Current	IDD	Configuration Dependent				mA
Input High Voltage		Ex. 25 MHz crystal, VDD=3.3 V, No load,		25		mA
		$\overline{\text{PDTS}} = 0$		20		μA
Input High Voltage	V _{IH}	X1/ICLK only	(VDD/2)+1			V
Input Low Voltage	V _{IL}	X1/ICLK only			(VDD/2)-1	V
Input High Voltage	V _{IH}		VDD-0.5			V
Input Low Voltage	V _{IL}	$\overline{\text{PDTS}}$, SRCLOCK, DATA, STROBE			0.8	V
Output High Voltage	V _{OH}	I _{OH} = -8 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 8 mA			0.4	V
Output High Voltage, CMOS level	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Short Circuit Current		CLK outputs		± 70		mA
Input Capacitance	C _{IN}	$\overline{\text{PDTS}}$ pin		4		pF
Internal Pull-down Resistor	R _{PD}	CLK outputs		525		k Ω
Internal Pull-up Resistor	R _{PU}	$\overline{\text{PDTS}}$ pin		250		k Ω

AC Electrical Characteristics

VDD = 3.3 V \pm 10%, Ambient Temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F _{IN}	Fundamental crystal	5		27	MHz
		Input Clock	2		50	MHz
Output Frequency		VDD=3.3 V	0.25		200	MHz
Output Clock Rise Time	t _{OR}	20% to 80%, Note 1		0.8		ns
Output Clock Fall Time	t _{OF}	80% to 20%, Note 1		0.8		ns
Output Clock Duty Cycle		Note 2	40	49-51	60	%
Power-up Time		STROBE goes high until stable CLK out		3	10	ms
		PDT \overline{S} goes high until stable CLK out		.2	2	ms
Maximum Output Jitter, short term	t _j	Reference Clock		\pm 300		ps
Maximum Output Jitter, short term	t _j	All other clocks, C _L =15 pF, configuration dependent		\pm 200		ps
Pin-to-Pin Skew		Low Skew Outputs	-250		250	ps

Note 1: Measured with 15 pF load.

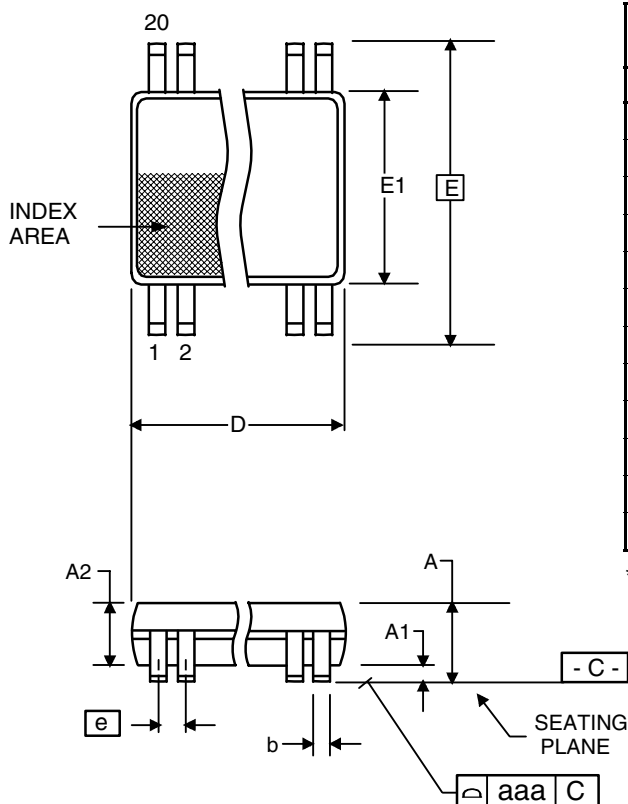
Note 2: Duty Cycle is configuration dependent. Most configurations are min 45% / max 55%

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

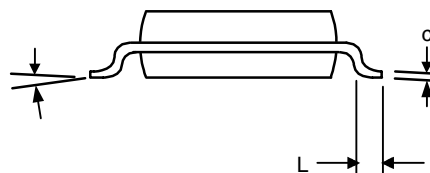
Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
308RLF	308RLF	Tubes	20-pin SSOP	0 to +70° C
308RLFT		Tape and Reel	20-pin SSOP	0 to +70° C
308RILF	308RILF	Tubes	20-pin SSOP	-40 to +85° C
308RILFT		Tape and Reel	20-pin SSOP	-40 to +85° C

“LF” suffix to the part number denotes Pb-Free configuration, RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

ICS308

SERIAL PROGRAMMABLE QUAD PLL VERSACLOCK SYNTHESIZER

SER PROG CLOCK SYNTHESIZER

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.