Datasheet

Serial EEPROM series Standard EEPROM

I²C BUS EEPROM (2-Wire)

BR24Sxxx-W

(8K 16K 32K 64K 128K 256K)

●General Description

BR24Sxxx–W is a serial EEPROM of I²C BUS interface method

●Features

- Completely conforming to the world standard I²C BUS.
  All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.7V to 5.5V single power source action most suitable for battery use
- FAST MODE 400kHz at 1.7V to 5.5V
- Page write mode useful for initial value write at factory shipment
- Highly reliable connection by Au pad and Au wire
- Auto erase and auto end function at data rewrite
- Low current consumption
  - At write operation (5V) : 0.5mA (Typ.)
  - At read operation (5V) : 0.2mA (Typ.)
  - At standby operation (5V) : 0.1μA (Typ.)
- Write mistake prevention function
  - Write (write protect) function added
  - Write mistake prevention function at low voltage
- Data rewrite up to 1,000,000 times
- Data kept for 40 years
- Noise filter built in SCL / SDA terminal
- Shipment data all address FFh

●Packages W(Typ.) x D(Typ.) x H(Max.)



SOP8
5.00mm x 6.20mm x 1.71mm



TSSOP-B8
3.00mm x 6.40mm x 1.20mm



SOP- J8
4.90mm x 6.00mm x 1.65mm



TSSOP-B8J
3.00mm x 4.90mm x 1.10mm



SSOP-B8
3.00mm x 6.40mm x 1.35mm



MSOP8
2.90mm x 4.00mm x 0.90mm



VSON008X2030
2.00mm x 3.00mm x 0.60mm

●Page write

Number of pages	16Byte	32Byte	64Byte
Product number	BR24S08-W BR24S16-W	BR24S32-W BR24S64-W	BR24S128-W BR24S256-W

●BR24Sxxx-W

Capacity	Bit format	Type	Power source voltage	SOP8	SOP-J8	SSOP-B8	TSSOP-B8	MSOP8	TSSOP-B8J	VSON008 X2030
8Kbit	1K×8	BR24S08-W	1.7V to 5.5V	●	●	●	●	●	●	●
16Kbit	2K×8	BR24S16-W	1.7V to 5.5V	●	●	●	●	●	●	●
32Kbit	4K×8	BR24S32-W	1.7V to 5.5V	●	●	●	●	●	●	●
64Kbit	8K×8	BR24S64-W	1.7V to 5.5V	●	●	●	●	●	●	
128Kbit	16K×8	BR24S128-W	1.7V to 5.5V	●	●	●	●			
256Kbit	32K×8	BR24S256-W	1.7V to 5.5V	●	●					

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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●**Absolute Maximum Ratings** (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	450 (SOP8)	mW	When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		450 (SOP-J8)		When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		300 (SSOP-B8)		When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
		330 (TSSOP-B8)		When using at Ta=25℃ or higher 3.3mW to be reduced per 1℃.
		310 (TSSOP-B8J)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		310 (MSOP8)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
		300 (VSON008X2030)		When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
Storage Temperature	Tstg	−65 to +125	℃	
Operating Temperature	Topr	−40 to +85	℃	
Terminal Voltage	-	-0.3 to Vcc+1.0	V	

●**Memory cell characteristics (Ta=25℃, Vcc=1.7V to 5.5V)**

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Number of data rewrite times *1	1,000,000	-	-	Times
Data hold years *1	40	-	-	Years

*1 Not 100% TESTED

●**Recommended Operating Ratings**

Parameter	Symbol	Ratings	Unit
Power source voltage	Vcc	1.7 to 5.5	V
Input voltage	V_{IN}	0 to Vcc	

●**Electrical Characteristics**

(Unless otherwise specified, Ta=-40℃ to +85℃, V_{CC}=1.7V to 5.5V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ.	Max.		
"H" Input Voltage1	VIH1	0.7Vcc	-	Vcc+1.0	V	
"L" Input Voltage1	VIL1	-0.3	-	0.3Vcc	V	
"L" Output Voltage1	VOL1	-	-	0.4	V	IOL=3.0mA , 2.5V≦Vcc≦5.5V (SDA)
"L" Output Voltage2	VOL2	-	-	0.2	V	IOL=0.7mA , 1.7V≦Vcc≦2.5V (SDA)
Input Leakage Current	ILI	-1	-	1	μA	VIN=0 to Vcc
Output Leakage Current	ILO	-1	-	1	μA	VOUT=0 to Vcc (SDA)
Current consumption at action	ICC1	-	-	2.0	mA	Vcc=5.5V , fSCL =400kHz, tWR=5ms Byte Write, Page Write BR24S08/16/32/64-W
		-	-	2.5		Vcc=5.5V , fSCL =400kHz, tWR=5ms Byte Write, Page Write BR24S128/256-W
	ICC2	-	-	0.5	mA	Vcc=5.5V , fSCL =400kHz Random read, Current read, Sequential read
Standby Current	ISB	-	-	2.0	μA	Vcc=5.5V , SDA・SCL=Vcc A0, A1, A2=GND, WP=GND

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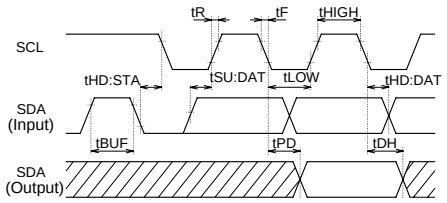
●Action timing characteristics

(Unless otherwise specified, Ta=-40℃ to +85℃, VCC=1.7V to 5.5V)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SCL Frequency	fSCL	-	-	400	kHz
Data clock "High" time	tHIGH	0.6	-	-	μs
Data clock "Low" time	tLOW	1.2	-	-	μs
SDA, SCL rise time *1	tR	-	-	0.3 *2	μs
SDA, SCL fall time *1	tF	-	-	0.3	μs
Start condition hold time	tHD:STA	0.6	-	-	μs
Start condition setup time	tSU:STA	0.6	-	-	μs
Input data hold time	tHD:DAT	0	-	-	ns
Input data setup time	tSU:DAT	100	-	-	ns
Output data delay time	tPD	0.1	-	0.9	μs
Output data hold time	tDH	0.1	-	-	μs
Stop condition data setup time	tSU:STO	0.6	-	-	μs
Bus release time before transfer start	tBUF	1.2	-	-	μs
Internal write cycle time	tWR	-	-	5	ms
Noise removal valid period (SDA,SCL terminal)	tI	-	-	0.1	μs
WP hold time	tHD:WP	0	-	-	ns
WP setup time	tSU:WP	0.1	-	-	μs
WP valid time	tHIGH:WP	1.0	-	-	μs

*1 : Not 100% TESTED
*2 : BR24S16/64-W : 1.0μs.

●Sync data input / output timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Figure 1-(a) Sync data input / output timing

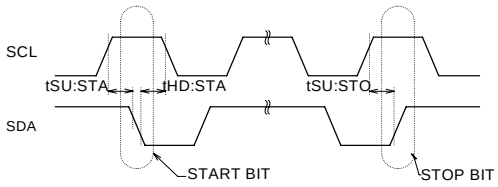


Figure 1-(b) Start - stop bit timing

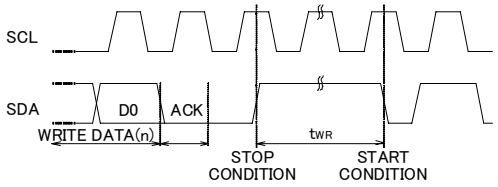


Figure 1-(c) Write cycle timing

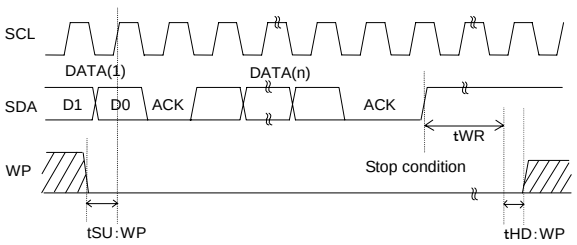
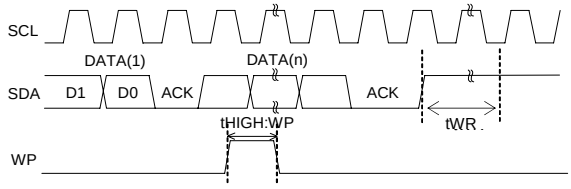


Figure 1-(d) WP timing at write execution



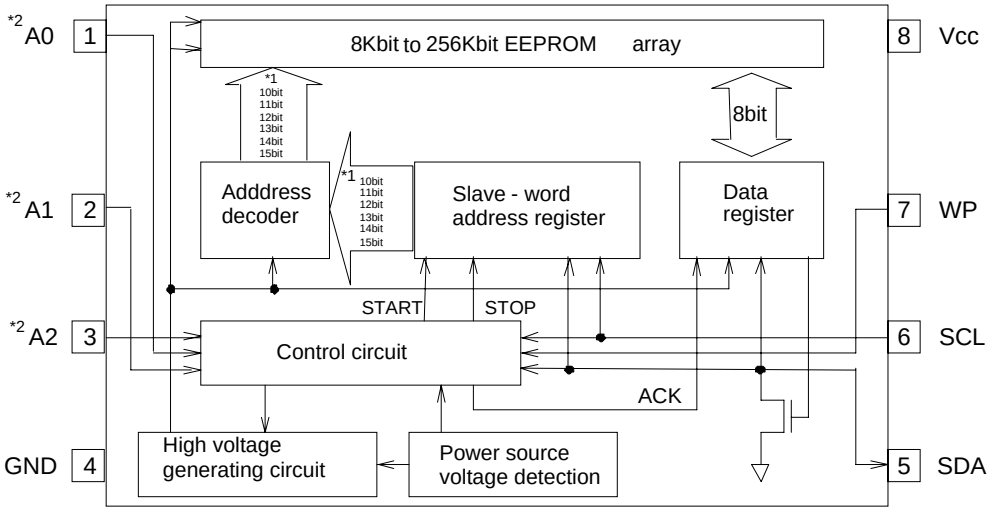
○At write execution, in the area from the D0 taken clock rise of the first DATA(1), to tWR, set WP= 'LOW'.
○By setting WP "HIGH" in the area, write can be cancelled.
When it is set WP = 'HIGH' during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Figure 1-(e) WP timing at write cancel

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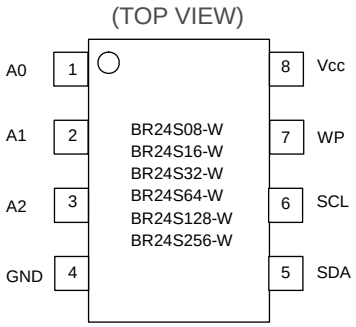
●Block Diagram



*1 10bit: BR24S08-W
11bit: BR24S16-W
12bit: BR24S32-W
13bit: BR24S64-W
14bit: BR24S128-W
15bit: BR24S256-W

*2 A0, A1=Don't use: BR24S08-W
A0, A1, A2=Don't use: BR24S16-W

●Pin Configuration



●Pin Descriptions

Terminal name	Input/ Output	Function		
		BR24S08-W	BR24S16-W	BR24S32/64/128/256-W
A0	Input	Don't use	Don't use	Slave address setting
A1	Input	Don't use	Don't use	Slave address setting
A2	Input	Slave address setting	Don't use	Slave address setting
GND	-	Reference voltage of all input / output, 0V.		
SDA	Input / Output	Slave and word address, Serial data input serial data output		
SCL	Input	Serial clock input		
WP	Input	Write protect terminal		
Vcc	-	Connect the power source.		

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●**Typical Performance Curves**
(The following values are Typ. ones.)

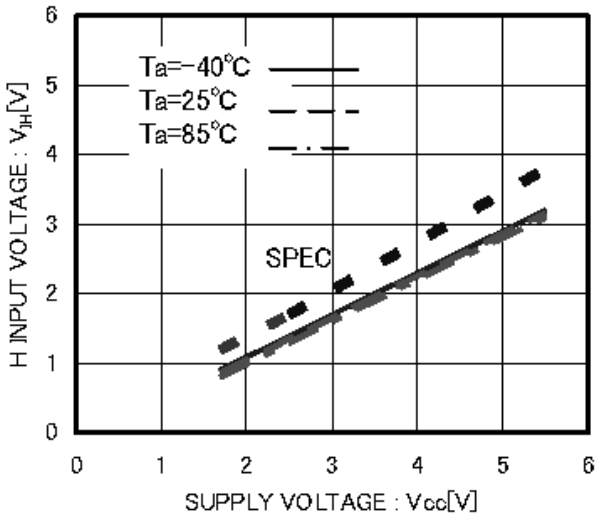


Figure 2. "H" Input Voltage VIH
(A0, A1, A2, SCL, SDA, WP)

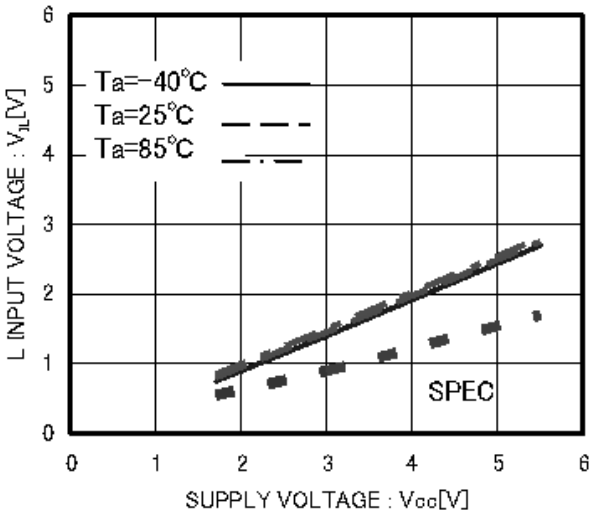


Figure 3. "L" Input Voltage VIL
(A0, A1, A2, SCL, SDA, WP)

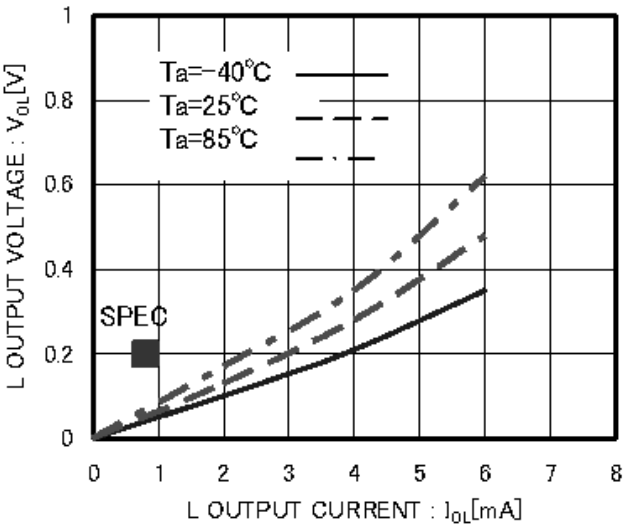


Figure 4. "L" Output Voltage
VOL-IOL1(Vcc=1.7V)

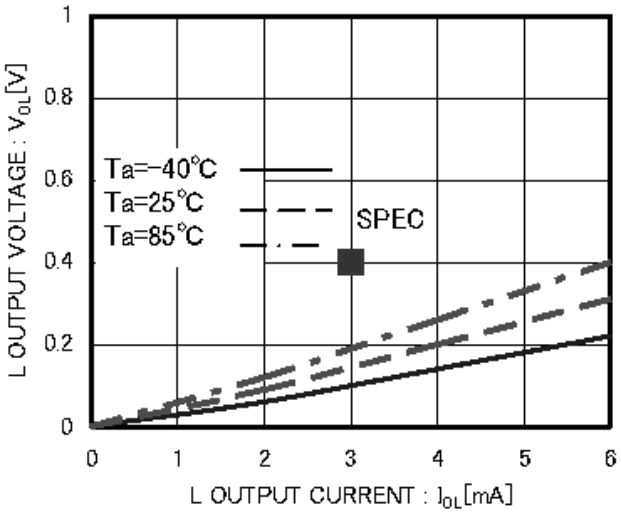


Figure 5. "L" Output Voltage VOL-IOL
(Vcc=2.5V)

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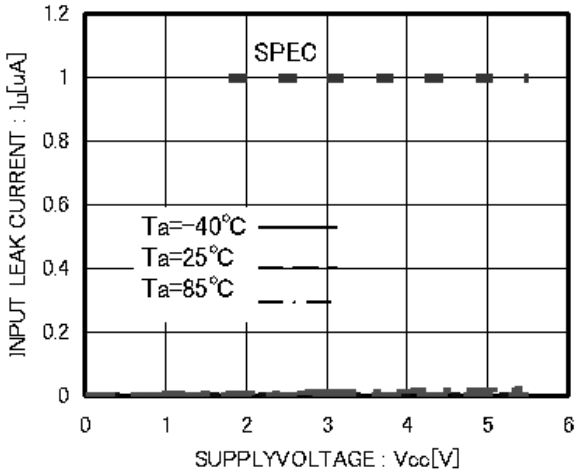


Figure 6. Input Leak Current ILI
(A0, A1, A2, SCL, WP)

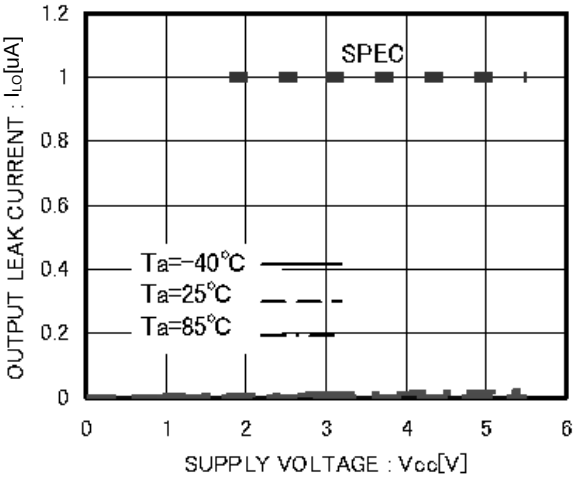


Figure 7. Output Leak Current ILO (SDA)

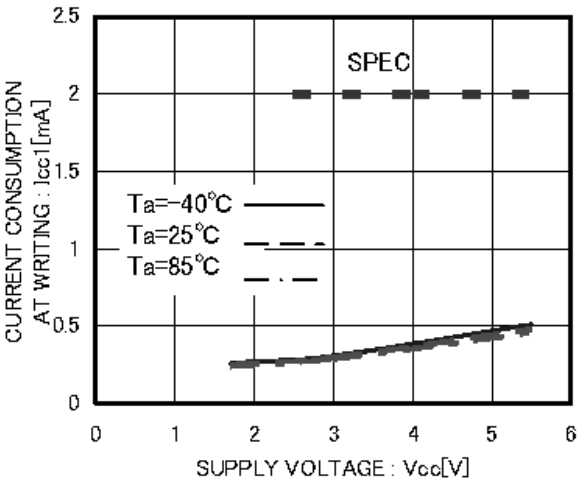


Figure 8. Current consumption at WRITE operation
ICC1
(fscl=400kHz BR24S16/32/64-W)

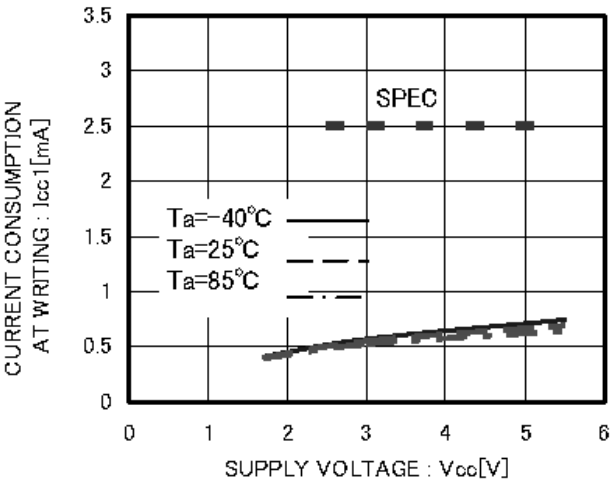


Figure 9. Current consumption at WRITE operation
ICC1
(fscl=400kHz BR24S128/256-W)

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●**Typical Performance Curves - Continued**

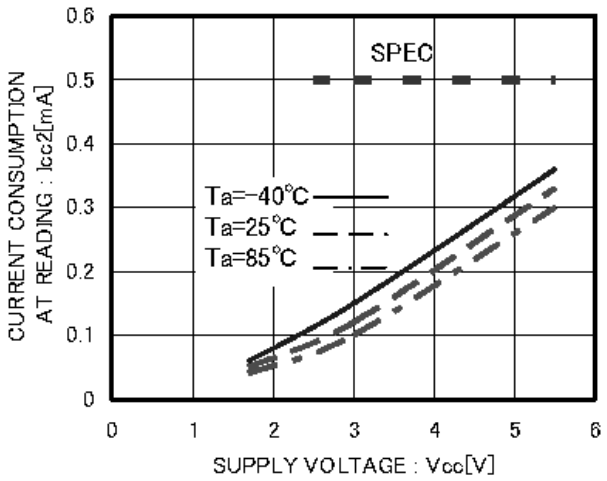


Figure 10. Current consumption at READ operation ICC2 (fscl=400kHz)

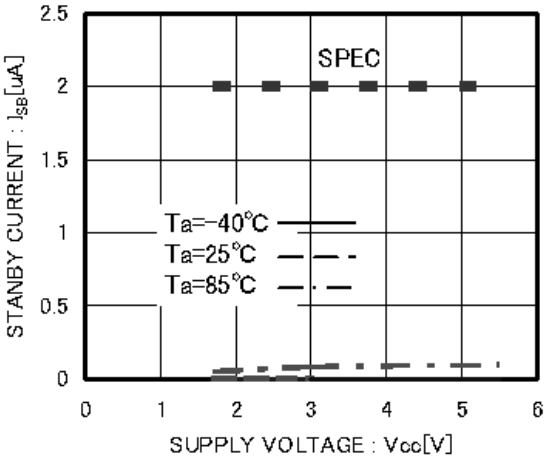


Figure 11. Standby operation I_{SB}

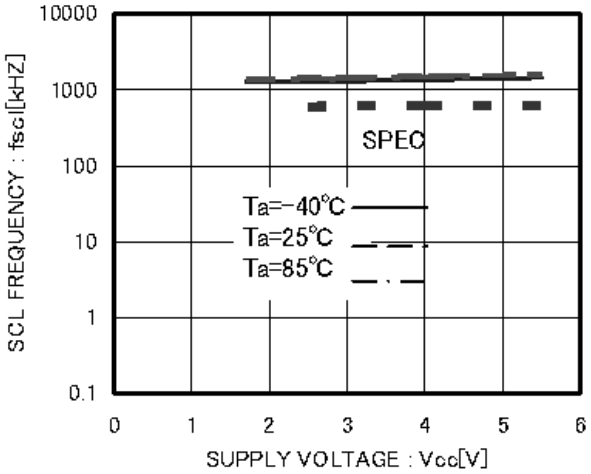


Figure 12. SCL frequency fSCL

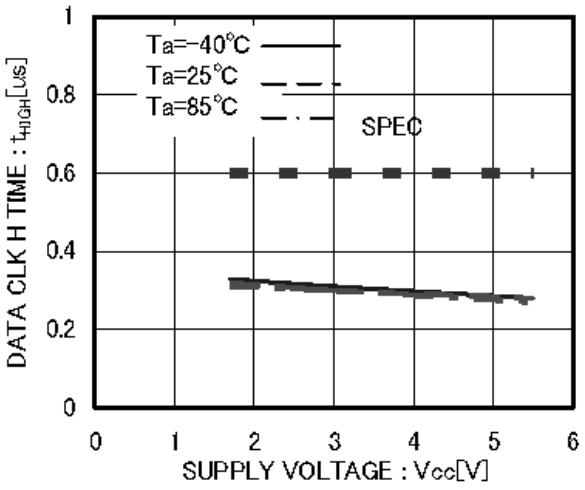


Figure 13. Data clock High Period tHIGH

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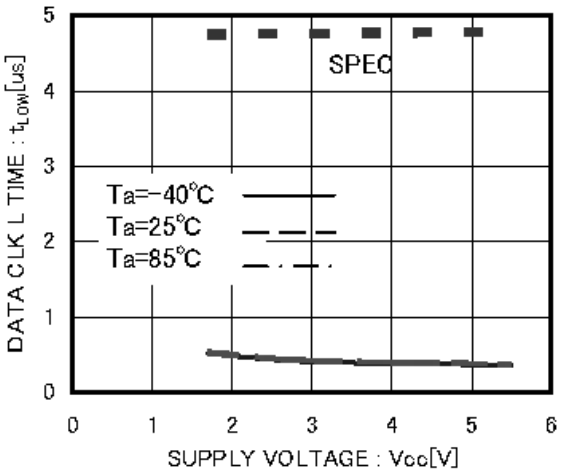


Figure 14. Data clock LOW Period tLOW

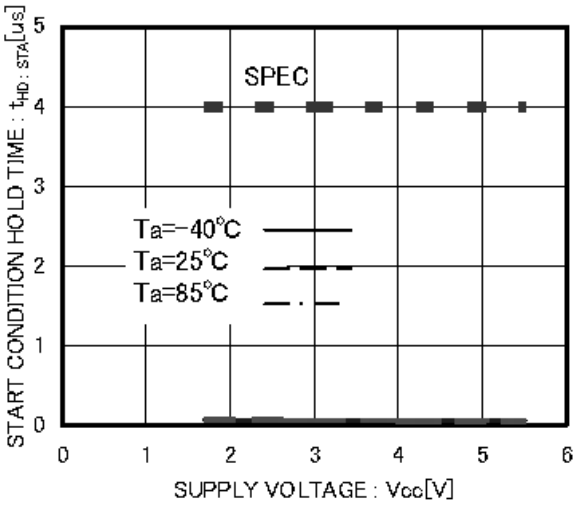


Figure 15. Start Condition Hold Time tHD:STA

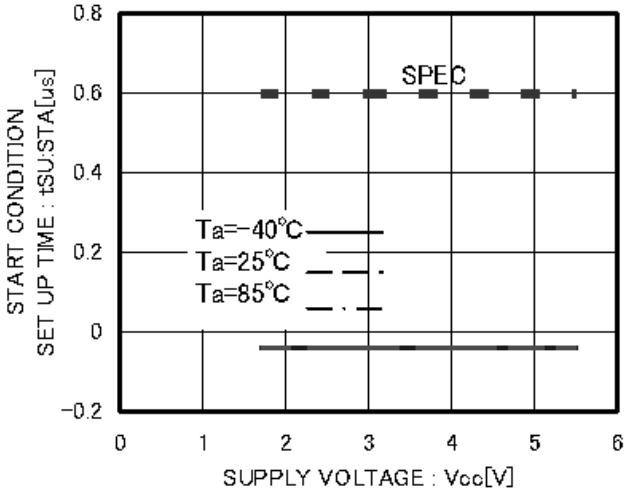


Figure 16. Start Condition Setup Time tSU:STA

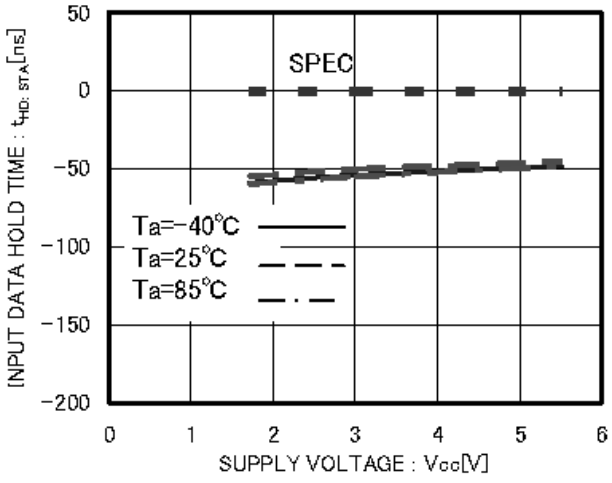


Figure 17. Input Data Hold Time tHD:DAT(HIGH)

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●**Typical Performance Curves - Continued**

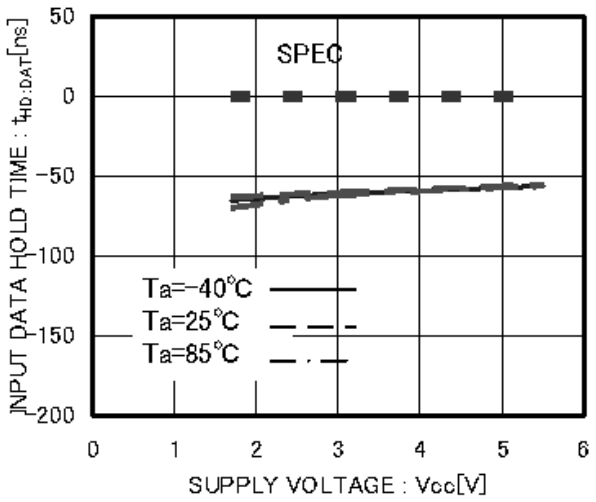


Figure 18. Input Data Hold Time tHD:DAT(LOW)

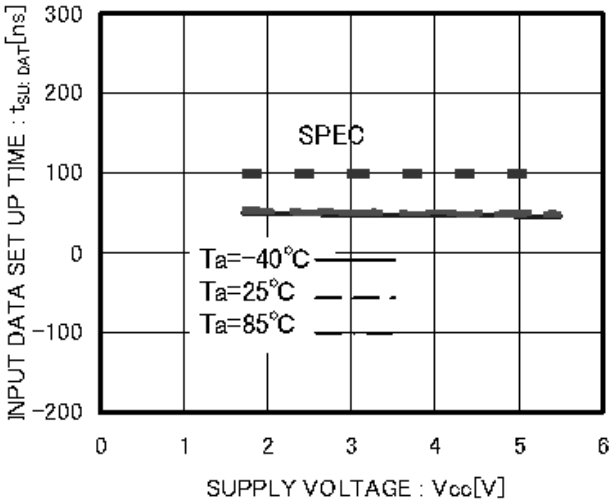


Figure 19. Input Data Setup Time tSU:DAT(HIGH)

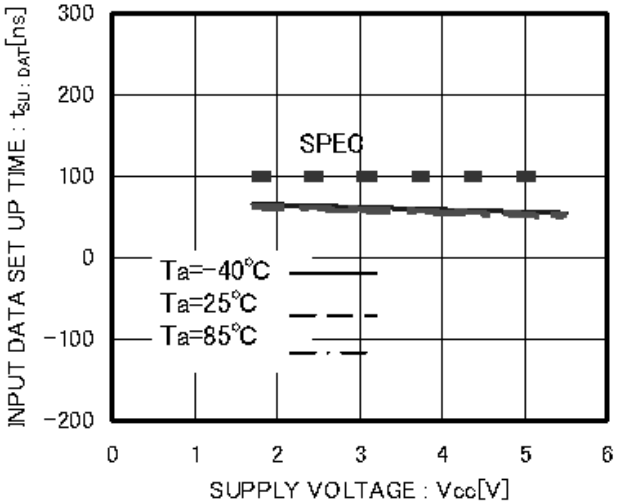


Figure 20. Input Data Setup Time tSU:DAT(LOW)

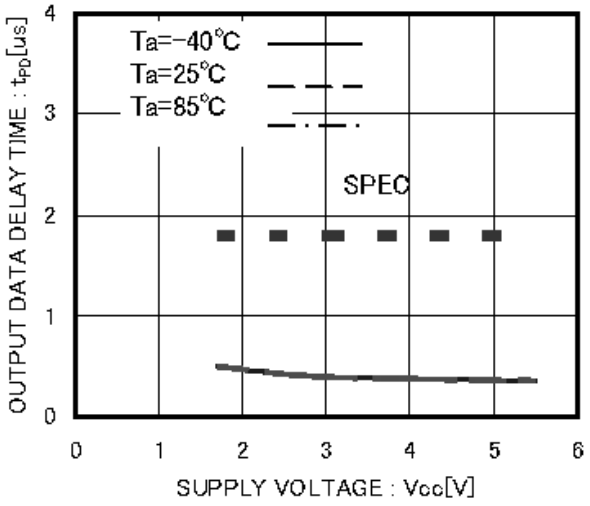


Figure 21. “L” Data output delay time tPD0

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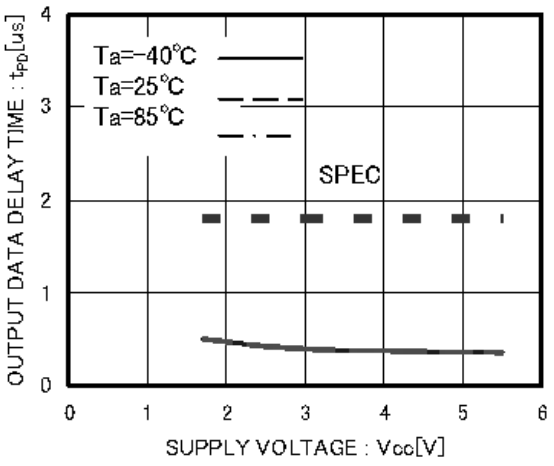


Figure 22. “H” Data output delay time tPD1

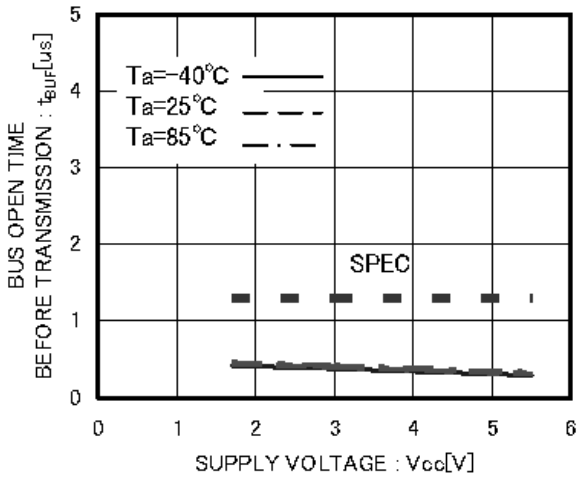


Figure 23. BUS open time before transmission tBUF

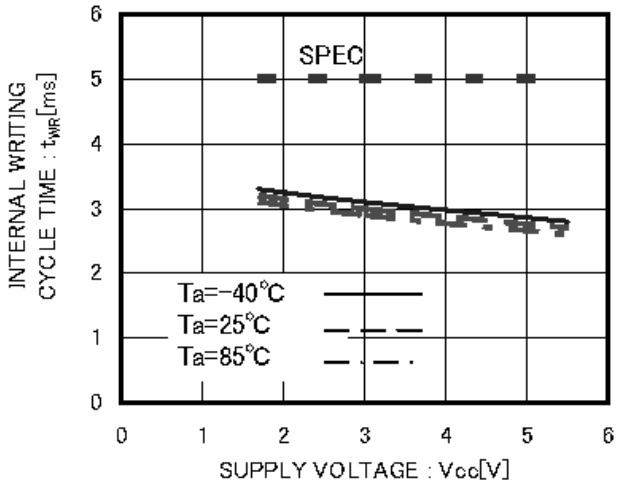


Figure 24. Internal writing cycle time tWR

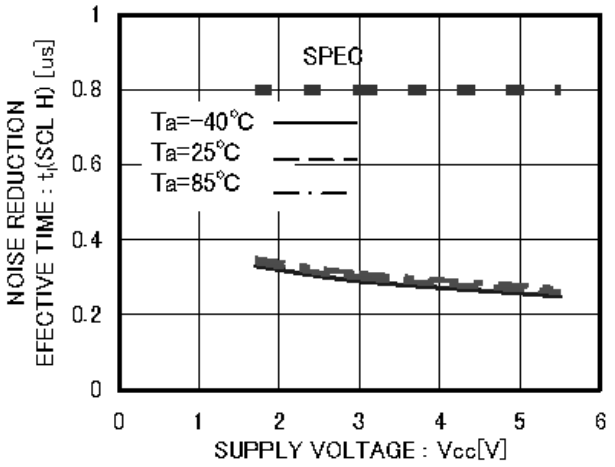


Figure 25. Noise reduction affection time tI(SCL H)

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●**Typical Performance Curves - Continued**

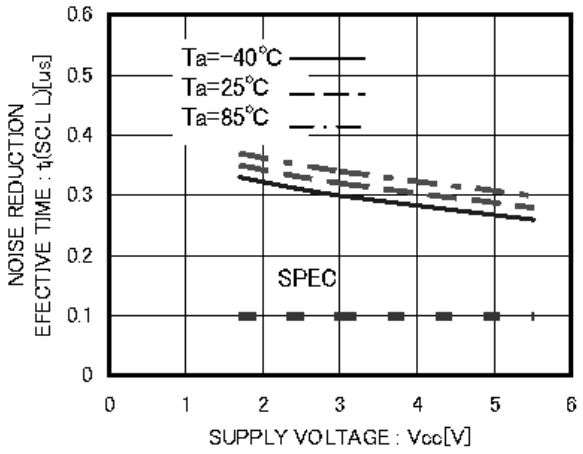


Figure 26. Noise reduction effective time tI(SCL L)

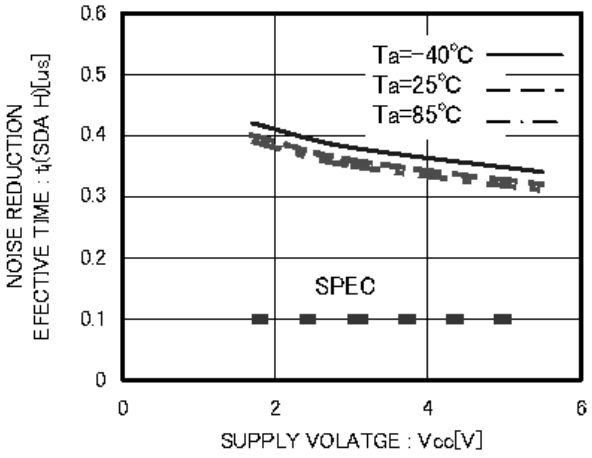


Figure 27. Noise reduction effective time tI(SDA H)

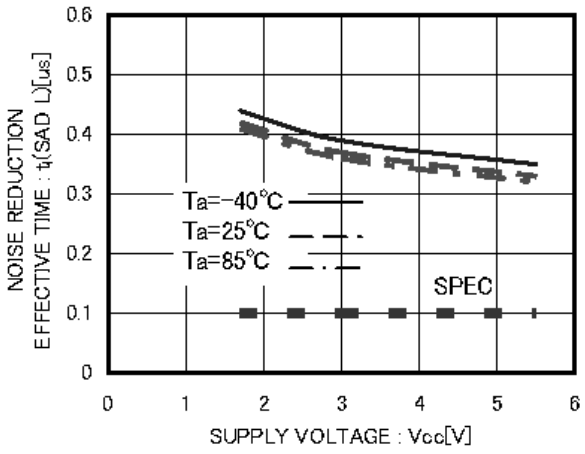


Figure 28. Noise reduction effective time tI (SDA L)

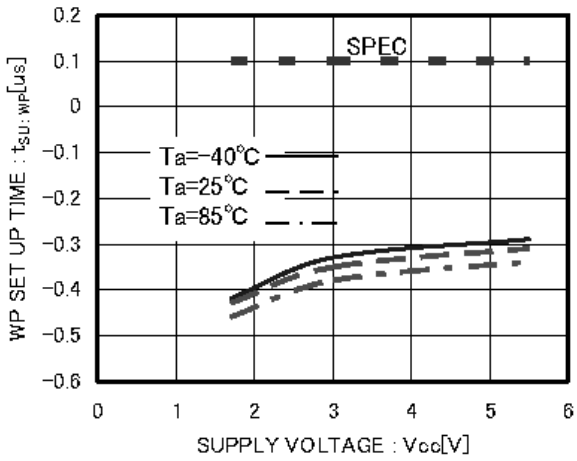


Figure 29. WP setup time tSU:WP

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●**Typical Performance Curves - Continued**

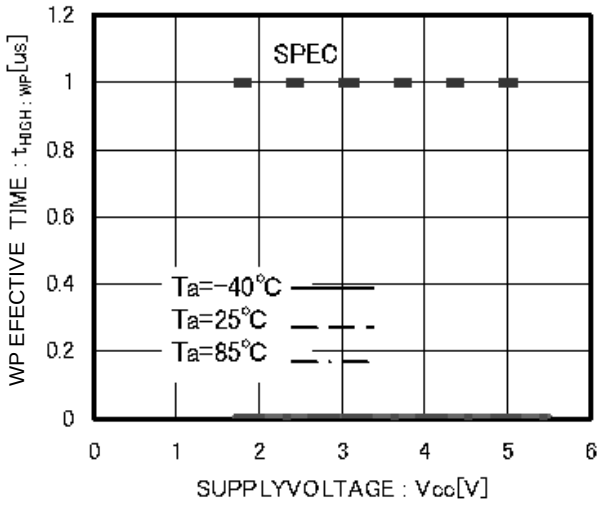


Figure 30. WP effective time tHIGH:WP

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●I²C BUS Communication

○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte.
I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).
Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by addresses peculiar to devices.
EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

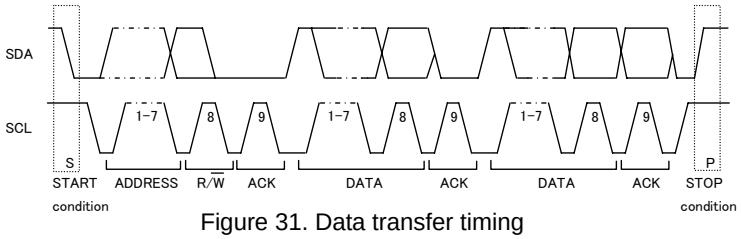


Figure 31. Data transfer timing

○Start condition (start bit recognition)

・Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
・This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command is executed.

○Stop condition (stop bit recognition)

・Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

○Acknowledge (ACK) signal

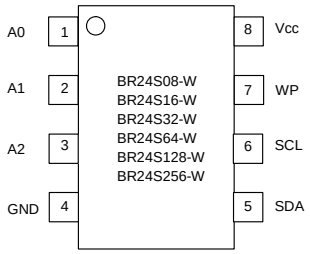
・This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
・The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
・This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
・Each write action outputs acknowledge signal) (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
・Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'.
・When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action. And this IC gets in standby status.

○Device addressing

・Output slave address after start condition from master.
・The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
・Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
・The most insignificant bit (R/$\overline{W}$ --- READ/$\overline{WRITE}$) of slave address is used for designating write or read action, and is as shown below.

Setting R/$\overline{W}$ to 0 --- write (setting 0 to word address setting of random read)
Setting R/$\overline{W}$ to 1 --- read

Type	Slave address								Maximum number of connected buses
BR24S08-W	1	0	1	0	A2	P1	P0	R/$\overline{W}$	2
BR24S16-W	1	0	1	0	P2	P1	P0	R/$\overline{W}$	1
BR24S32-W, BR24S64-W BR24S128-W, BR24S256-W	1	0	1	0	A2	A1	A0	R/$\overline{W}$	8



P0 to P2 are page select bits.
Note) Up to 2 units of BR24S08-W, up to 1 units of BR24S16-W, and up to 8 units of BR24S32/64/128/256-W can be connected.
Device address is set by 'H' and 'L' of each pin of A0, A1, and A2.

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●Write Command

○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity.
Up to 64 arbitrary bytes can be written. (In the case of BR24S128/256-W)

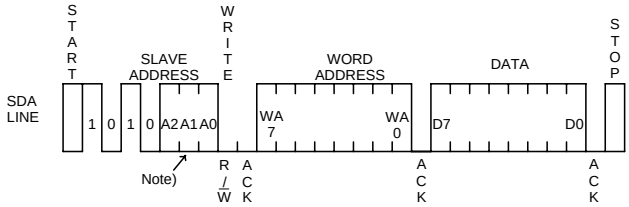
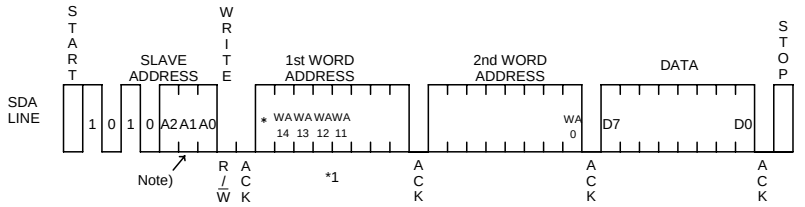


Figure 32. Byte write cycle (BR24S08/16-W)



*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

Figure 33. Byte write cycle (BR24S32/64/128/256-W)

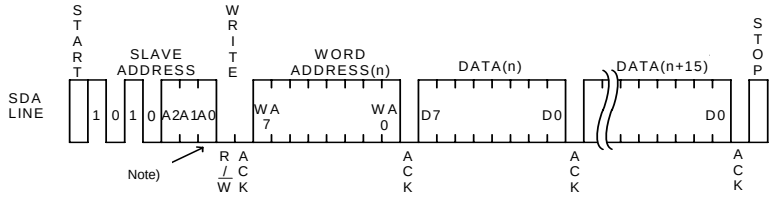
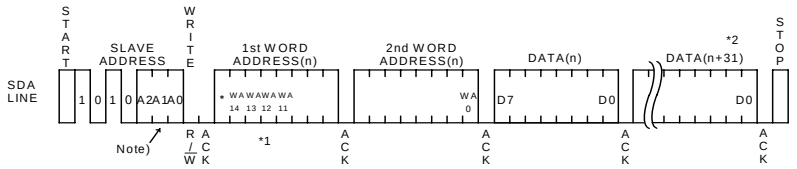


Figure 34. Page write cycle (BR24S08/16-W)



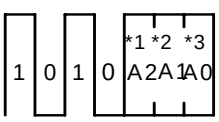
*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

*2 As for BR24S128/256-W becomes (n+63).

Figure 35. Page write cycle (BR24S32/64/128/256-W)

・Data is written to the address designated by word address (n-th address).
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk: Up to 16 bytes (BR24S08-W, BR24S16-W)
: Up to 32 bytes (BR24S32-W, BR24S64-W)
: Up to 64 bytes (BR24S128-W, BR24S256-W)
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment in Page 15.)
・As for page write command of BR24S08-W and, BR24S16-W, after page select bit(PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits is incremented internally, and data up to 16 bytes can be written.
・As for page write cycle of BR24S32-W and BR24S64-W , after the significant 7 bits (in the case of BR24S32-W) of word address, or the significant 8 bits (in the case of BR24S64-W) of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 5 bits is incremented internally, and data up to 32 bytes can be written.
・As for page write cycle of BR24S128-W and BR24S256-W, after the significant 9 bit (in the case of BR24S128-W) of word address, or the significant 10bit (in the case of BR24S256-W) of word address are designated arbitrarily, by continuing data input of 64 bytes or more.

Note)



*1 In BR24S16-W, A2 becomes P2
*2 In BR24S08/16-W, A1 becomes P1
*3 In BR24S08/16-W, A0 becomes P0

Figure 36. Difference of slave address each type

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○Notes on write cycle continuous input

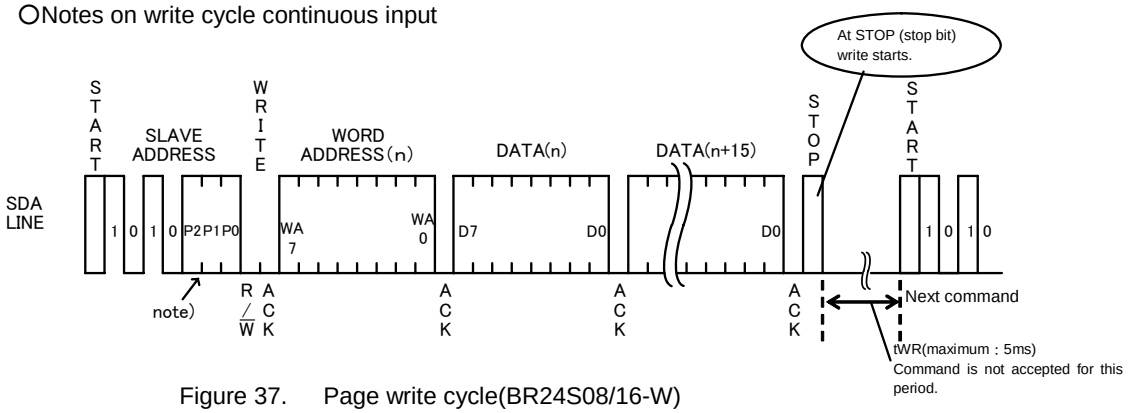
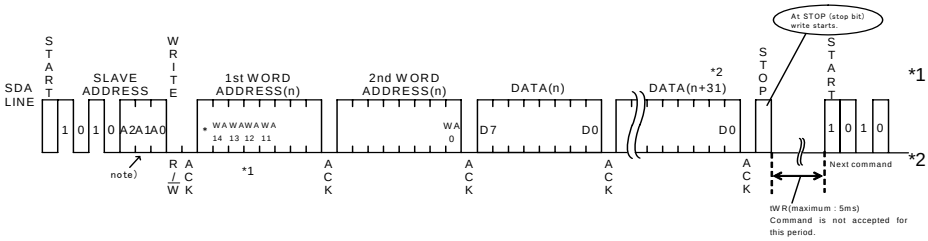


Figure 37. Page write cycle(BR24S08/16-W)



*1 As for WA12, BR24S32-W becomes Don't care.
As for WA13, BR24S32/64-W becomes Don't care.
As for WA14, BR24S32/64/128-W becomes Don't care.

*2 As for BR24S128/256-W becomes (n+63).

Figure 38. Page write cycle(BR24S32/64/128/256-W)

○Notes on page write cycle

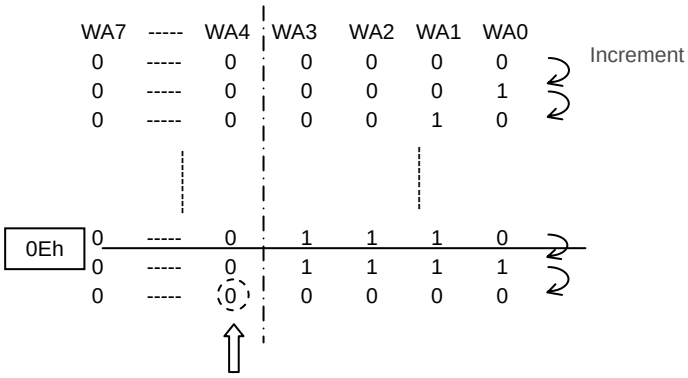
List of numbers of page write

Number of pages	16Byte	32Byte	64Byte
Product number	BR24S08-W BR24S16-W	BR24S32-W BR24S64-W	BR24S128-W BR24S256-W

The above numbers are maximum bytes for respective types. Any bytes below these can be written.
In the case of BR24S256-W, 1 page = 64bytes, but the page write cycle write time is 5ms at maximum for 64byte bulk write.
It does not stand 5ms at maximum × 64byte = 320ms(Max.).

○Internal address increment

Page write mode (in the case of BR24S16-W)



Significant bit is fixed.
No digit up

For example, when it is started from address 0Eh, therefore, increment is made as below,
0Eh→0Fh→00h→01h・・・, which please note.

* 0Eh・・・16 in hexadecimal, therefore, 00001110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all address is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.
At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', mistake write can be prevented.
During tWR, set the WP terminal always to 'L'. If it is set 'H', write is forcibly terminated.

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●Read Command

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

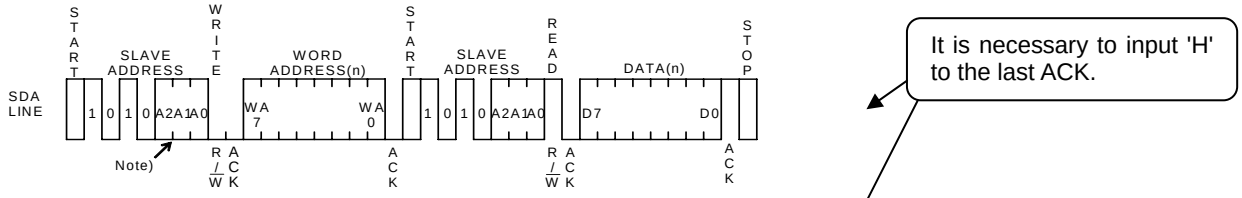


Figure 39. Random read cycle (BR24S08/16-W)

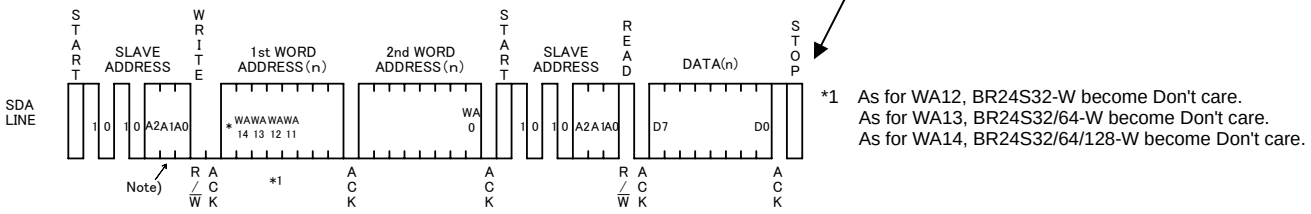


Figure 40. Random read cycle (BR24S32/64/128/256-W)

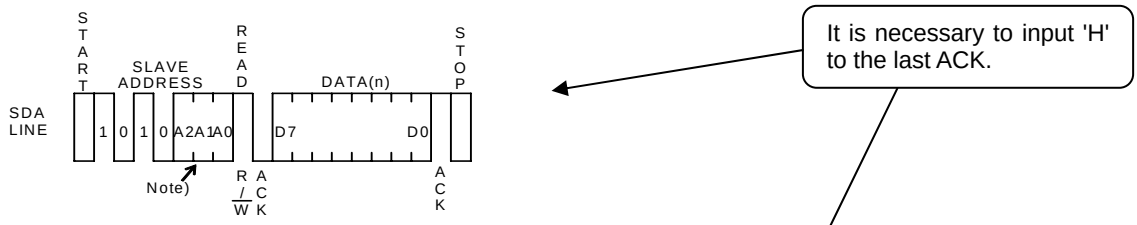


Figure 41. Current read cycle

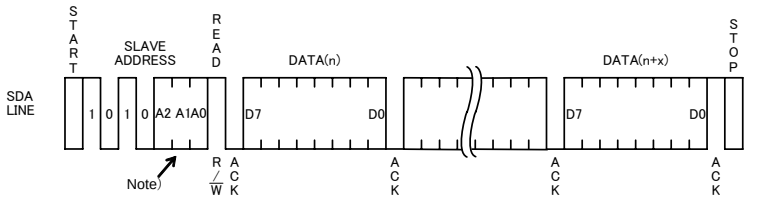
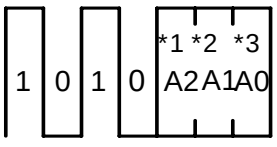


Figure 42. Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H'.
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

Note)



*1 BR24S16-W A2 becomes P2.
*2 BR24S08/16-W A1 becomes P1.
*3 BR24S08/16-W A0 becomes P0.

Figure 43. Difference of slave address of each type

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●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kids of them are shown in the figure below. (Refer to Figure 44(a), Figure 44 (b), Figure 44 (c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

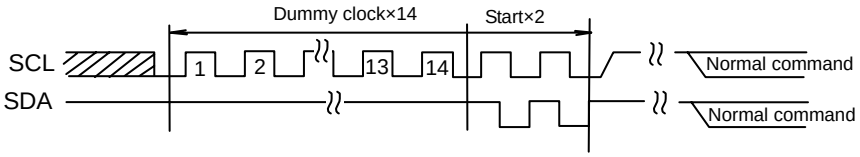


Figure 44-(a) The case of 14 Dummy clock + START + START+ command input

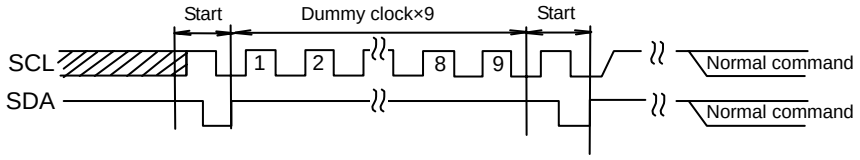
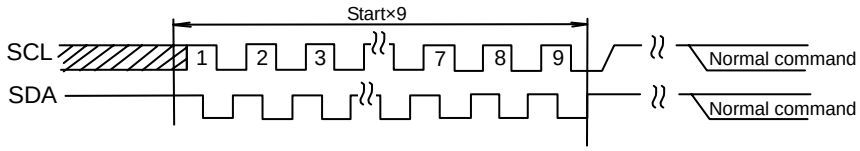


Figure 44-(b) The case of START+9 Dummy clock + START + command



* Start command from START input.

Figure 44-(c) START × 9 + command input

●Acknowledge polling

During internal write, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, R/$\overline{W}$ = 0, when to carry out current read cycle after write, slave address R/$\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data so forth.

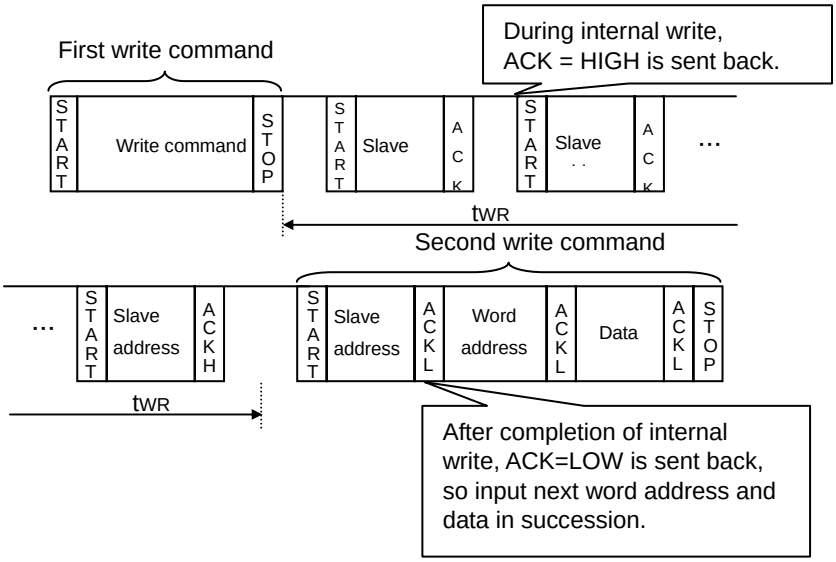


Figure 45. Case to continuously write by acknowledge polling

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●WP valid timing (write cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.
WP input in this area becomes Don't care. Set the setup time to rise of D0 taken 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP='H' during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again.(Refer to Figure 46.)
After execution of forced end by WP standby status gets in, so there is no need to wait for tWR (5ms at maximum).

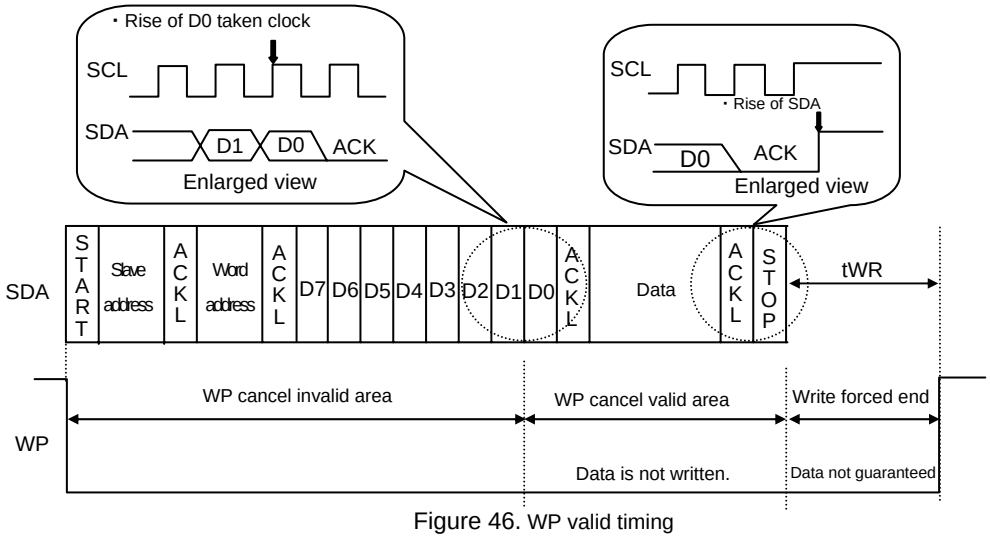


Figure 46. WP valid timing

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled.
(Refer to Figure 47.)
However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

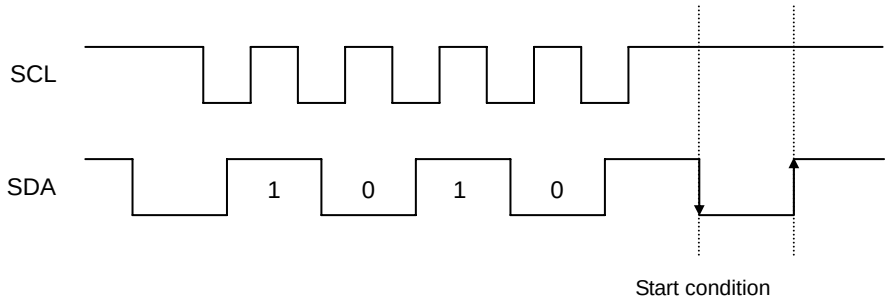


Figure 47. Case of cancel by start, stop condition during slave address input

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●I/O peripheral circuit

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus output of 'H' to SDA bus and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$Vcc - I_L R_{PU} - 0.2Vcc \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8Vcc - V_{IH}}{I_L}$$

Ex.) When Vcc = 3V, I_L=10μA, V_{IH} = 0.7Vcc

from(2)

$$R_{PU} \leqq \frac{0.8\times 3 - 0.7\times 3}{10\times 10^{-6}}$$

$$\leqq 30 \ [k\Omega]$$

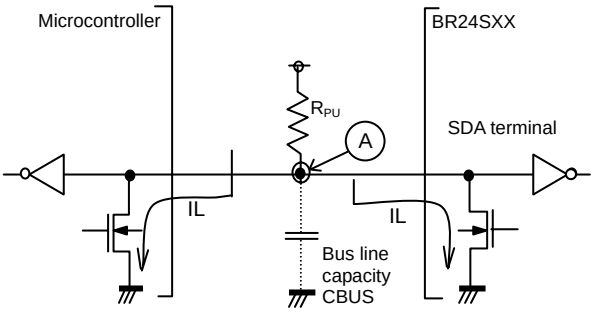


Figure 48. I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{Vcc - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{Vcc - V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$$V_{OLMAX} \leqq V_{IL} - 0.1\ Vcc$$

Ex.) When Vcc= 3V, V_{OL}0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

from(1),

$$R_{PU} \geqq \frac{3-0.4}{3\times 10}$$

$$\geqq 867 \quad [\Omega]$$

And

V_{OL}=0.4 [V]

V_{IL}=0.3×3

=0.9 [V]

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

●A0, A1, A2, WP process

○Process of device address terminals (A0,A1,A2)

Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up or pull down, or Vcc or GND. And, pins (Don't use PIN) not used as device address may be set to any of 'H', 'L', and 'Hi-Z'.

Types with Don't use PIN	BR24S08F/FJ/FV/FVT/FVM/FVJ/NUX-W	A0, A1
	BR24S16F/FJ/FV/FVT/FVM/FVJ/NUX-W	A0, A1, A2

○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In 'H' status, only READ is available and WRITE of all address is prohibited. In the case of 'L', both are available. In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

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●Cautions on microcontroller connection

○Rs

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

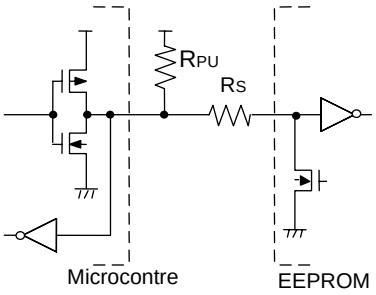
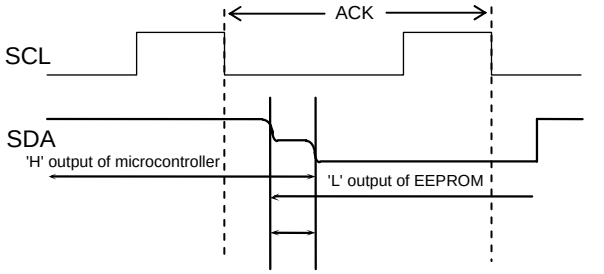


Figure 49. I/O circuit



Over current flows to SDA line by 'H' output of microcontroller and 'L' output of EEPROM.

Figure 50. Input/output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by following relations.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA shoulder be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1Vcc.

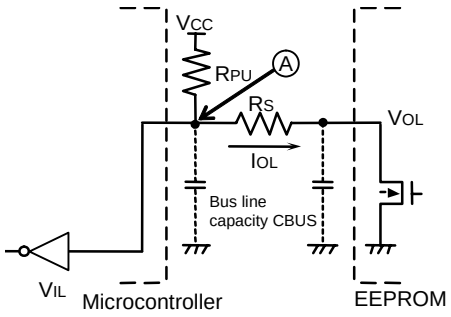


Figure 51. I/O circuit

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ

$$\text{from(2)}, \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67\ [k\Omega]$$

○Maximum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

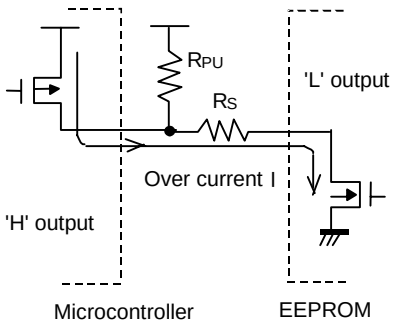


Figure 52. I/O circuit diagram

$$\frac{V_{CC}}{RS} \leqq I$$

$$\therefore \quad RS \geqq \frac{V_{CC}}{I}$$

Example) When V_{CC}=3V, I=10mA

$$RS \geqq \frac{3}{10\times10\text{-}3}$$

$$\geqq 300[\Omega]$$

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●I²C BUS input / output circuit

○Input (A0, A1, A2, SCL, WP)

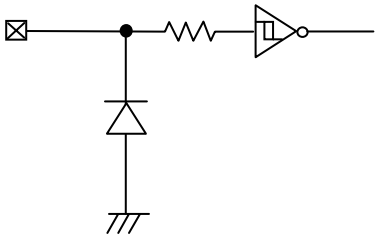


Figure 53. Input pin circuit diagram

○Input/Output (SDA)

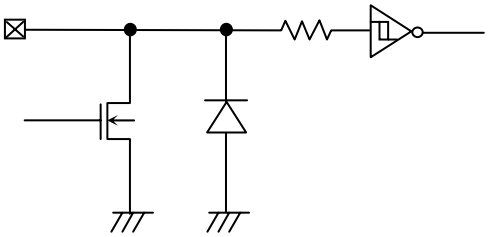


Figure 54. Input /output pin circuit diagram

●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following condition at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of tR, tOFF, and Vbot for operating POR circuit.

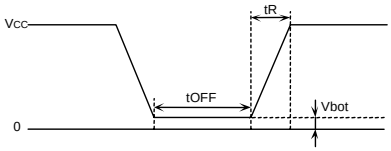


Figure 55. Rise waveform diagram

Recommended conditions of tR,tOFF,Vbot

tR	tOFF	Vbot
10ms or below	10ms or longer	0.3V or below
100ms or below	10ms or longer	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above conditions 1 cannot be observed. When SDA becomes 'L' at power on.

→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

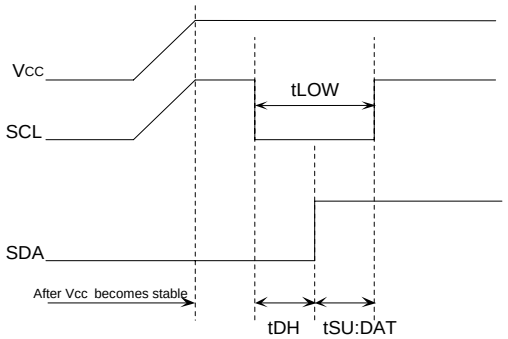


Figure 56. When SCL='H' and SDA='L'

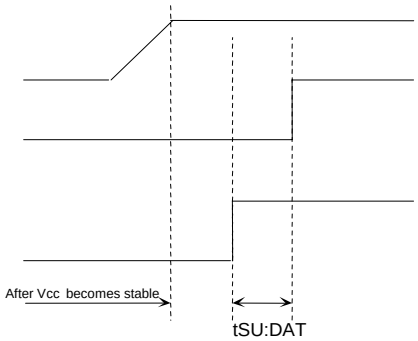


Figure 57. When SCL='H' and SDA='L'

b) In the case when the above condition 2 cannot be observed.

→After power source becomes stable, execute software reset(Page 17).

c) In the case when the above conditions 1 and 2 cannot be observed.

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●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

●Notes for Use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

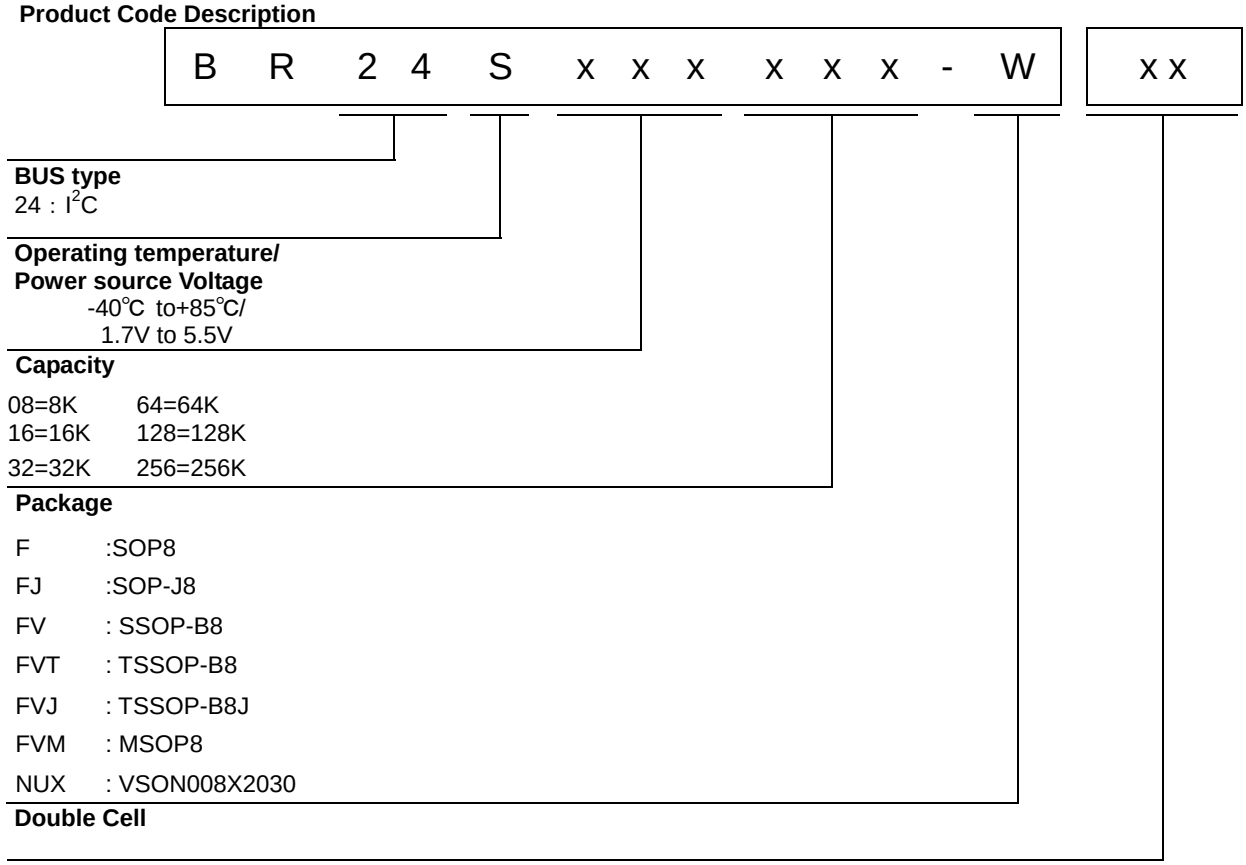
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

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●Ordering Information

Product Code Description

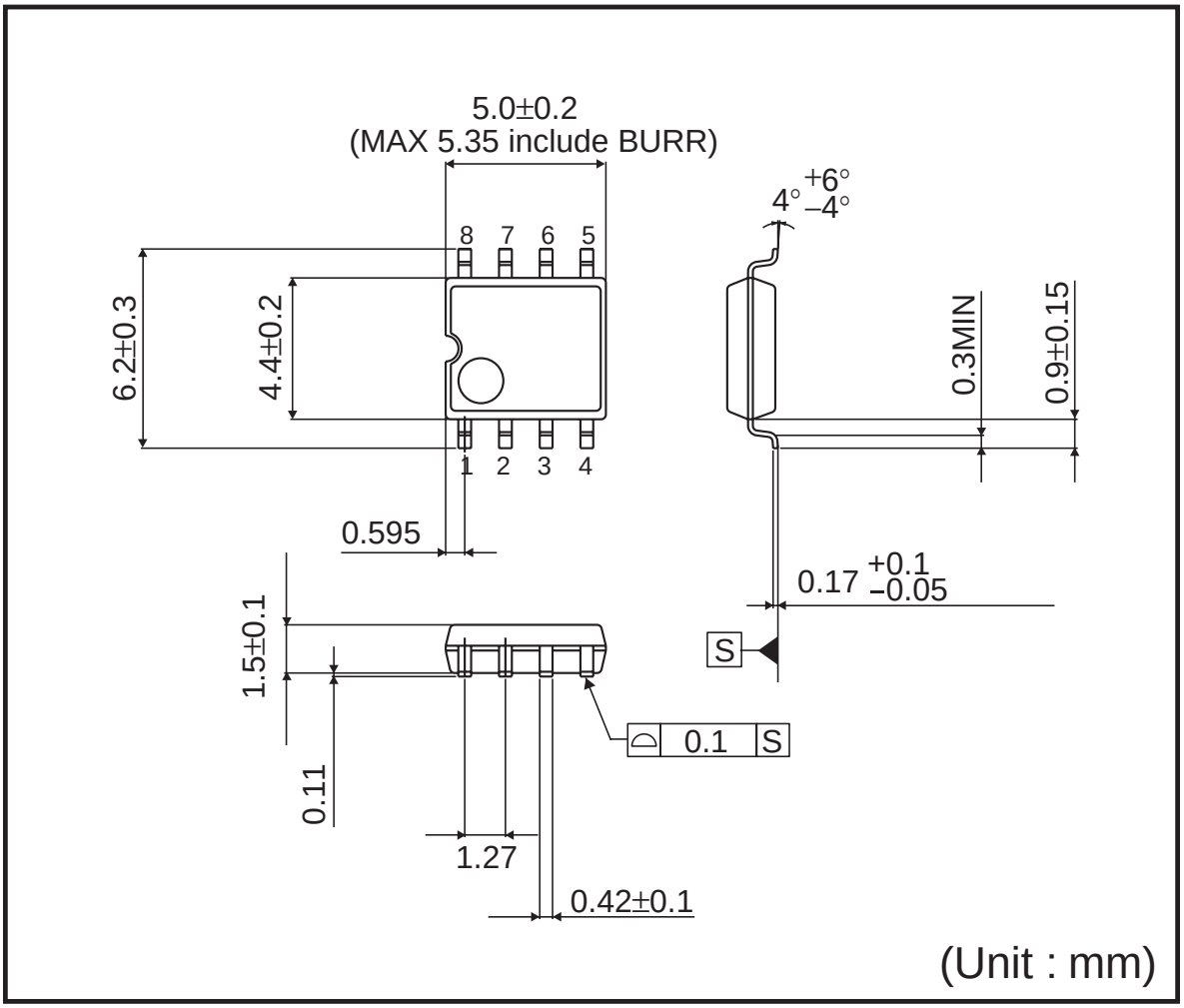


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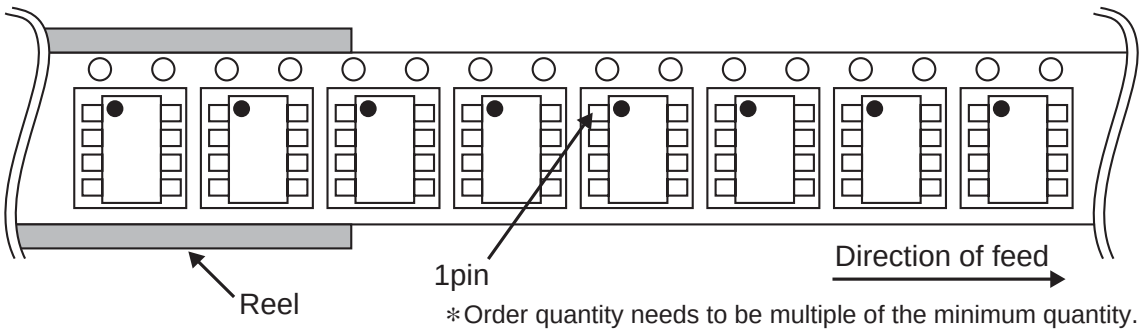
●**Physical Dimension Tape and Reel Information**

SOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



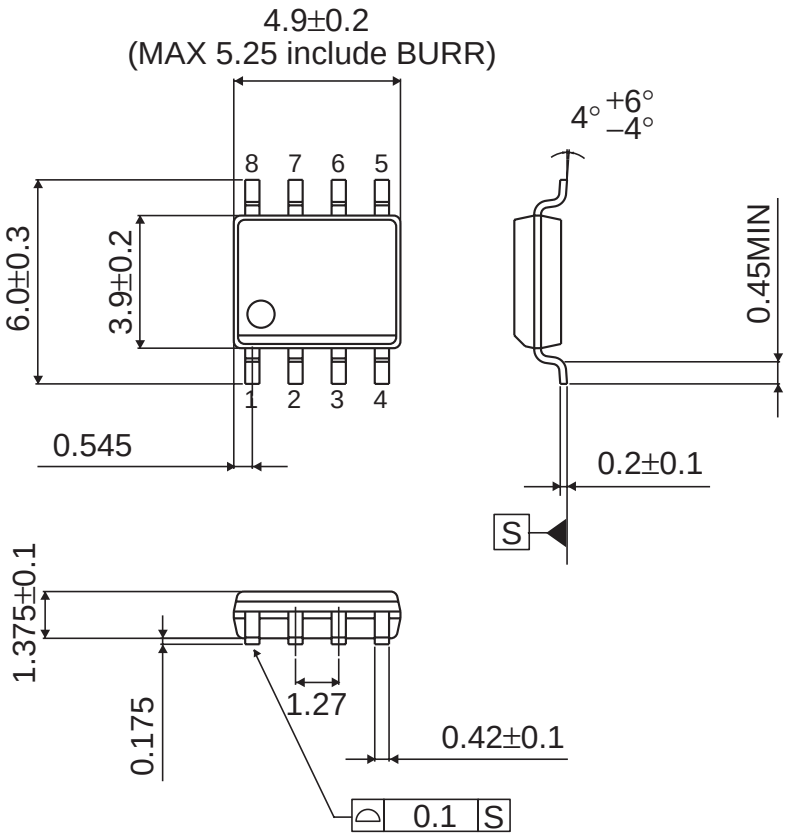
＊Order quantity needs to be multiple of the minimum quantity.

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●**Physical Dimension Tape and Reel Information - continued**

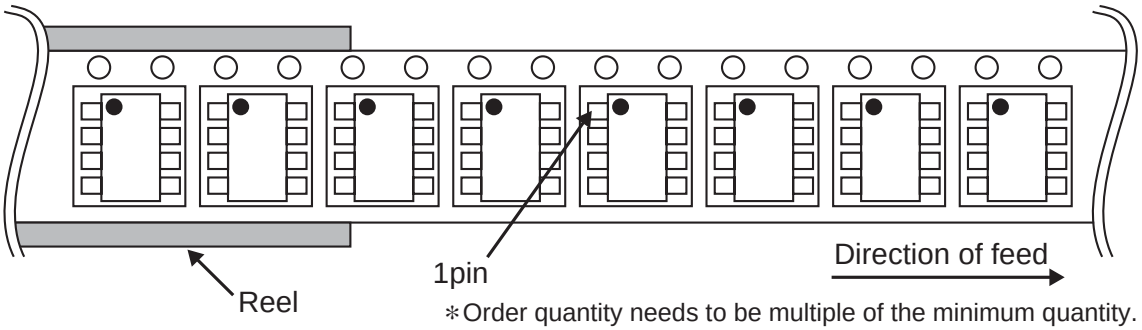
SOP-J8



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



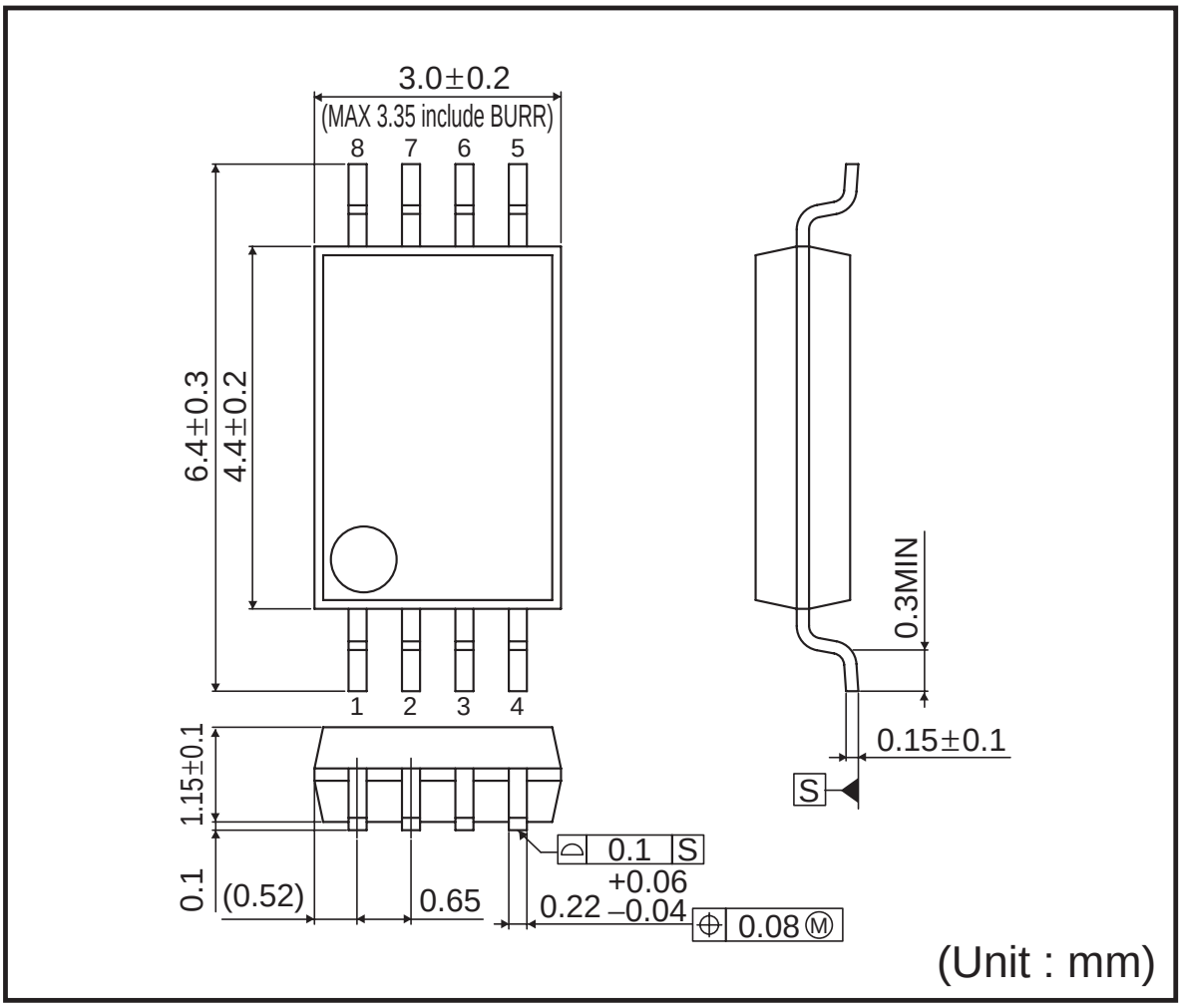
∗Order quantity needs to be multiple of the minimum quantity.

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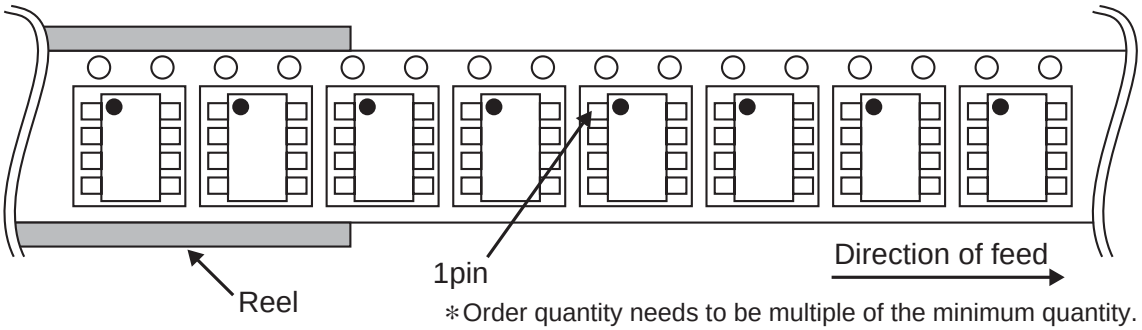
●**Physical Dimension Tape and Reel Information - continued**

SSOP-B8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



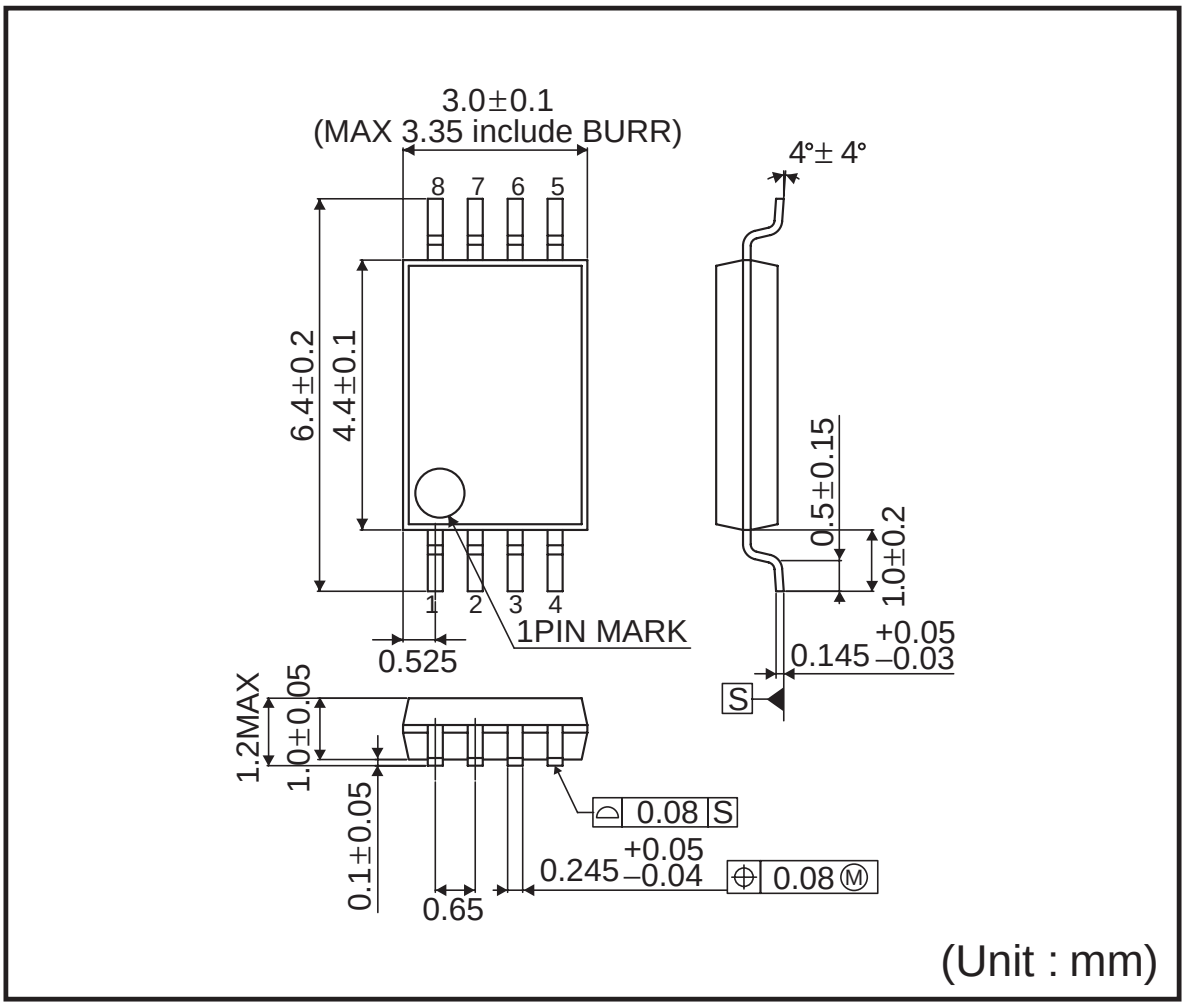
∗Order quantity needs to be multiple of the minimum quantity.

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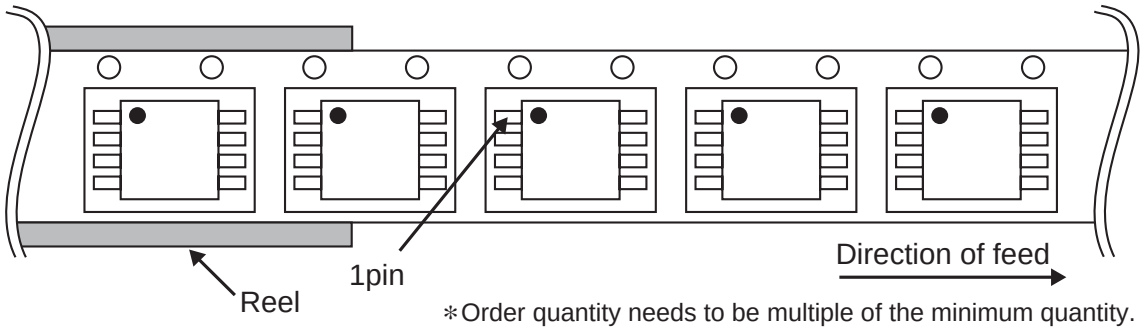
●**Physical Dimension Tape and Reel Information - continued**

TSSOP-B8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



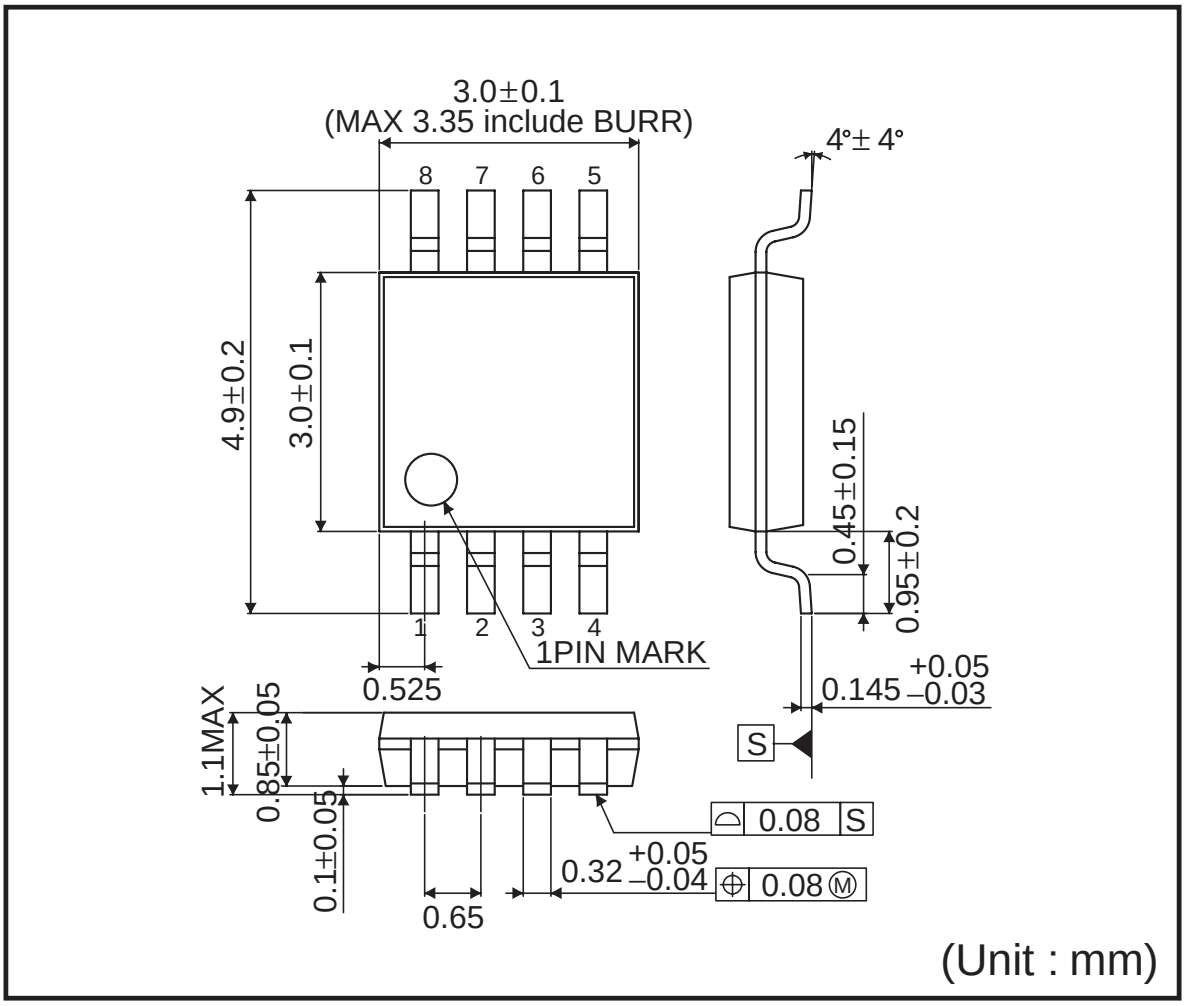
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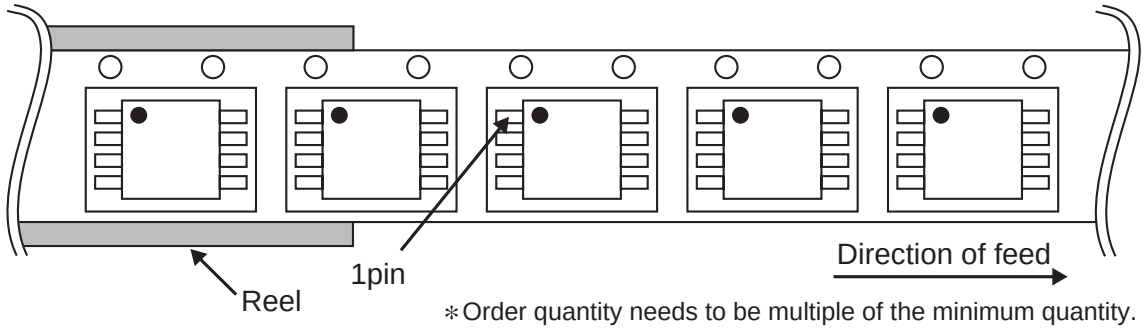
●**Physical Dimension Tape and Reel Information - continued**

TSSOP-B8J



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



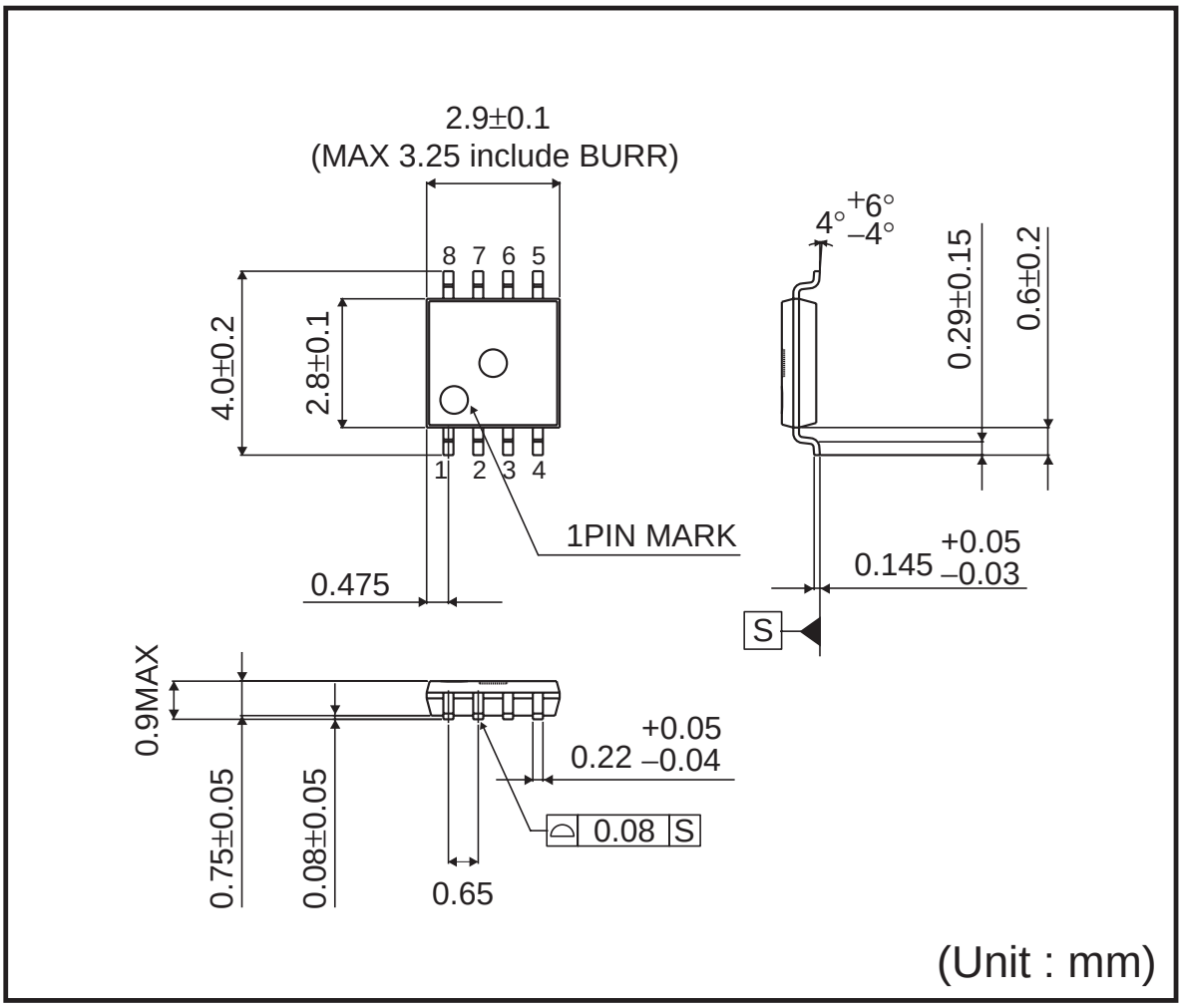
∗Order quantity needs to be multiple of the minimum quantity.

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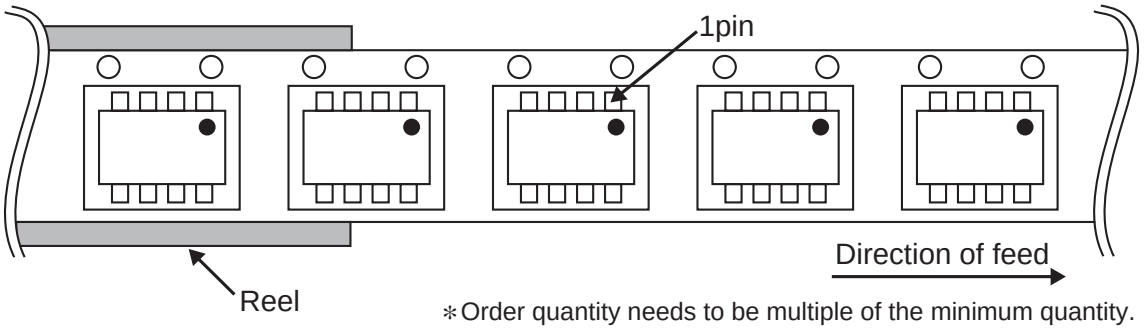
●**Physical Dimension Tape and Reel Information - continued**

MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



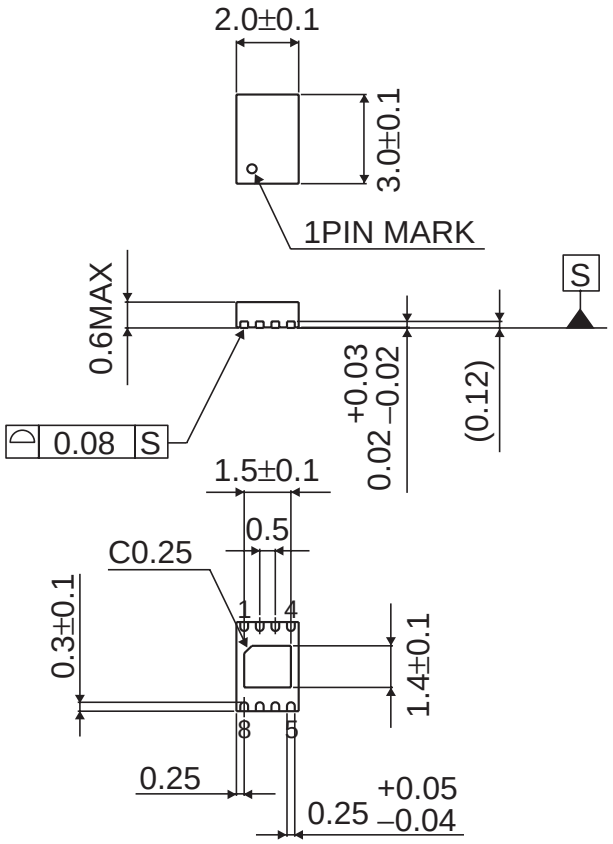
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●**Physical Dimension Tape and Reel Information - continued**

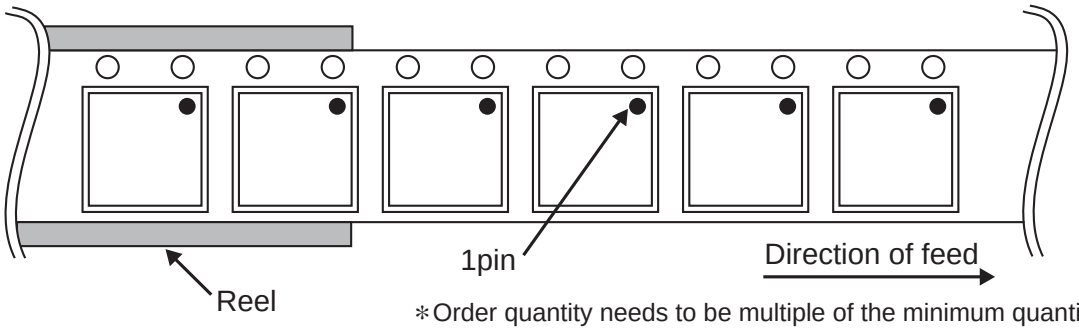
VSON008X2030



(Unit : mm)

<Tape and Reel information>

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Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



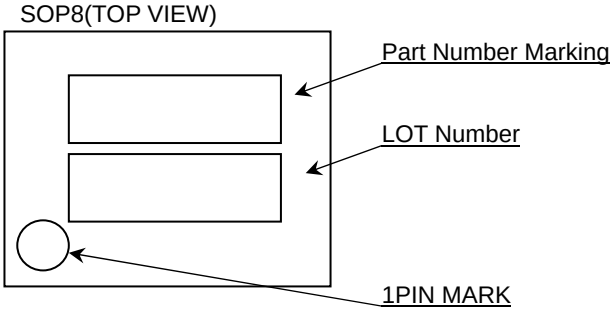
∗Order quantity needs to be multiple of the minimum quantity.

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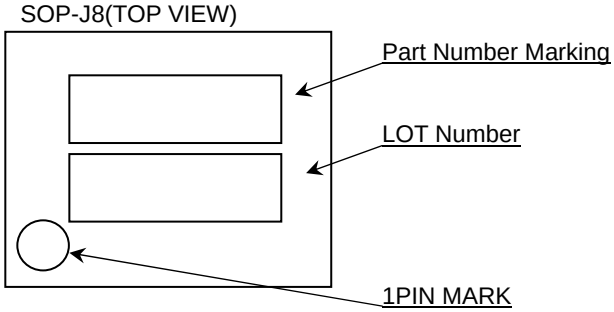
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●Marking Diagrams

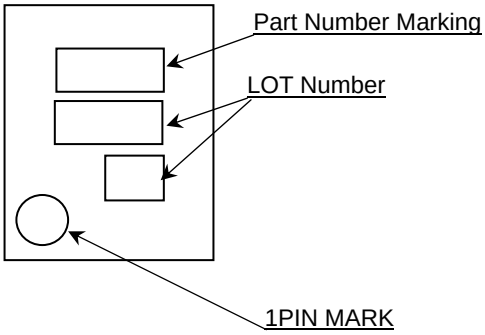
SOP8(TOP VIEW)



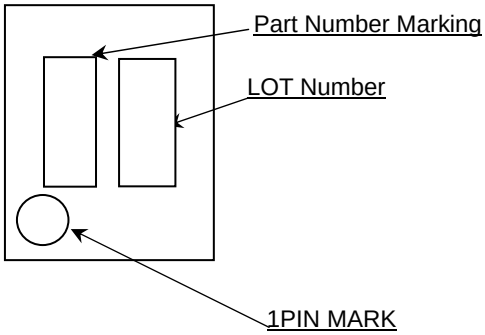
SOP-J8(TOP VIEW)



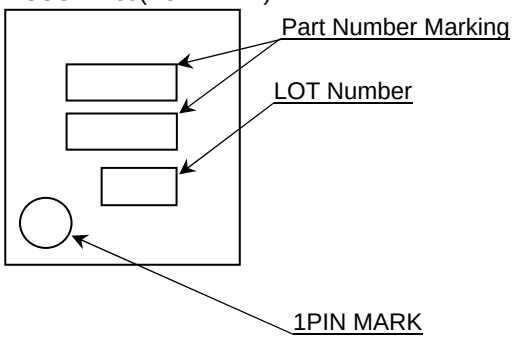
SSOP-B8(TOP VIEW)



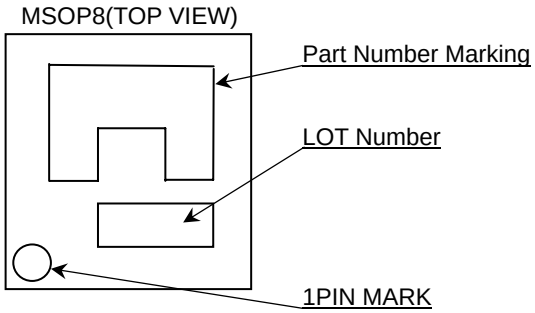
TSSOP-B8(TOP VIEW)



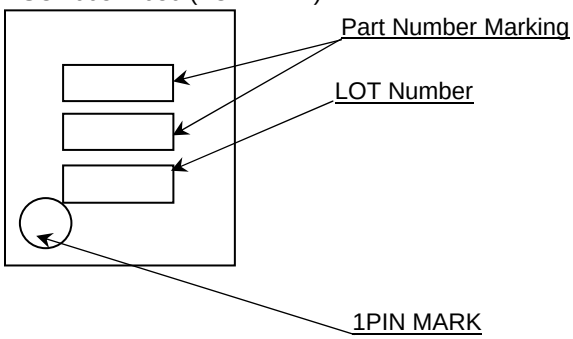
TSSOP-B8J(TOP VIEW)



MSOP8(TOP VIEW)



VSON008X2030 (TOP VIEW)



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●**Marking Information**

Capacity	Product Name Marking	Package Type
8K	S08	SOP8
	S08	SOP-J8
	S08	SSOP-B8
	S08	TSSOP-B8
	S08	TSSOP-B8J
	S08	MSOP8
	S08	VSON008X2030
16K	S16	SOP8
	S16	SOP-J8
	S16	SSOP-B8
	S16	TSSOP-B8
	S16	TSSOP-B8J
	S16	MSOP8
	S16	VSON008X2030
32K	S32	SOP8
	S32	SOP-J8
	S32	SSOP-B8
	S32	TSSOP-B8
	S32	TSSOP-B8J
	S32	MSOP8
	S32	VSON008X2030
64K	S64	SOP8
	S64	SOP-J8
	S64	SSOP-B8
	S64	TSSOP-B8
	S64	TSSOP-B8J
	S64	MSOP8
128K	4S128	SOP8
	4S128	SOP-J8
	S128	SSOP-B8
	4S128	TSSOP-B8
256K	4S256	SOP8
	4S256	SOP-J8

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●Revision History

Date	Revision	Changes
20.Aug.2012	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

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