

CoolGaN™

CoolGaN™ Transistor 175 V G3

Features

- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade 3x5 package

Potential applications

- Telecom & Datacenter
- Class D Audio
- Sync Rectification for AC-DC and DC-DC converters
- e-Mobility, UAVs
- Battery powered tools
- Solar & Energy storage systems

Product validation

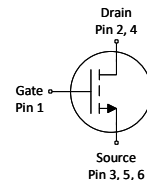
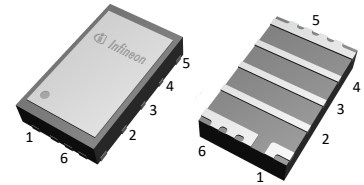
Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	175	V
$R_{DS(on)}$	6.7	mΩ
I_D	46	A
Q_{oss}	60	nC
Q_G	8.5	nC
Q_{rr}	0	nC

Part number	Package	Marking	Related links
IGC090S18S1	PG-TSON-6	90SJ1	see Appendix A

PG-TSON-6



Top side is exposed silicon substrate, internally connected to source terminal. Not recommended to use as an electrical connection.

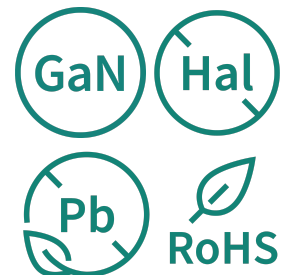


Table of contents

Description	1
Maximum ratings	3
Recommended operating conditions	4
Thermal characteristics	5
Electrical Characteristics	6
Electrical characteristics diagrams	8
Package outlines	13
Appendix A	16
Revision history	17
Trademarks	18
Disclaimer	18

1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	175	V	$V_{GS}=0\text{ V}$
Pulsed drain-source voltage ¹⁾	$V_{DS, pulse}$	-	-	210	V	$V_{GS}=0\text{ V}$, 1 h total time
Continuous drain current	I_D	-	-	46	A	$V_{GS}=5\text{ V}$, $T_C=25\text{ °C}$
				12		$V_{GS}=5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D, pulse}$	-	-	340	A	$T_j=25\text{ °C}$
				210		$T_j=150\text{ °C}$
Pulsed gate-source voltage ¹⁾	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	45	W	$T_C=25\text{ °C}$
				3.3		$T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40	-	-	-	-

1) Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

2) Device on 4-layer FR4 PCB, vertical in still air.

3) Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	0.5	0.6	°C/W	-
Thermal resistance, junction - case, bottom			1.9	2.8		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	60	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	38	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical Characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.0	2.9	V	$V_{DS}=V_{GS}$, $I_D=5.0\text{ mA}$
Drain-source leakage current	I_{DSS}	-	0.25	-	μA	$V_{DS}=140\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			3.0			$V_{DS}=140\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	18	-	μA	$V_{GS}=5\text{ V}$, $T_j=25\text{ °C}$
			0.01			$V_{GS}=-4\text{ V}$, $T_j=25\text{ °C}$
			150			$V_{GS}=5\text{ V}$, $T_j=125\text{ °C}$
			0.01			$V_{GS}=-4\text{ V}$, $T_j=125\text{ °C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.7	9.0	m Ω	$V_{GS}=5\text{ V}$, $I_D=10\text{ A}$
Gate resistance ⁴⁾	R_G	-	0.5	-	Ω	-

⁴⁾ Defined by design. Not subject to production test.

Table 6 Capacitance characteristics ⁵⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	800	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=87.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		420			
Reverse transfer capacitance	C_{rss}		3.8			

⁵⁾ Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.0	-	nC	$V_{DS}=87.5\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		1.6		nC	
Gate to drain charge ⁶⁾	Q_{gd}		2.1		nC	
Switching charge	Q_{sw}		2.5		nC	
Gate charge total ⁶⁾	Q_g		8.5		nC	
Gate plateau voltage	$V_{plateau}$		2.5		V	
Output charge ⁶⁾	Q_{oss}	-	60	-	nC	$V_{DS}=87.5\text{ V}$, $V_{GS}=0\text{ V}$

⁶⁾ Defined by design. Not subject to production test.

Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	15	A	$T_C=25\text{ °C}$
Pulsed current, reverse	$I_{S,pulse}$			184		
Source-Drain reverse voltage	V_{SD}	-	2.3	-	V	$V_{GS}=0\text{ V}, I_{S,pulse}=10\text{ A}, T_j=25\text{ °C}$
			2.0			$V_{GS}=0\text{ V}, I_{S,pulse}=0.5\text{ A}, T_j=25\text{ °C}$
Reverse recovery charge ⁷⁾	Q_{rr}	-	0	-	nC	$V_R=87.5\text{ V}, I_{S,pulse}=10\text{ A}, di_{S,pulse}/dt=100\text{ A}/\mu\text{s}$

⁷⁾ Defined by design. Not subject to production test.

5 Electrical characteristics diagrams

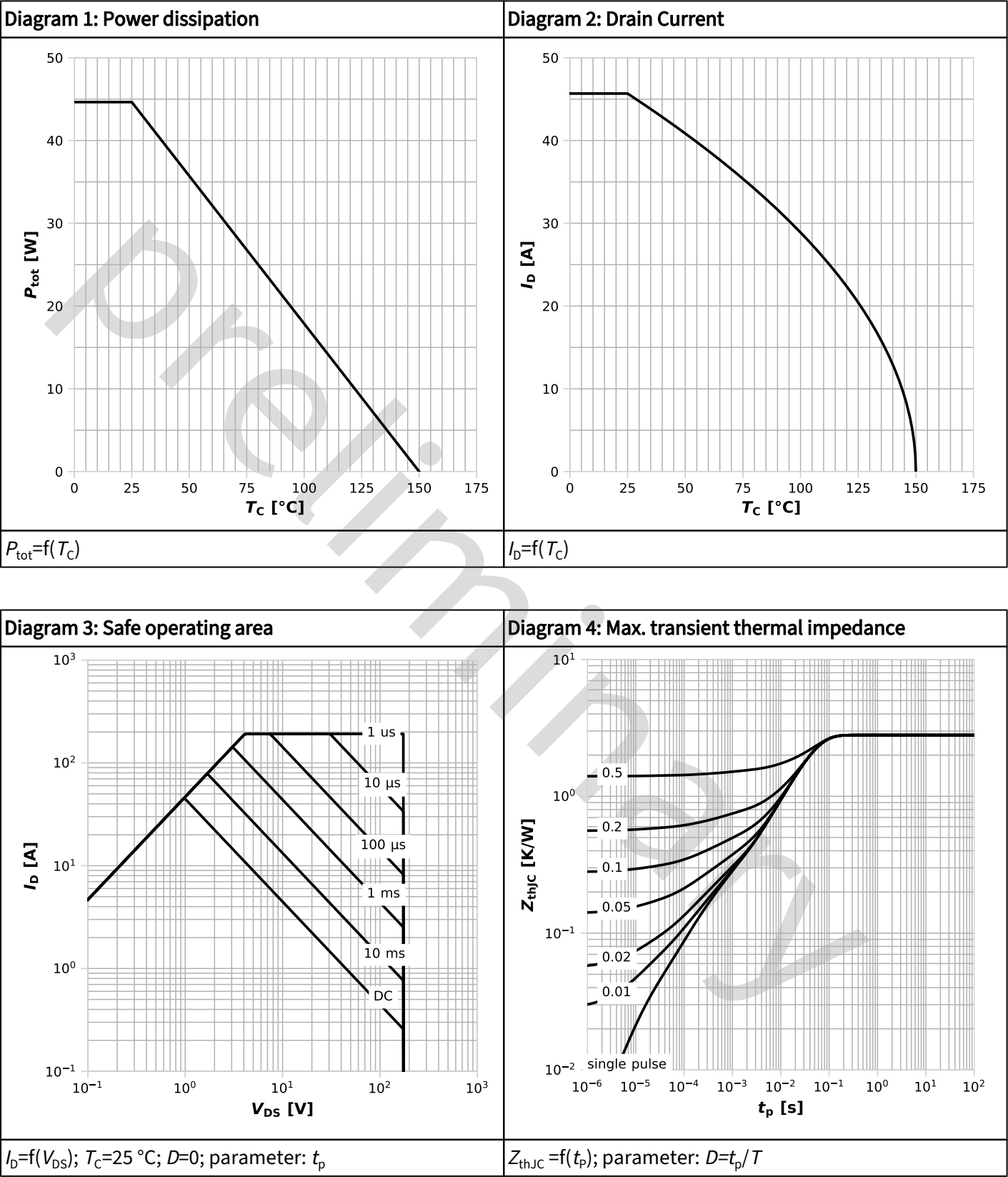
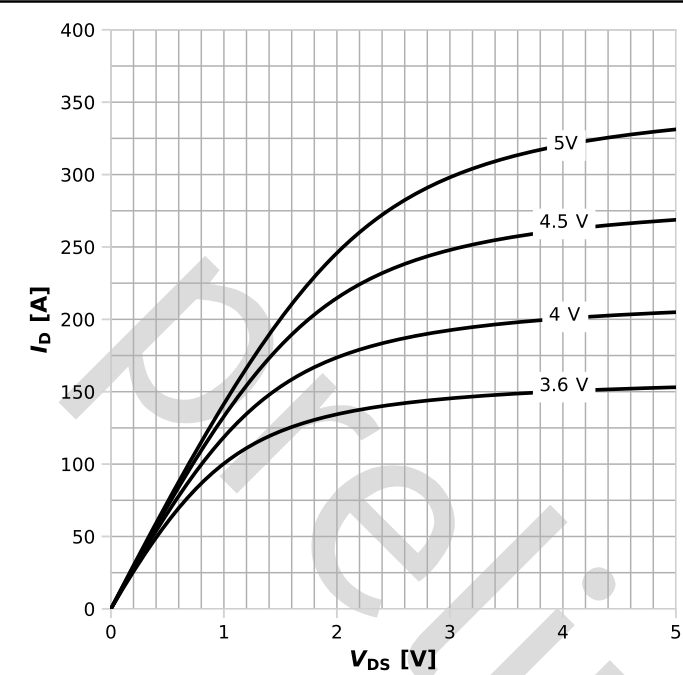
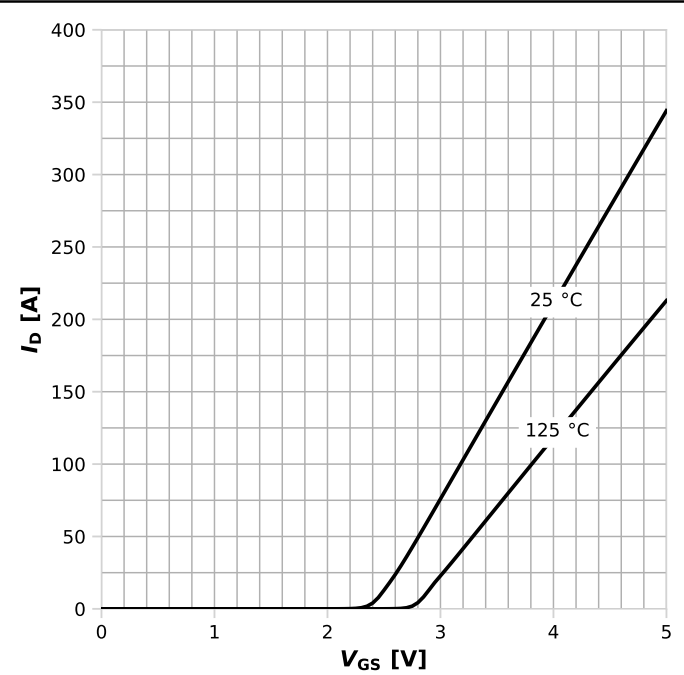


Diagram 5: Typ. output characteristics



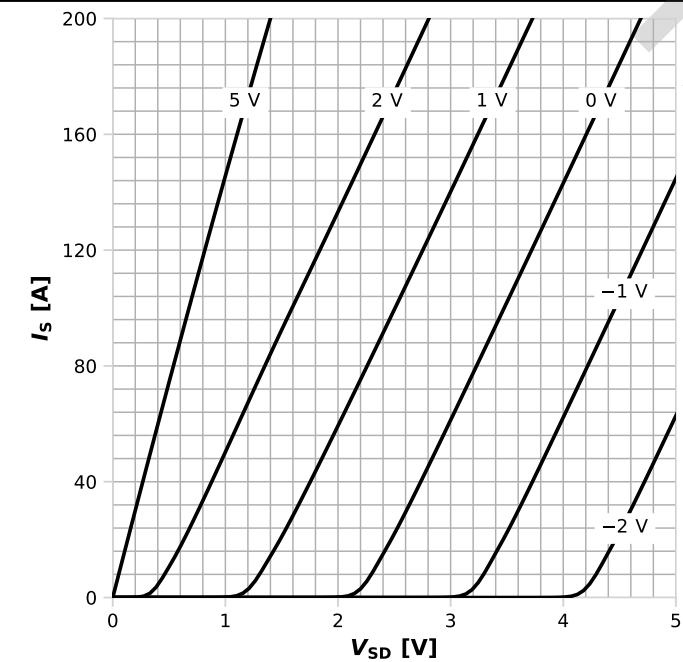
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



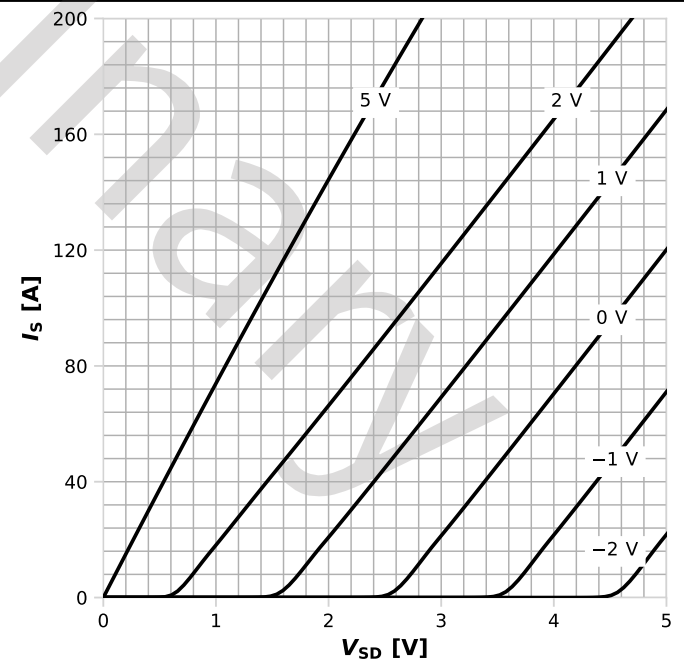
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. channel reverse characteristics



$I_S = f(V_{SD})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Typ. channel reverse characteristics



$I_S = f(V_{SD})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

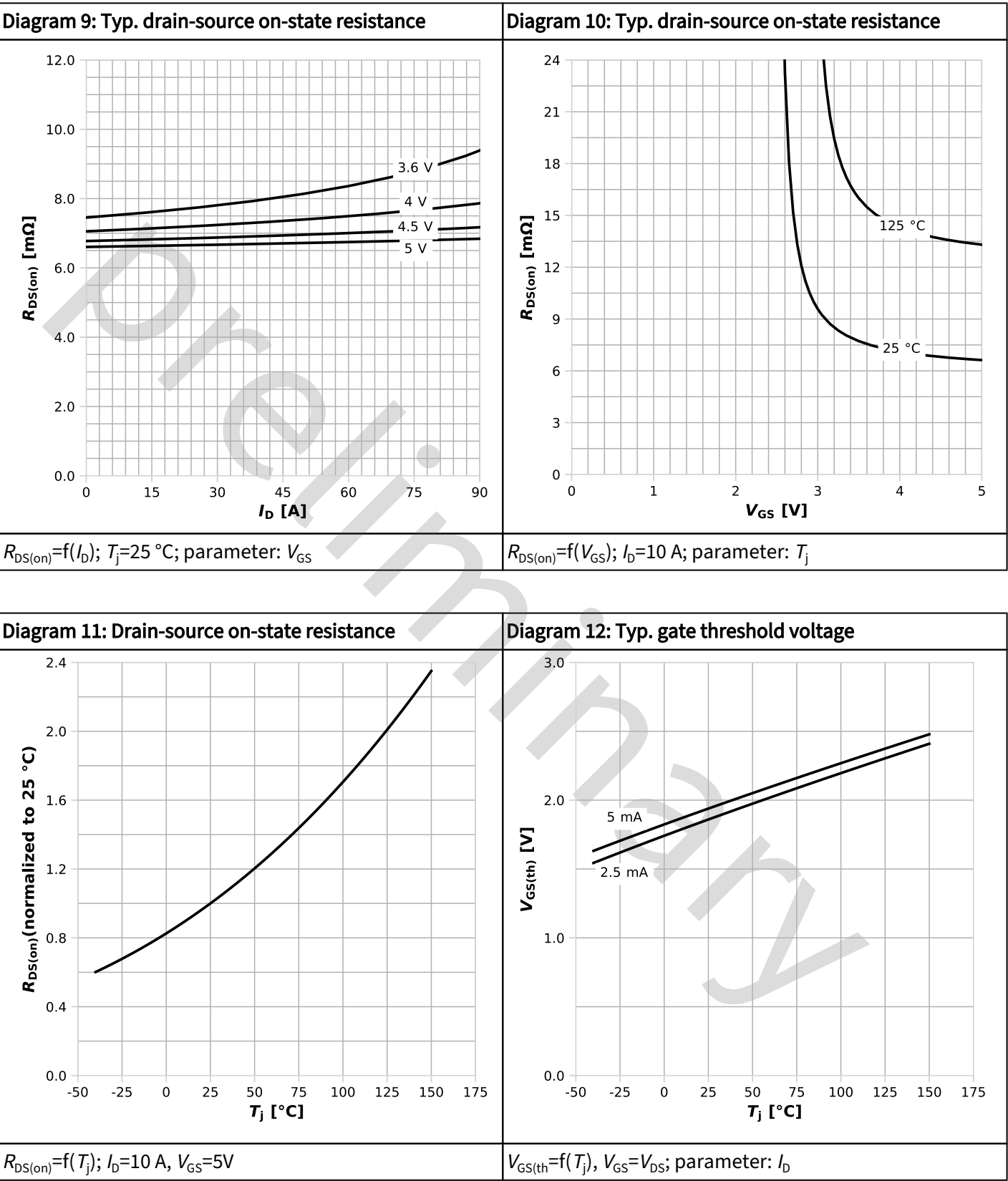
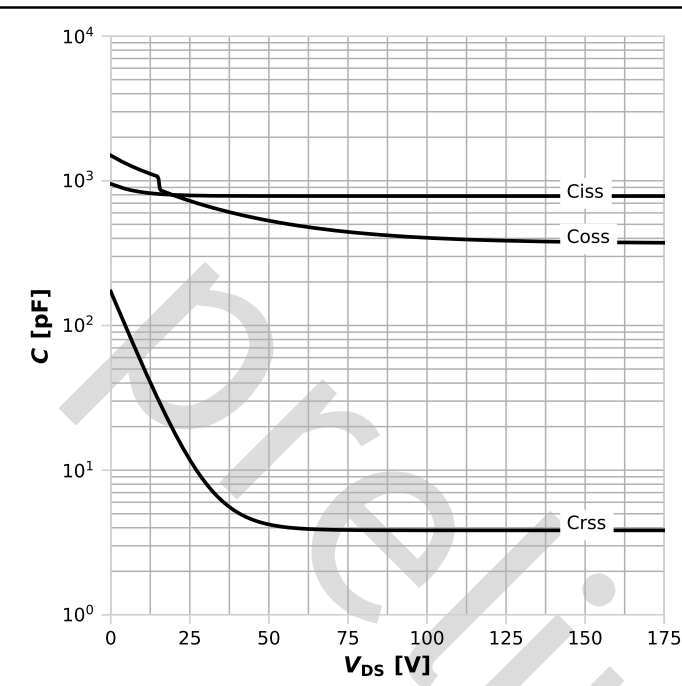
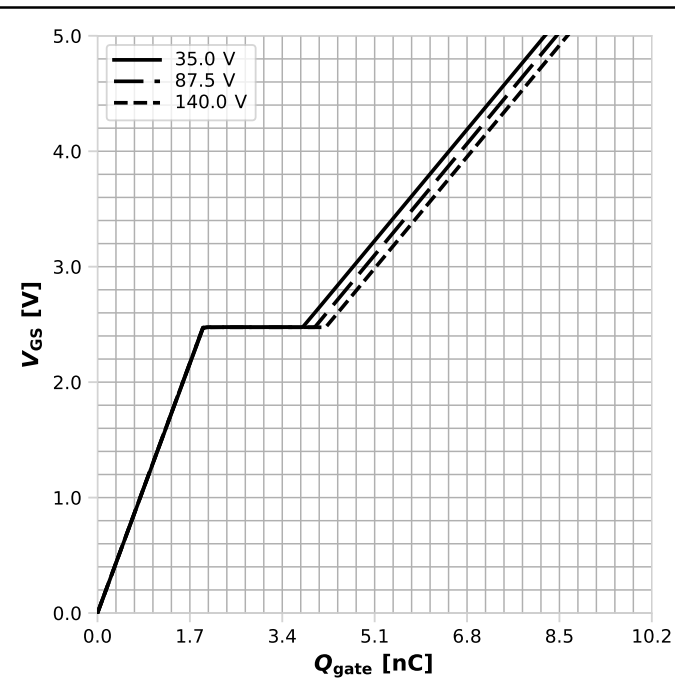


Diagram 13: Typ. capacitances



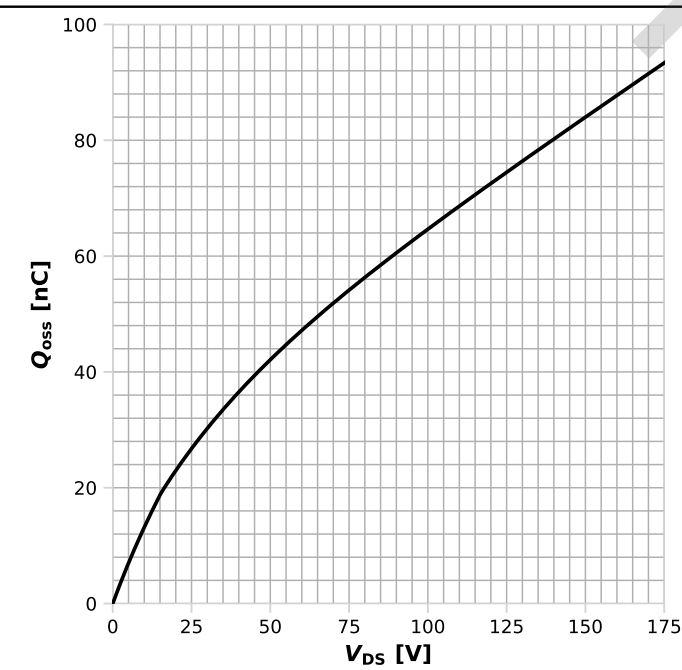
$C=f(V_{DS}); V_{GS}=0\text{ V}$

Diagram 14 Typ. gate charge



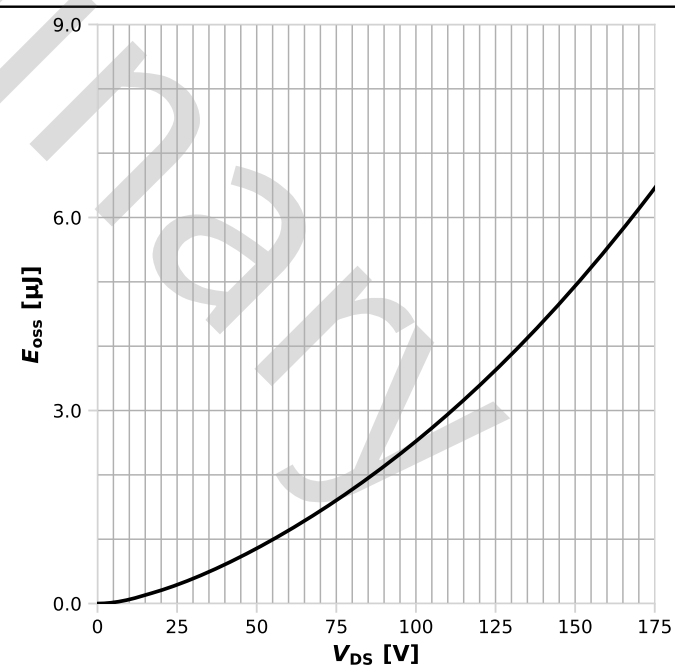
$V_{GS}=f(Q_{gate}); I_D=10\text{ A pulsed}; \text{parameter: } V_{DS}$

Diagram 15: Typ. output charge



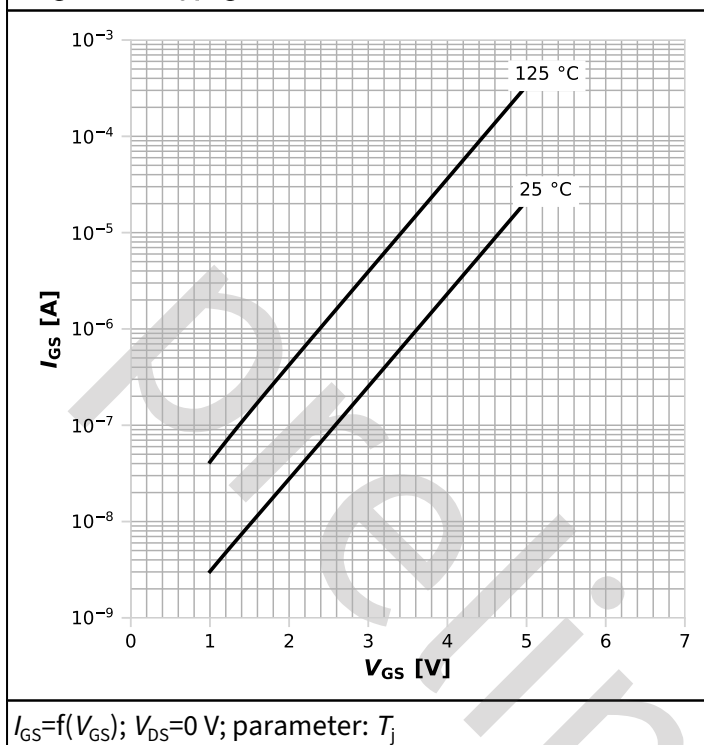
$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$

Diagram 16: Typ. Coss stored Energy



$E_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$

Diagram 17: Typ. gate characteristics forward



6 Package outlines

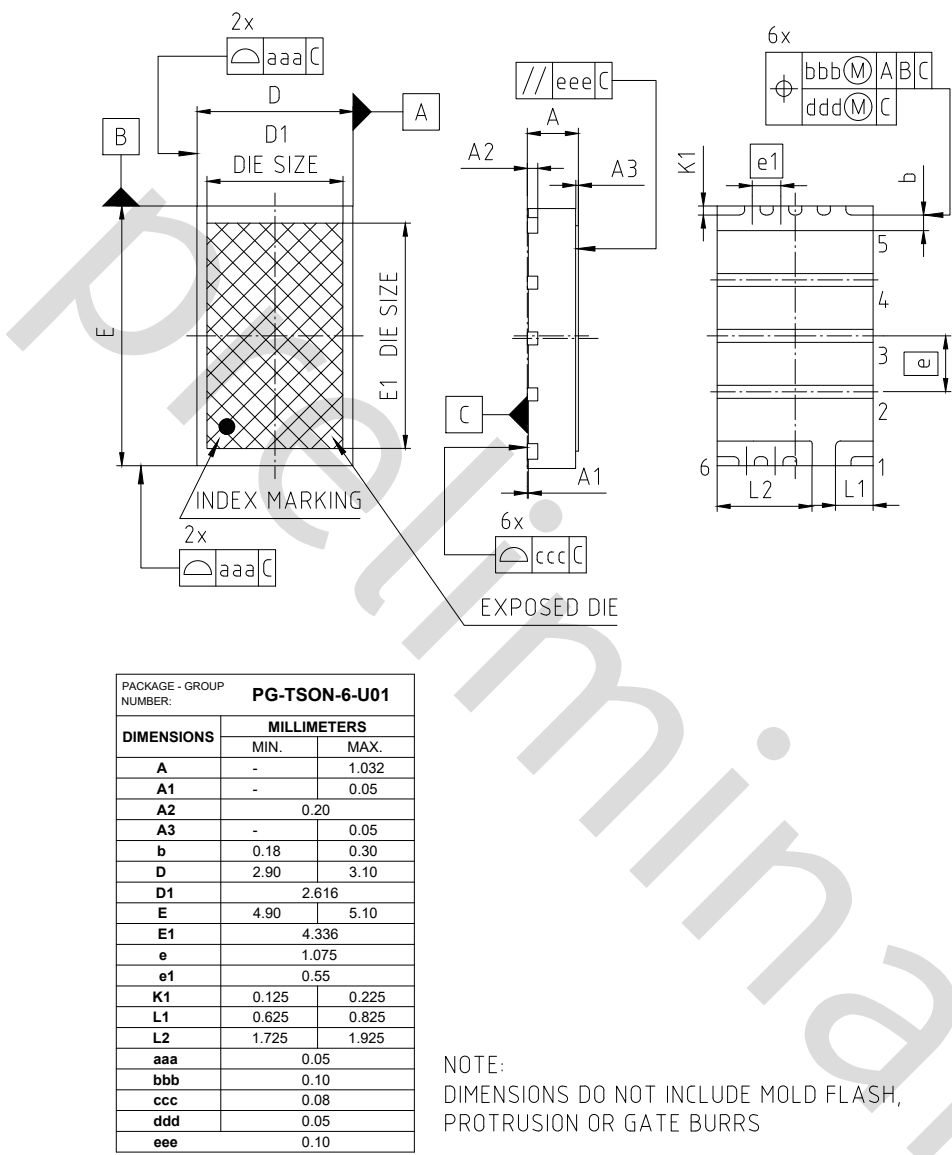


Figure 1 Outline PG-TSON-6, dimensions in mm

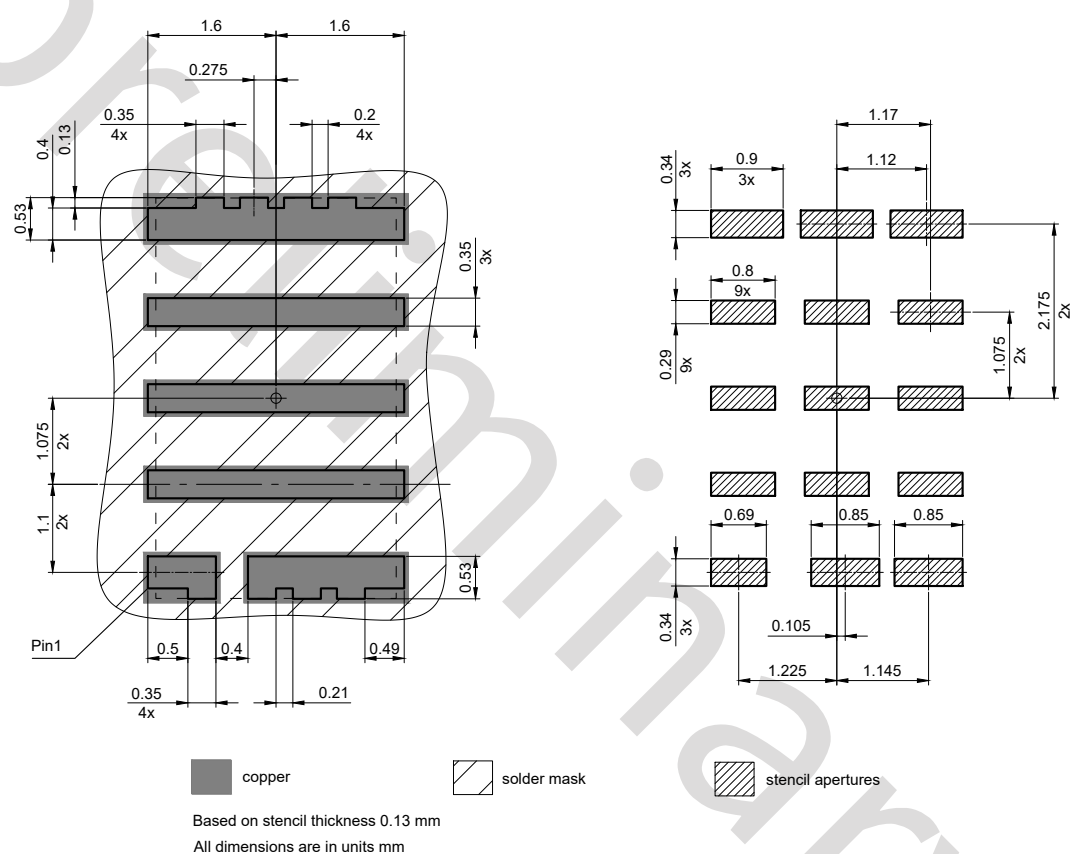


Figure 2 Footprint drawing PG-TSON-6, dimensions in mm

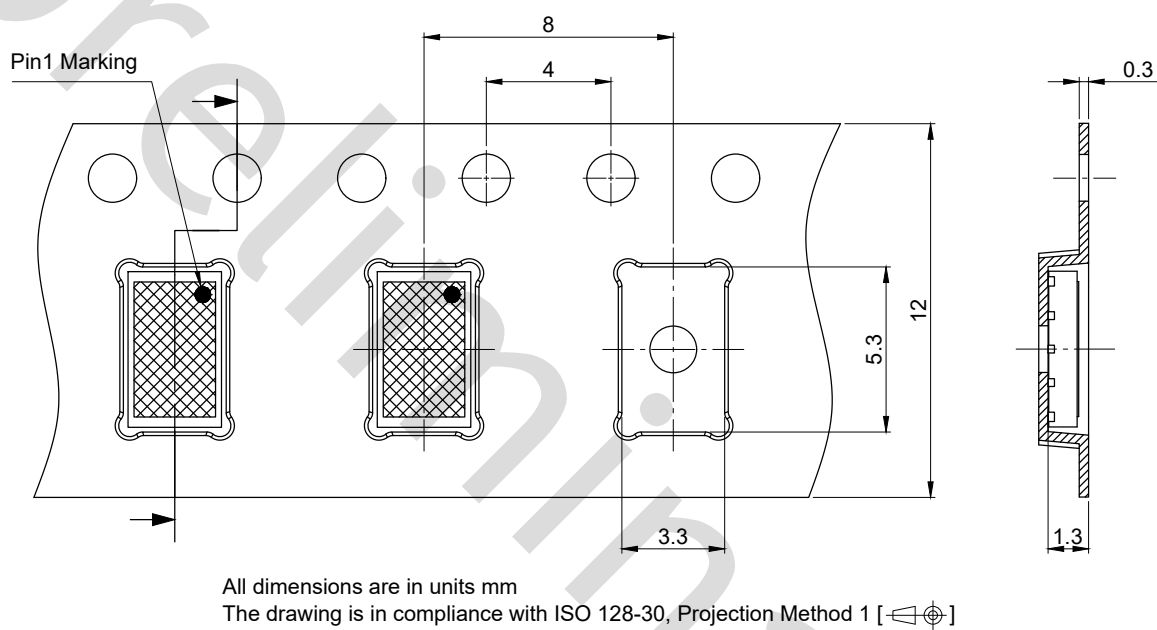


Figure 3 Packaging variant PG-TSON-6, dimensions in mm

7 Appendix A

Table 9 **Related links**

- [IFX CoolGaN™ GaN webpage](#)
- [IFX CoolGaN™ reliability white paper](#)
- [IFX CoolGaN™ gate driver application note](#)
- [IFX CoolGaN™ Evaluation Boards](#)
- [IFX Packages Description-PG-TSON-6-2](#)

Preliminary

Revision history

IGC090S18S1

Revision 2025-12-15, Rev. 0.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
0.1	2025-12-15	Release of preliminary version
0.2	2025-12-15	Updated marking

Preliminary

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