Ultra-Low Offset Voltage Operational Amplifier

OP07

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/marketSolutions/militaryAerospace/pdf/Die_Broc.pdf is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/OP07

2.0 Part Number. The complete part number(s) of this specification follow:

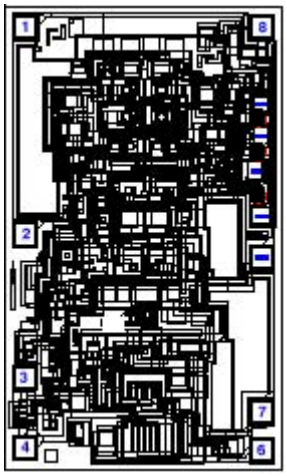
Part Number	Description
OP07-000C	Ultra-Low Offset Voltage Operational Amplifier
OP07R000C	Radiation Tested Ultra-Low Offset Voltage Operational Amplifier

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
57 mil x 93 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1. V_{IO} TRIM
2. -INPUT
3. +INPUT
4. $-V_S$
5. NC
6. OUTPUT
7. $+V_S$
8. V_{IO} TRIM

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3.3 Absolute Maximum Ratings 1/

Supply Voltage (V_S) ..... ±22V dc
Input Voltage (V_{IN}) 2/..... ±22V dc
Differential Input Voltage ....±30V dc
Output Short Circuit Duration..... Indefinite
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Ambient Operating Temperature Range..... -55°C to +125°C

Absolute Maximum Ratings Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For supply voltage less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Samples Size and Qual Acceptance Criteria – 10/0
(b) Qual Sample Package – DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I -Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Input Offset Voltage	V_{IO}		-25	+25	µV
Input Bias Current	$+I_{IB}$		-2	+2	nA
	$-I_{IB}$		-2	+2	
Input Offset Current	I_{IO}		-2	+2	nA
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	-10	10	µV/V
Input Voltage Range	IVR		±13		V
Common Mode Rejection Ratio	CMRR	V_{CM} = IVR	110		dB
Supply Current	I_S	No Load		4	mA
Output Voltage Swing	V_{OP}	R_L =1k Ω	±10		V
		R_L = 2k Ω	±12		
Open Loop Voltage Gain	A_{VS}	V_{OUT} = ±10V, R_L = 2kΩ	300		V/mV
Slew Rate	+SR, -SR	V_{IN} = ±5V, A_{VS} = 1	0.08		V/µs

Table I Notes:
1/ V_S = ±15V, V_{CM} = 0V, and T_A = 25°C, unless otherwise specified.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Input Offset Voltage	V_{IO}		1	-25	25	µV
			2, 3	-60	60	
		M, D, L. R 3/	1	-400	400	
Input Offset Current	I_{IO}	V_{CM} = 0V	1	-2	2	nA
			2, 3	-4	4	
		M, D, L. R 3/	1	-25	25	
Supply Current 2/	Is		1		4	mA
			2, 3		5	
		M, D, L. R 3/	1		4	
Input Offset Voltage Temperature Sensitivity 2/	ΔVIO/Δt		2, 3	-0.6	0.6	µV/°C
Input Voltage Range 2/	IVR		1, 2, 3	-13	13	V
Power Supply Rejection Ratio 2/	PSRR	Vs = ±3V to ±18V	1	-10	10	µV/V
			2, 3	-20	20	
Input Offset Adjustment Range 2/	+$V_{IO\ ADJ}$		1	0.5		mV
	-$V_{IO_{ADJ}}$				-0.5	
Output Voltage Swing 2/	V_{OP}	R_L = 1kΩ	1, 2, 3	-10	10	V
		R_L = 2kΩ		-12	12	
Open Loop Voltage Gain	A_{VS}	Vout = ±10V, R_L = 2kΩ	1	300		V/mV
			2, 3	200		
		M, D, L. R 3/	1	100		
Common Mode Rejection Ratio 2/	CMRR	V_{CM} = IVR	1	110		dB
			2, 3	106		
Slew Rate 2/	±SR	V_{IN} = ±5V, AV = 1	4	0.08		V/µS

Table II Notes:
1/ V_S = ±15V and V_{CM} = 0V, unless otherwise specified.
2/ This parameter not tested post irradiation.
3/ Devices tested at 100Krad irradiation.

Table III - Life Test Endpoint and Delta Parameter
(Product is tested in accordance with Table II with the following exceptions)

Parameter	Symbol	Sub-groups	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
			Min	Max	Min	Max		
Input Offset Voltage	V_{IO}	4	-60	60	-135	135	±75	µV
		5, 6			-170	170		
Input Bias Current	$+I_{IB}$	1	-3	+3	-4	+4	±1	nA
		2, 3			-6	+6		
	$-I_{IB}$	1	-3	+3	-4	+4	±1	
		2, 3			-6	+6		
Input Offset Current	I_{IO}	1	-3	+3	-4	+4		nA
		2, 3			-6	+6		

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	2 Nov. 2001
B	Change PSRR range from ±4.5 to ±20V to ±3 to ±18V on Table I. Update web address	20 Dec. 2001
C	Add radiation part. Update web address	Feb. 10, 2003
D	Die picture labeled incorrectly, update to current revision.	July 22, 2003
E	Update 1.0 Scope description.	23 Jul. 2007
F	Update header/footer & add to 1.0 scope description.	Feb. 13,2008
G	Add Junction Temperature…..+150°C to 3.3 Absolute Max. Ratings	March 31, 2008
H	Updated Section 4.0c note to indicate pre-screen temp testing being performed.	June 5, 2009
I	Updated fonts and sizes to ADI standards	Sept 27, 2011