EZ-PD™ PMG1-B1 USB Type-C Buck-boost controller

Single-port

General description

EZ-PD™ PMG1-B1 is a highly integrated single-port USB Type-C Power Delivery (PD) solution with integrated buck-boost controllers. It complies to the latest USB Type-C and PD specifications. EZ-PD™ PMG1-B1 has integrated gate drivers for VBUS NFET on the consumer path for sink application. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ PMG1-B1 supports a wide input voltage range (4 to 24 V with 40 V tolerance) and programmable switching frequency (150 to 600 kHz) in an integrated PD solution.

EZ-PD™ PMG1-B1 is the most programmable USB-PD solution with on-chip 32-bit Arm® Cortex®-M0 processor, 128-KB flash, 16-KB RAM and 32-KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as ADC, PWMs and timers.

Applications

- Cordless power tool charger
- Wireless speakers
- Portable electronics

Features

USB-PD

- Supports one USB-PD port
- Supports latest USB-PD 3.1
- Extended data messaging

Type-C

- Configurable resistors R_P and R_D
- VBUS NFET gate driver
- Integrated 100-mW VCONN power supply and control

1x buck-boost controller

- 150 kHz to 600 kHz switching frequency
- 5.5 to 24 V input, 40 V tolerant
- 3.3 to 21.5 V output
- Supports selectable pulse skipping mode (PSM) and forced continuous conduction mode (FCCM)
- Supports soft start
- Programmable spread spectrum frequency modulation for low EMI
- Supports current sensing for constant current control

1x legacy/proprietary charging block

- Supports Apple charging 2.4A and USB BC 1.2

Features

System-level fault protection

- VBUS overvoltage protection (OVP), and undervoltage protection (UVP)
- VBUS to CC short protection
- VOUT UVP, OVP, and OCP
- Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
- Supports connector and board temperature measurement using external thermistors

32-bit MCU subsystem

- 48-MHz Arm® Cortex®-M0 CPU
- 128-KB Flash
- 16-KB SRAM
- 32-KB ROM

Peripherals and GPIOs

- Up to 21 GPIOs including two over-voltage GPIOs
- 2x 8-bit ADC
- 8x 16-bit Timer/Counter/PWMs (TCPWM)
- 1x 12-bit ADC

Communication interfaces

- 3x SCBs (I^2C/SPI/UART/LIN)

Clocks and oscillators

- Integrated oscillator eliminating the need for an external clock

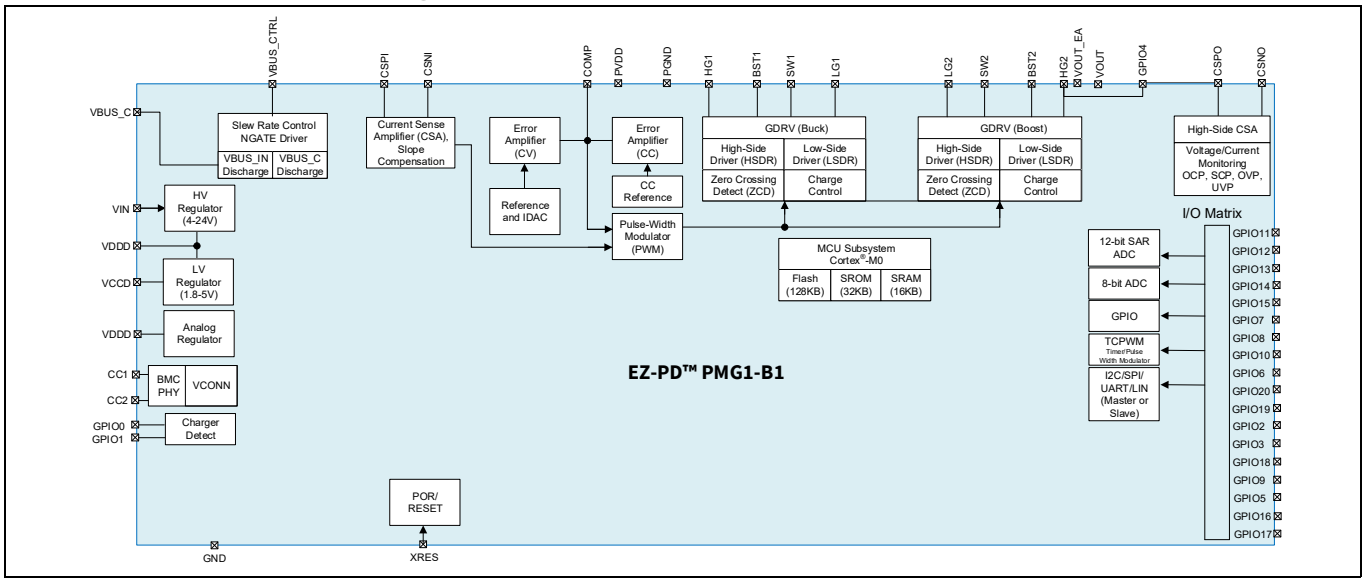
Power supply

- 4 to 24 V input (40 V tolerant)
- 3.3 to 21.5 V output
- Integrated LDO capable of 5 V, 75 mA
- Standby regulator of 3 V, 10 mA

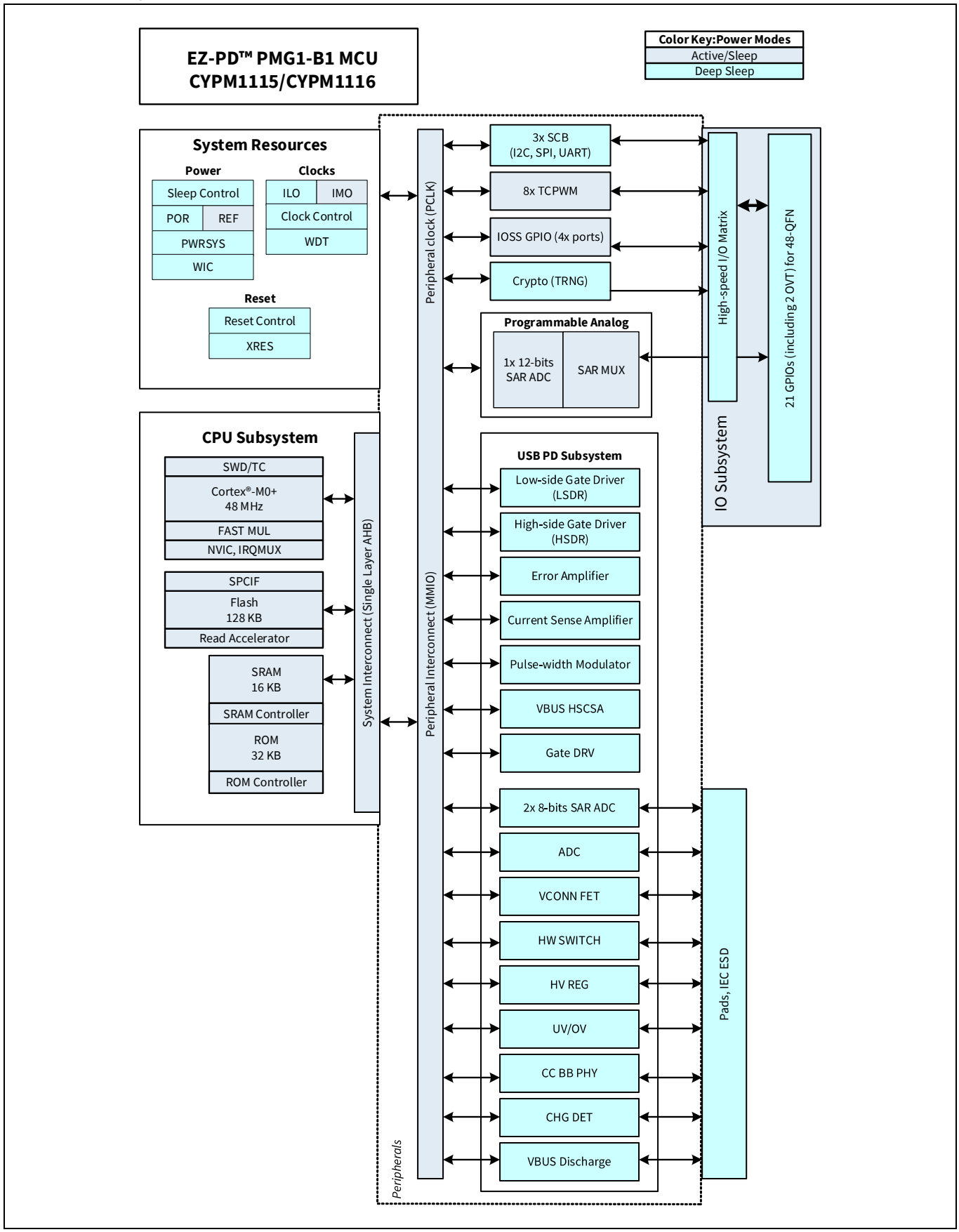
Packages

- 48-pin QFN
- Supports ambient temperature range (–40°C to +105°C) with 125°C operating junction temperature

Functional block diagram



Block diagram



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1 Functional overview

1.1 MCU subsystem

1.1.1 CPU

The Cortex®-M0 in EZ-PD™ PMG1-B1 devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

1.1.2 Flash ROM and SRAM

EZ-PD™ PMG1-B1 devices have 128-KB flash and 32-KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as I^2C, SPI, and so on. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest USB power delivery specifications and application needs.

The 16-KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

1.2 USBPD subsystem

This subsystem provides the interface to the Type-C USB port. This subsystem comprises:

- USBPD physical layer
- VCONN switches and 100mW VCONN source
- Undervoltage protection (UVP), overvoltage protection (OVP) on VBUS
- Output high-side current sense amplifier (HS CSA)
- VBUS discharge control
- Gate driver for VBUS consumer NFET
- Charger detection block for legacy charging (for example: BC1.2, Apple charging, and so on)
- Short-circuit protection (SCP)
- VBUS to CC SCP

1.2.1 USBPD physical layer

The USBPD subsystem contains the USBPD physical layer block and supporting circuits. The USBPD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.1 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel. The USBPD block includes all termination resistors (R_p and R_d) and their switches as required by the USB Type-C spec. R_p and R_d resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The R_p resistor is implemented as a current source.

The PMG1-B1 device family along with the accompanying firmware is fully complaint with revision 3.1 of the USB Power delivery specification. The device supports programmable power supply (PPS) operation at all valid voltages from 3.3 to 21 V.

EZ-PD™ PMG1-B1 devices support R_p under HW control in unconnected (standby) state to minimize standby power.

EZ-PD™ PMG1-B1 devices support USBPD extended messages containing data of up to 260 bytes. The extended messages are larger than expected by USBPD 2.0 hardware. As per the USBPD protocol specification, USBPD 3.1 compliant devices implement a chunking mechanism; messages are limited to revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

1.2.2 VCONN switches

EZ-PD™ PMG1-B1' internal LDO voltage regulator is capable of powering a 100 mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories (VPA) as defined in the USB Type-C specification. All circuitry including VCONN switches and overcurrent protection is integrated in the device. In the event the VCONN current exceeds the VCONN OCP limit, EZ-PD™ PMG1-B1 can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.3 VBUS UVP and OVP

VBUS under-voltage and overvoltage faults are monitored using internal resistor dividers. The fault thresholds and response times are user configurable. In the event of a UVP or OVP, EZ-PD™ PMG1-B1 can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect followed by re-connect.

1.2.4 VOUT OCP and SCP

VOUT overcurrent and short-circuit faults are monitored using internal CSAs. Similar to OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. In the event of OCP or SCP, PMG1-B1 can be configured to shut down the buck-boost controller.

1.2.5 HS-CSA for VOUT

EZ-PD™ PMG1-B1 device family supports VOUT current measurement and control using an external resistor (5 mΩ) in series with the VOUT path. The voltage drop across this resistor is used to measure the average output current. The same resistor is also used to sense and precisely control the output current in the constant current mode of operation.

1.2.6 VBUS discharge control

The chip supports high-voltage (21.5 V) VBUS discharge circuitry. Upon the detection of device disconnection, faults, or hard resets, the chip will discharge the output VBUS terminals to vSafe5V and/or vSafe0V within the time limits specified in the USBPD specification.

1.2.7 Gate driver for VBUS consumer NFET

EZ-PD™ PMG1-B1 devices have an integrated high-voltage gate driver to drive the gate of an external high-side NFET on the VBUS consumer path. The gate driver drives the load switch that controls the connection between VBUS_C and CSPI. VBUS_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives VBUS_CTRL low to 0 V. To turn on the external NFET, it drives the gate to VBUS_C + 8 V. There is an optional slow turn-on feature which reduces the high-current spikes on the output. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 to 10 ms is configurable using firmware.

1.2.8 Legacy charge detection and support

EZ-PD™ PMG1-B1 implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging, Qualcomm quick charge 2.0/3.0/4.0/5.0, and Samsung AFC protocols.

1.2.9 VBUS to CC short protection

CC pins have integrated protection from accidental shorts to high-voltage VBUS and VBAT. EZ-PD™ PMG1-B1 devices can handle up to 24 V external voltage on its CC pins without damage. In the event, an overvoltage is detected on the CC pin, it can be configured to shut down the Type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

1.3 Buck-boost subsystem

The buck-boost subsystem in EZ-PD™ PMG1-B1 devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. **Figure 1** shows the buck-boost subsystem's main external components and connections.

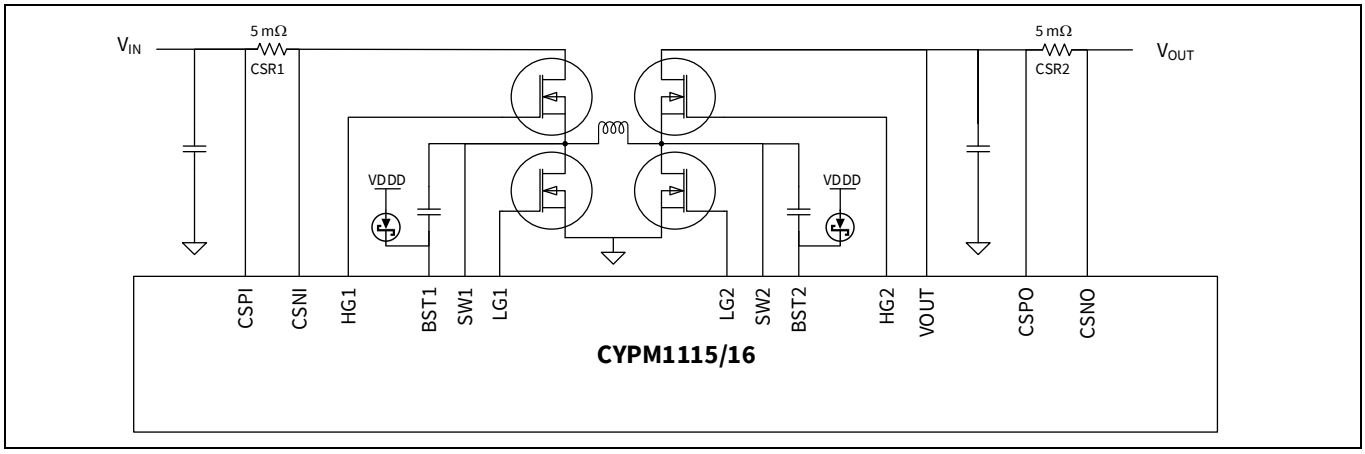

Figure 1 Buck-boost schematic showing external components

Buck-boost subsystem in EZ-PD™ PMG1-B1 devices have the following key functional blocks:

- High-side (cycle-by-cycle) CSA
- High-side and low-side gate driver
- Pulse-width modulator (PWM)
- Error amplifier (EA)

1.3.1 High-side (cycle-by-cycle) CSA

EZ-PD™ PMG1-B1 device's buck-boost controller implements peak current control in both boost and buck modes. A high-side CSA is used for peak current sensing through an external resistor (5 mΩ; see CSR1 in **Figure 1**) placed in series with the buck control FET. This CSA has a high bandwidth and a very wide common mode range. This CSR is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 1**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

1.3.2 High-side gate driver and low-side gate driver (HG/LG)

EZ-PD™ PMG1-B1' buck-boost controller provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high-side gate drivers drive the high-side external FET with a nominal VGS of 5 V. The high-side gate driver has a programmable drive strength to drive external FET. An external capacitor and schottky diode form a bootstrap network to collect and store the high voltage source (VIN + ~5 V for HG1 and VOUT + ~5 V for HG2) needed to drive the high-side FET. The low-side gate driver drives the low-side external FET with a nominal VGS of 5 V using energy sourced from EZ-PD™ PMG1-B1' internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive external FET. In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5 V) provided the VIN voltage is between 4.5 V and 24 V.

1.3.3 Error amplifier (EA)

EZ-PD™ PMG1-B1' buck-boost controller contains two EAs for output voltage and current regulation. The EA is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VOUT high-side CSA through the external resistor. The output of the VOUT CSA is compared with an internal reference in EA block and EA output is fed to the PWM block. EZ-PD™ PMG1-B1 firmware configures and controls the integrated programmable EA circuit for achieving the required VOUT voltage output from the power section.

1.3.4 Pulse-width modulator (PWM)

EZ-PD™ PMG1-B1 device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

EZ-PD™ PMG1-B1 devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: PSM and FCCM.

1.3.5 Pulse skipping mode (PSM)

In pulse skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ PMG1-B1 devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the EZ-PD™ PMG1-B1 devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

1.3.6 Forced continuous conduction mode (FCCM)

In FCCM mode, the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

1.4 Buck-boost controller operation regions

The input-side CSA's output is compared with the output of the EA to determine the pulse width of the PWM. PWM block compares the input voltage and output voltage to determine the buck, boost, and buck-boost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VIN vs VOUT thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

1.4.1 Buck region operation (VIN >> VOUT)

When the VIN voltage is significantly higher than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 2**.

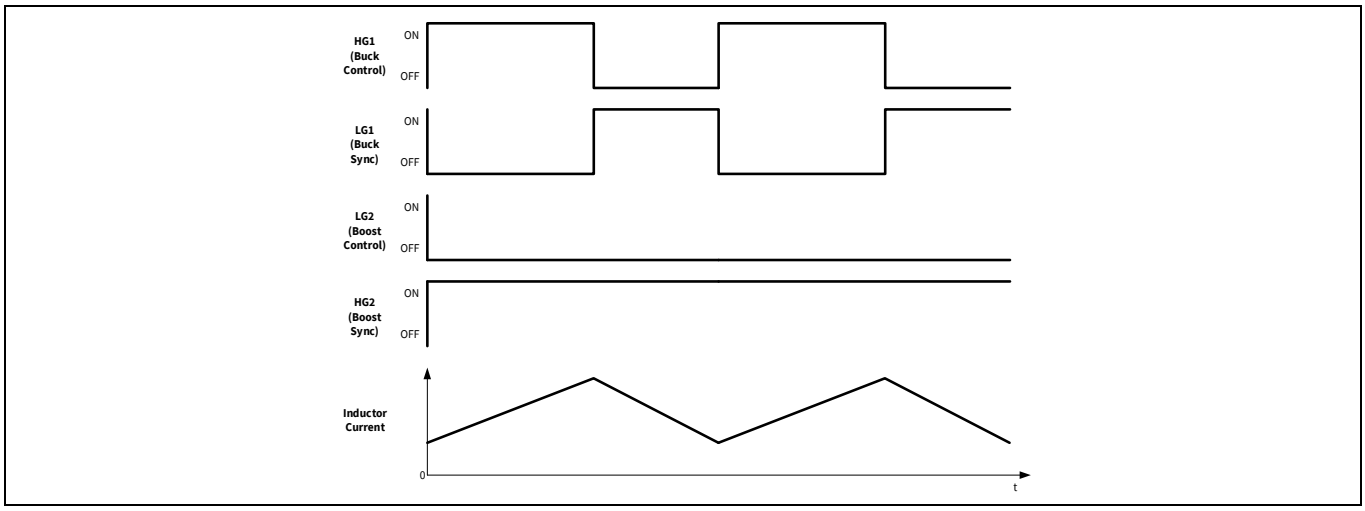

Figure 2 Buck operation waveforms

1.4.2 Boost region operation (VIN << VOUT)

When the VIN voltage is significantly lower than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 3**.

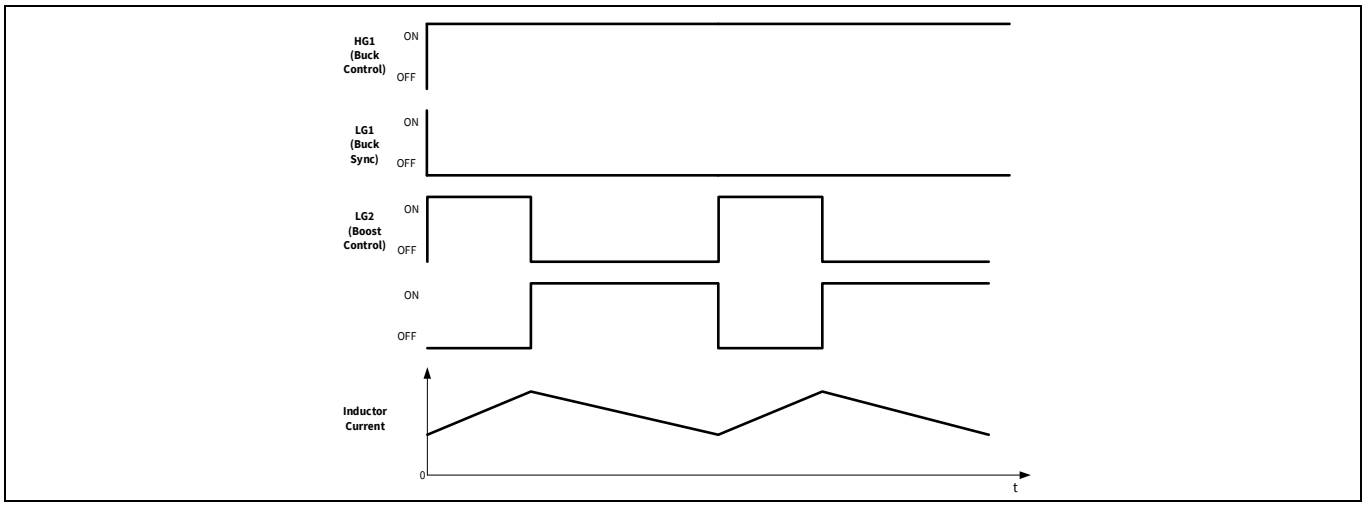

Figure 3 Boost operation waveforms

1.4.3 Buck-boost region 1 operation (VIN ~> VOUT)

When the VIN voltage is slightly higher than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck-boost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 4**.

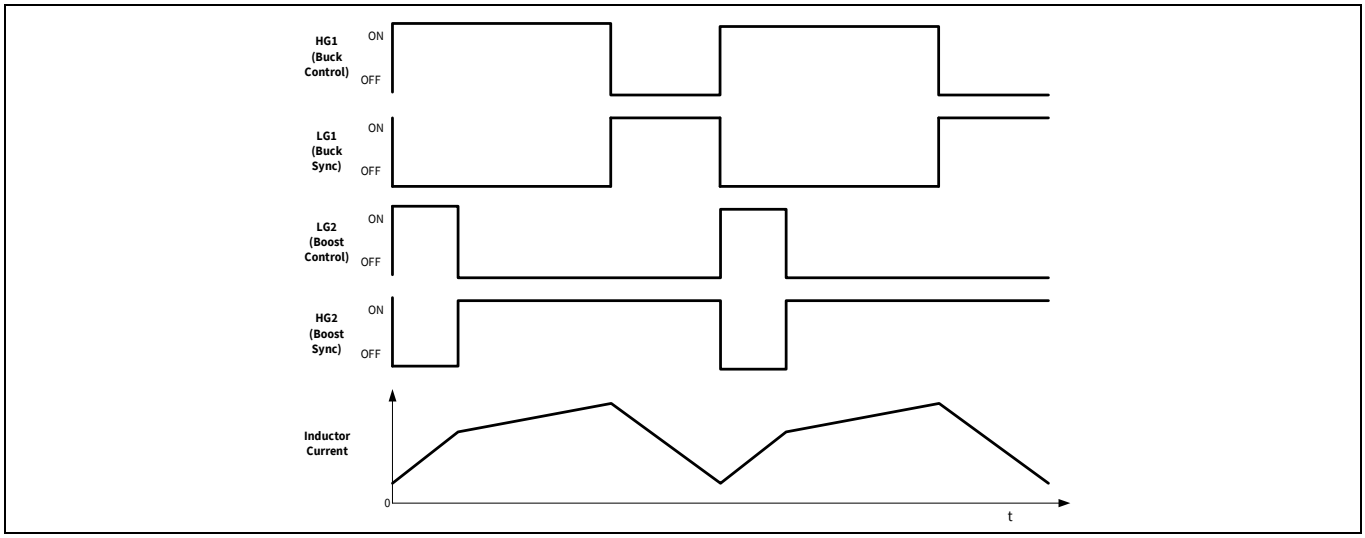

Figure 4 Buck-boost region 1 (VIN ~> VOUT) operation waveforms

1.4.4 Buck-boost region 2 operation (VIN ~< VOUT)

When the VIN voltage is slightly lower than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck-boost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 5**.

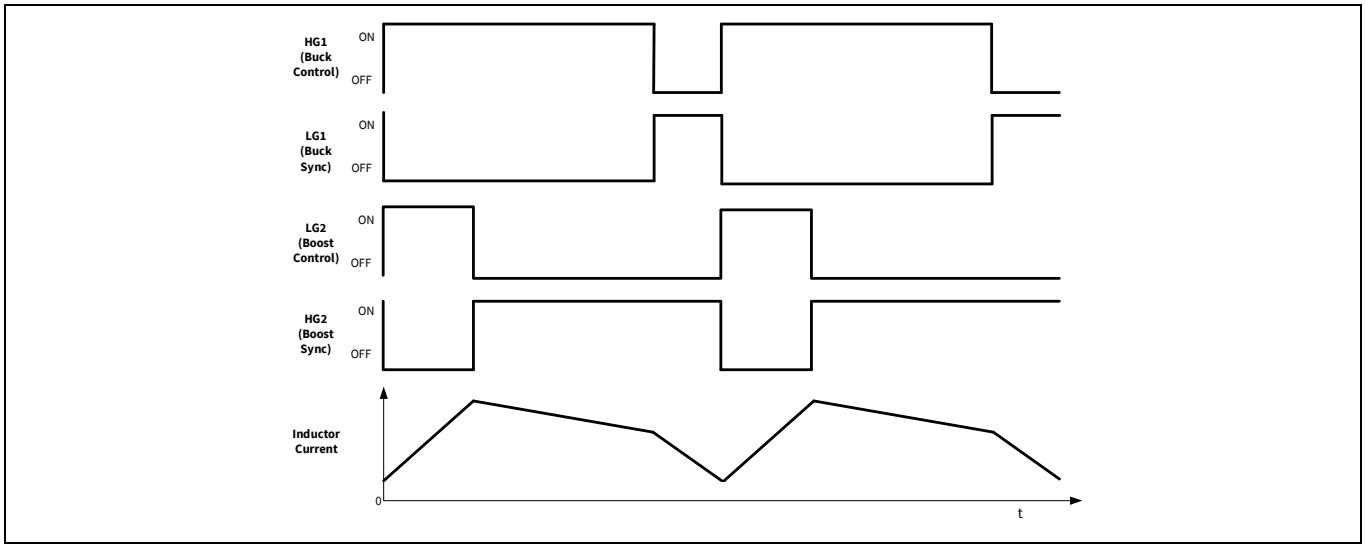

Figure 5 Buck-boost region 2 (VIN ~< VOUT) operation waveforms

1.4.5 Switching frequency and spread spectrum

EZ-PD™ PMG1-B1 devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

1.5 Analog blocks

1.5.1 ADC

EZ-PD™ PMG1-B1 devices have two 8-bit SAR ADCs and one 12-it SAR ADC. The 8-bit SAR ADCs are used for general purpose A/D conversion applications in the chip. The 12-bit SAR ADC is used for battery monitoring applications. All ADCs can be accessed from the GPIOs through an on-chip analog mux. See **Table 25** for detailed specifications of the 8-bit ADCs. See **Table 26** and **Table 27** for detailed specifications of the 12-bit ADC.

1.6 Integrated digital blocks

1.6.1 Serial communication block (SCB)

EZ-PD™ PMG1-B1 devices have three SCB blocks that can be configured for I^2C, SPI, UART or LIN. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. This I^2C implementation is compliant with the standard Philips I^2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C port I/Os for SCB0 are overvoltage tolerant (OVT). The I^2C ports for SCB1-2 are not OVT tolerant.

1.6.2 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ PMG1-B1 devices support eight timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

1.7 I/O subsystem

The EZ-PD™ PMG1-B1 devices have 21 GPIOs including the I^2C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight output drive modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control
- OVT on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed in order to reduce internal multiplexing complexity. Data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves.
The configuration of the pins can be done by the programming of registers through software for each digital I/O port. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the high-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

1.8 System resources

1.8.1 Watchdog timer (WDT)

EZ-PD™ PMG1-B1 devices have a WDT running from the internal low-speed oscillator (ILO). This allows watchdog operation during Deep Sleep and generate a watchdog reset (WDR) if not serviced before the timeout occurs. The WDR is recorded in the Reset Cause register.

1.8.2 Reset

EZ-PD™ PMG1-B1 devices can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is preserved through reset and allows application firmware to determine the cause of the reset. XRES pin is the dedicated pin for asserting an external hardware reset.

1.8.3 Clock system

EZ-PD™ PMG1-B1 devices have a fully integrated clock with no external crystal required. EZ-PD™ PMG1-B1 device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N = Divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In **Figure 6**, PERXYZ_CLK represents the clocks for different peripherals.

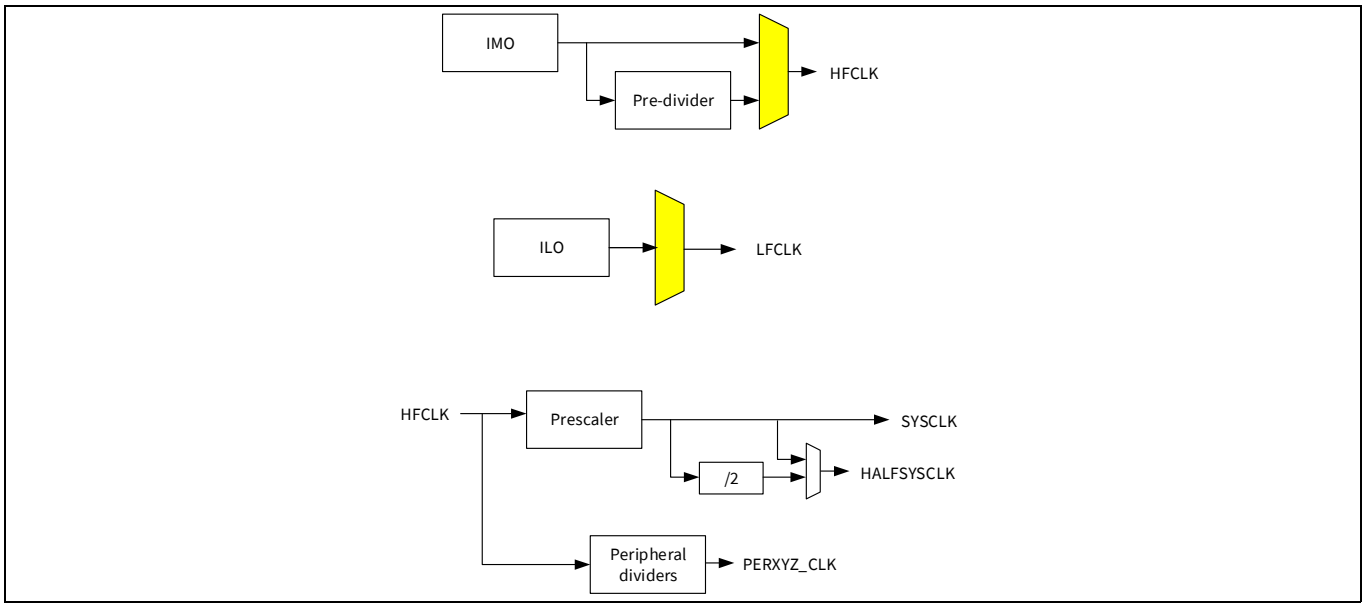

Figure 6 Clocking architecture of EZ-PD™ PMG1-B1 devices

1.8.4 Internal main oscillator (IMO) clock source

The IMO is the primary source of internal clocking in EZ-PD™ PMG1-B1 devices. IMO default frequency for EZ-PD™ PMG1-B1 devices is 48 MHz±2%.

1.8.5 ILO clock source

The ILO is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB Suspend (Deep Sleep) mode.

2 Power subsystem

Figure 7 shows an overview of the power subsystem architecture for EZ-PD™ PMG1-B1 devices. The power subsystem of EZ-PD™ PMG1-B1 devices operate from VIN supply which can vary from 4 to 24 V. The V_{DDD} pin, the output of an internal 5 V LDO, gets input from V_{IN} supply. When input supply to the IC is from CSN0, the standby regulator provides 3 V to V_{DDD}. The current capability of the V_{DDD} pin is up to 75 mA including internal as well as external loads (applicable only if supply is from V_{IN}). EZ-PD™ PMG1-B1 devices have two different power modes: Active and Deep Sleep, transitions between which are managed by the power system. The V_{CCD} pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-µF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.

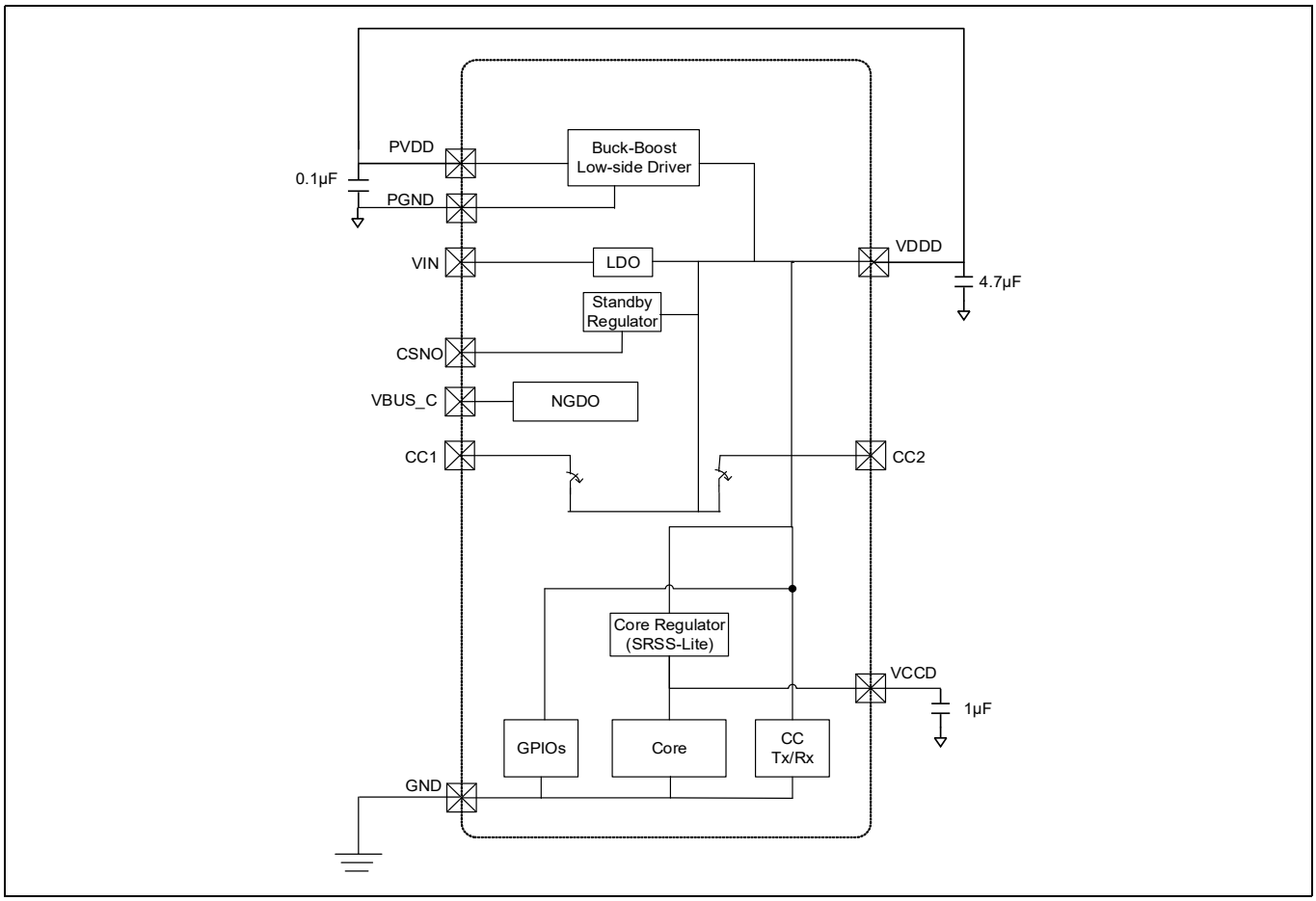

Figure 7 Power system requirement block diagram[1]

Note
1. It is recommended to tie PGND and GND together in the layout for better EMI performance.

2.1 VIN under-voltage lockout (UVLO)

EZ-PD™ PMG1-B1 supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

2.2 Using external VDDD supply

By default, external VDDD is not supported for EZ-PD™ PMG1-B1 devices. However, usage of external VDDD supply can be enabled using firmware. The prerequisite for enabling external forcing of VDDD is to always maintain VIN higher than VDDD.

2.3 Power modes

The power modes of the device accessible and observable by the user are listed in **Table 1**.

Table 1 Power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep controller is sequencing the system out of reset
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.
XRES	Power is valid and XRES is asserted. Core is powered down.

3 Pin list

Table 2 48-QFN package pinout

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
1	BST1	–	PVDD+0.5[2, 3]	Boosted power supply of the buck high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1. Also, connect a bootstrap capacitor from this pin to SW1.
2	HG1	-0.5		Buck high-side gate driver output. Connect to the buck (input) side control (high-side) FET gate. Use a wide trace to minimize inductance of this connection. Absolute min and max are with respect to SW1 pin.
3	SW1	-0.7	35	Negative power rail of the buck high-side gate driver. This is also connected to one input terminal of ZCD of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
4	LG1	-0.5	PVDD+0.5[2]	Buck low-side gate driver output. Connect to the buck (input) side sync (low-side) FET gate. Use a wide trace to minimize inductance of this connection.
5	PGND	-0.3	0.3	Ground of low-side gate driver. This is also connected to one input terminal of ZCD of buck low-side gate driver. Connect directly to the port's board ground plane.
6	PVDD	–	VDDD	Supply of low-side gate driver. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ PMG1-B1 IC as possible.
7	LG2	-0.5	PVDD+0.5[2]	Boost low-side gate driver output. Connect to the boost (output) side control (low-side) FET gate. Use a wide trace to minimize inductance of this connection.
8	VOUT	-0.3	24	Output of the buck-boost converter. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the boost sync (high-side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
9	SW2			Negative power rail of the boost high-side gate driver. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
10	HG2	-0.5	PVDD+0.5[2]	Boost high-side gate driver output. Connect to the boost (output) side sync (high-side) FET gate. Use a wide trace to minimize inductance of this connection.
11	BST2	–		Boosted power supply of the boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from V_{DDD} to BST2. Also, connect a bootstrap capacitor from this pin to SW2.
12	VBUS_CTRL	-0.5	32	VBUS NFET gate driver output. Connect to the provider NFET's gate.
13	COMP		PVDD+0.5[2]	EA output pin. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
14	VBUS_C	-0.3	24	Type-C connector VBUS voltage. Connect to the Type-C connector's VBUS pin.
15	VOUT_EA			Input of feedback voltage of EA from converter output
16	CSNO			Negative input of output current sensing amplifier. Connect to negative terminal of the output current sense resistor.
17	CSPO			Positive input of output CSA. Connect to positive terminal of the output current sense resistor.

Notes
2. Max voltage must not exceed 6 V.
3. Max absolute voltage w.r.t GND must not exceed 40 V.

Table 2 48-QFN package pinout *(continued)*

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
18	CC2	-0.5	24	Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's Type-C connector. Also, connect a 390-pF capacitor to ground.
19	CC1			Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's Type-C connector. Also, connect a 390-pF capacitor to ground.
22	VDDD	–	6	5-V LDO output. Connect a 1-µF ceramic bypass capacitor to this pin.
40	XRES	-0.5	PVDD+0.5[2]	External reset – active low. Contains a 3.5-kΩ to 8.5-kΩ internal pull-up.
43	GND	–	–	Chip ground. Connect to the exposed pad (EPAD).
44	VDDD		6	5-V LDO output. Connect a 10-µF bypass capacitor to this pin.
45	VCCD		–	1.8-V core LDO output. Connect a 0.1-µF bypass capacitor to ground. Do not connect anything else to this pin.
46	VIN	-0.3	40	4 to 24 V input supply. Connect a ceramic bypass capacitor to GND close to this pin.
47	CSPI			Positive input of input CSA. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
48	CSNI			Negative input of input CSA. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
-	EPAD	–	–	Exposed ground pad. Connect directly to pin 36 and pin 22.

Notes
2. Max voltage must not exceed 6 V.
3. Max absolute voltage w.r.t GND must not exceed 40 V.

Table 3 GPIO ports, pins and their functionality

48-QFN		SCB function			Analog	TCPWM			Fault indicator
Pin#	GPIO #	UART	SPI	I2C		ACT#0	ACT#1	ACT#3	
20	DP_GPIO0	–	–	–	–	–	–	–	–
21	DM_GPIO1	–	–	–	–	–	–	–	–
23	GPIO2	–	–	–	–	tcpwm0_line	tcpwm.tr_compare_match[0]:0	tcpwm.tr_in[0]	–
24	GPIO3	–	–	–	–	tcpwm.line[1]:0	tcpwm.tr_compare_match[1]:0	tcpwm.tr_in[1]	–
25	GPIO4	–	–	–	–	tcpwm.line[2]:0	tcpwm.tr_compare_match[2]:0	tcpwm.tr_in[2]	usbpd. fault_gpio0
26	GPIO13	–	–	–	–	tcpwm.line[0]:1	tcpwm.tr_compare_match[0]:1	tcpwm.tr_in[3]	–
27	GPIO14	–	–	–	–	tcpwm.line[1]:1	tcpwm.tr_compare_match[1]:1	tcpwm.tr_in[4]	–
28	GPIO15	–	–	–	–	tcpwm.line[2]:1	tcpwm.tr_compare_match[2]:1	tcpwm.tr_in[5]	–
29	GPIO16	scb[2].uart_cts:0	–	–	–	tcpwm.line[6]:1	tcpwm.tr_compare_match[6]:1	-	–
30	GPIO17	scb[2].uart_rts:0	–	–	sarmux_7	tcpwm.line[5]:1	tcpwm.tr_compare_match[5]:1	-	–
31	GPIO18	scb[2].uart_rx:0	–	–	sarmux_6	tcpwm.line[4]:1	tcpwm.tr_compare_match[4]:1	-	–
32	GPIO19	scb[2].uart_tx:0	–	–	sarmux_5	tcpwm.line[3]:1	tcpwm.tr_compare_match[3]:1	–	–
33	GPIO5	scb[1].uart_rts:0	scb[1].spi_select0:0	–	sarmux_4	tcpwm.line[7]:0	tcpwm.tr_compare_match[7]:0	tcpwm.tr_in[7]	usbpd. fault_gpio1
34	GPIO6	scb[1].uart_rx:0	scb[1].spi_clk:0	scb[1].i2c_scl:0	sarmux_3	tcpwm.line[6]:0	tcpwm.tr_compare_match[6]:0	–	–
35	GPIO7	scb[1].uart_tx:0	scb[1].spi_miso:0	scb[1].i2c_sda:0	sarmux_2	tcpwm.line[5]:0	tcpwm.tr_compare_match[5]:0	–	–
36	GPIO8	scb[0].uart_rts:0	scb[0].spi_select0:0	scb[2].i2c_scl:0	sarmux_1	tcpwm.line[4]:0	tcpwm.tr_compare_match[4]:0	–	–
37	GPIO9	scb[0].uart_cts:0	scb[0].spi_mosi:0	scb[2].i2c_sda:0	sarmux_0	tcpwm.line[3]:0	tcpwm.tr_compare_match[3]:0	–	–
38	GPIO10	scb[1].uart_cts:0	scb[0].spi_miso:0	–	–	–	–	tcpwm.tr_in[6]	–
39	GPIO20	–	–	–	–	tcpwm.line[7]:1	tcpwm.tr_compare_match[7]:1	–	–
41	GPIO11	scb[0].uart_tx:0	scb[1].spi_mosi:0	scb[0].i2c_sda:0	–	–	–	–	–
42	GPIO12	scb[0].uart_rx:0	scb[0].spi_clk:0	scb[0].i2c_scl:0	–	srss.ext_clk:0	–	–	–

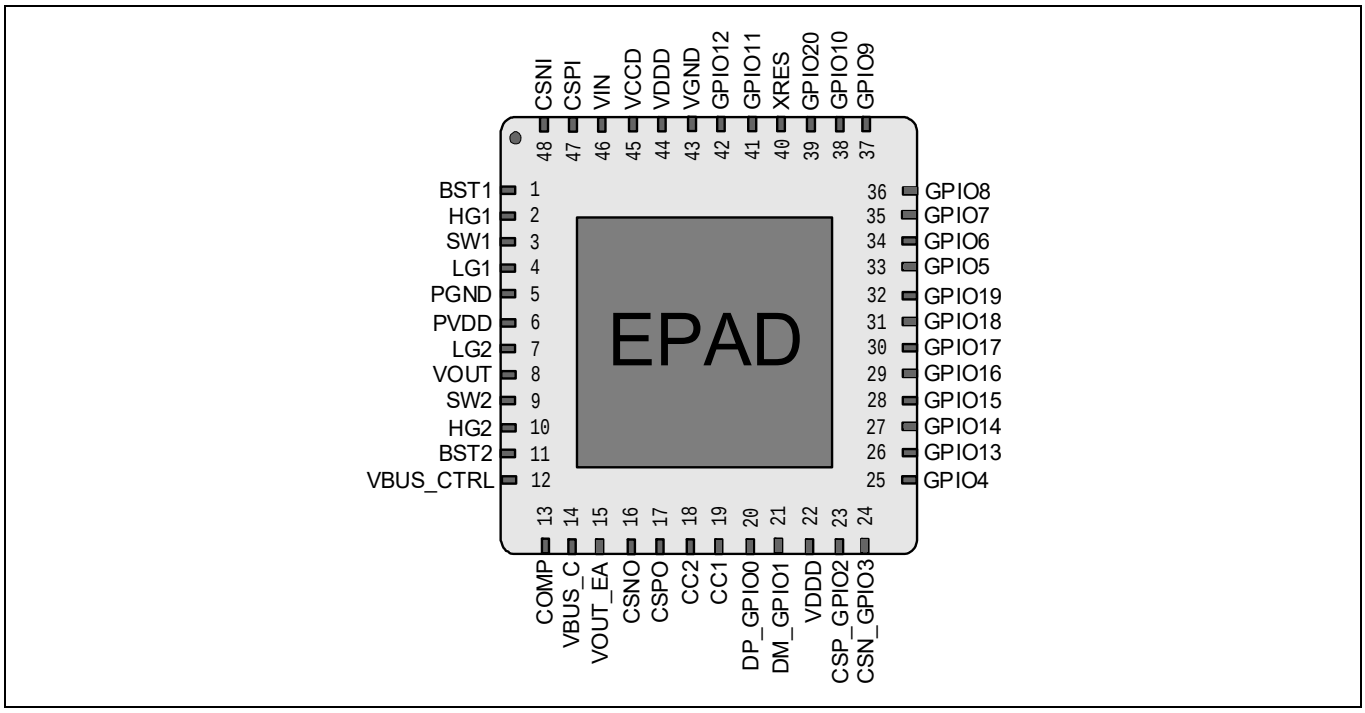

Figure 8 48-QFN pinout

4 EZ-PD™ PMG1-B1 programming

Program the application firmware into a EZ-PD™ PMG1-B1 device by programming the device flash over SWD interface.

4.1 Programming the device flash over SWD interface

The EZ-PD™ PMG1-B1 family of devices can be programmed using the SWD interface. Infineon provides programming hardware called **CY8CKIT-005 MiniProg4 kit**, which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a *hex* file.

As shown in the block diagram in **Figure 9**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pins of EZ-PD™ PMG1-B1 device. If the EZ-PD™ PMG1-B1 device is powered using an onboard power supply, it can be programmed using the "reset programming" option. For more details, refer the **CCGx (CYPDxxxx) programming specifications**.

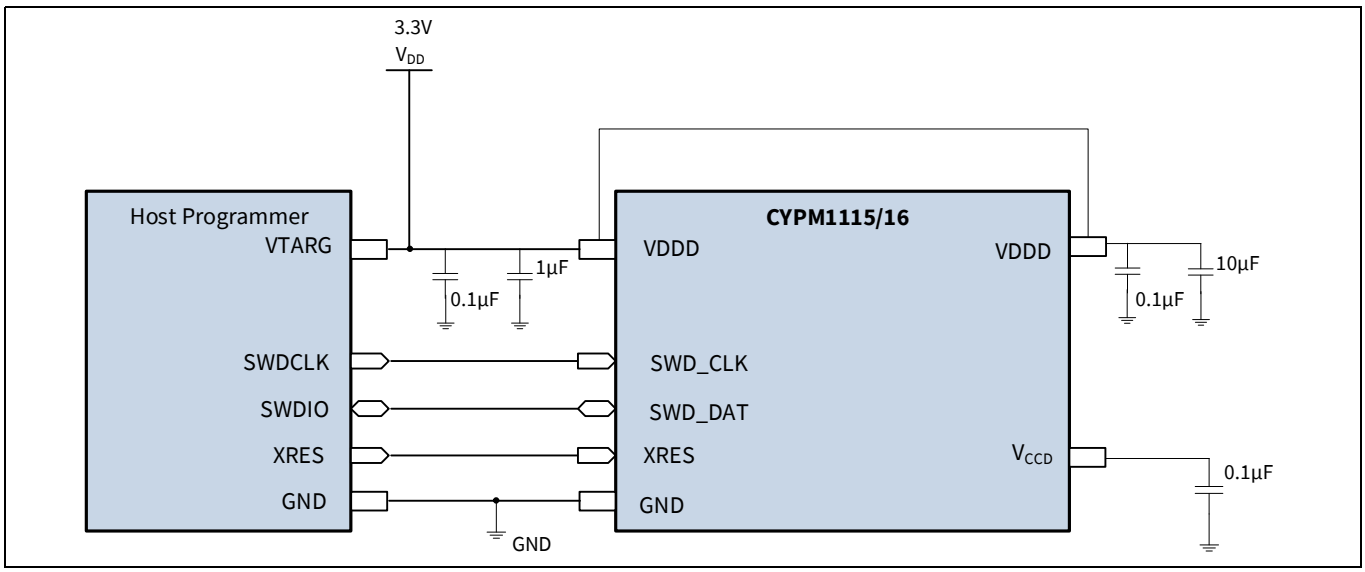

Figure 9 Connecting the programmer to CYPM1115/16 device

5 Applications

Figure 10 shows a typical power tool sink application block diagram using the EZ-PD™ PMG1-B1 device. In this application, EZ-PD™ PMG1-B1 is always in DRP role supporting the charging of the sink. It negotiates the power with the connected sink and uses the integrated buck-boost controller to supply the required voltage and current.

EZ-PD™ PMG1-B1 measures various temperatures using external NTC thermistors. EZ-PD™ PMG1-B1 throttles the output power based on temperature and/or shuts off the power under critical conditions. It also monitors the battery voltage and lowers the output power if the battery voltage is lower than the user-configured threshold. When no load is connected to the USB Type-C port, EZ-PD™ PMG1-B1 remains in standby mode without switching on the buck-boost controller.

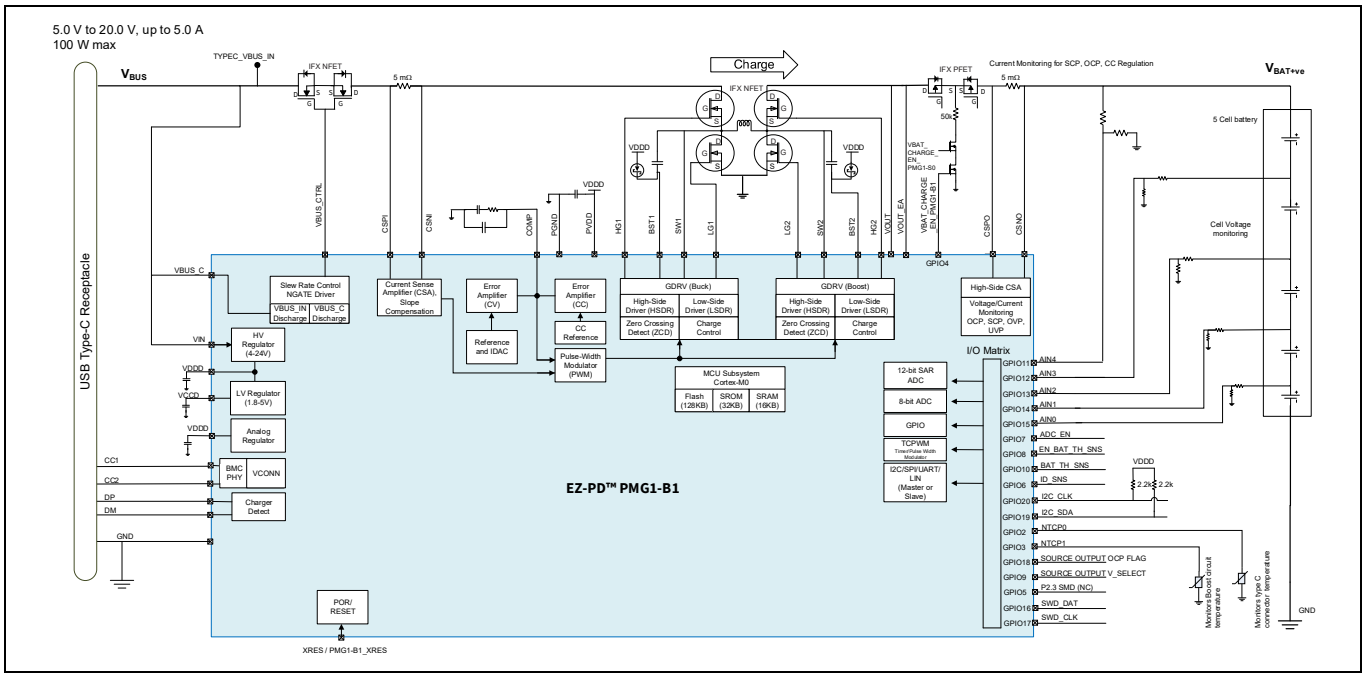

Figure 10 EZ-PD™ PMG1-B1 battery pack charging solution diagram

6 Electrical specifications

6.1 Absolute maximum ratings

Table 4 Absolute maximum ratings[5]

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{IN_MAX}	Maximum input supply voltage	–	–	40	V	–
V_{DDD_MAX}	Maximum supply voltage relative to V_{SS}			6		
V_{5V_MAX}	Maximum supply voltage relative to V_{SS}					
$V_{BUS\_C\_MAX}$	Max V_{BUS_C} (P0/P1) voltage relative to V_{SS}			24		
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins					
V_{GPIO_ABS}	Inputs to GPIO	–0.5		V_{DDD} + 0.5		
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage			6		
I_{GPIO_ABS}	Maximum current per GPIO	–25		25	mA	
$I_{GPIO\_INJECTION}$	GPIO injection current, max for $V_{IH} > V_{DDD}$, and min for $V_{IL} < V_{SS}$	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2000		–	V	All pins
ESD_CDM	Electrostatic discharge charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
T_J	Junction temperature	–40		125	°C	

Note
4. The standard compliance will not be performed on this demonstration hardware. Customers are responsible for their final end product compliance.
5. Usage above the absolute maximum conditions listed in **Table 5** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 3.0 to 5.5 V except where noted.

6.2.1 DC specifications

Table 5 DC Specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{IN}	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	V_{IN_BB}	Buck-boost operating input supply voltage	4.5				
SID.PWR#2	V_{DDD_REG}	VDDD output with VIN 5.5 to 24 V, max load = 75 mA	4.6		5.5		
SID.PWR#2A	V_{DDD_BYPASS}	VDDD output with VIN 4.5 to 5.5 V, max load = 75 mA	V_{IN} -0.7				
SID.PWR#3	V_{DDD_MIN}	VDDD output with VIN 4 to 4.5 V, max load = 20 mA	V_{IN} - 0.2		–		
SID.PWR#20	VBUS	VBUS_C valid range	3.3		21.5		
SID.PWR#5	V_{CCD}	Regulated output voltage (for core logic)	–	1.8	–		
SID.PWR#16	C_{EFC_VCCD}	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic
SID.PWR#17	C_{EXC_VDDD}	Power supply decoupling capacitor for V_{DDD}	–	10	–	µF	
SID.PWR#18	C_{EXV}	Bootstrap supply capacitor (BST1, BST2)		0.1			
SID.PWR#24	I_{DD_ACT}	Supply current at 0.4 MHz switching frequency		50		mA	T_A = 25°C, VIN = 12 V. CC IO IN transmit or receive, no I/O sourcing current, No VCONN load current, CPU at 24 MHz, PD port active. Buck-boost converter on, 3-nF gate driver capacitance.
Deep Sleep mode							
SID_DS1	I_{DD_DS1}	V_{IN} = 12 V. CC wakeup on, Type-C not connected, Source mode.	–	80	–	µA	Type-C not attached, CC enabled for wakeup. R_p connection should be enabled for the PD port. T_A = 25°C.
SID_DS2	I_{DD_DS2}	V_{IN} = 12 V, GPIO wake-up		50			USBPD disabled. Wake-up from GPIO. T_A = 25°C. All faults disabled.

6.2.2 CPU

Table 6 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.PWR#19	$T_{DEEPSLEEP}$	Wake-up from Deep Sleep mode		35	–	µs	–
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–			
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to Accept I^2C/CC command”	–	5	25	ms	

6.2.3 GPIO

Table 7 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	V_{IH_CMOS}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage low threshold	–		0.3 × V_{DDD}		
SID.GIO#11	V_{IH_TTL}	LVTTL input	2.0		–		–40°C ≤ TA ≤ +105°C
SID.GIO#12	V_{IL_TTL}	LVTTL input	–		0.8		
SID.GIO#7	V_{OH_3V}	Output voltage high level	V_{DDD} – 0.6		–		I_{OH} = –4 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#8	V_{OL_3V}	Output voltage low level	–		0.6		I_{OL} = 10 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–40°C ≤ T_A ≤ +105°C
SID.GIO#3	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDD}
SID.GIO#5	C_{PIN_A}	Max pin capacitance			22	pF	–40°C ≤ T_A ≤ +105°C, capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance		3	7		–40°C ≤ T_A ≤ +105°C, all V_{DDD}, all other I/Os
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, V_{DDD} > 2.7 V	100	–	–	mV	V_{DDD} > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × V_{DDD}				–

Table 8 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#16	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	C_{load} = 25 pF, –40°C ≤ T_A ≤ +105°C
SID.GIO#17	T_{FALLF}	Fall time in fast strong mode					
SID.GIO#18	T_{RISES}	Rise time in slow strong mode	10		60		
SID.GIO#19	T_{FALLS}	Fall time in slow strong mode					
SID.GIO#20	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.			7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ V_{DDD} ≤ 5.5 V.			16		–40°C ≤ T_A ≤ +105°C

Table 9 GPIO OVT DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	-140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5		8.5	kΩ	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value			8.5		
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	VDDD-0.6		–	V	I_{OH} = -4 mA
SID.GPIO_20VT_GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	–		0.6		I_{OL} = 8 mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input	–		0.8		
SID.GPIO_20VT_GIO#43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100		–	mV	
SID.GPIO_20VT_GIO#45	GPIO_20VT_ITOT_GPIO	GPIO_20VT maximum total sink pin current to ground	–		95	mA	V (GPIO_20VT pin) > V_{DDD}

Table 10 GPIO OVT AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in fast strong mode	1	–	15	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in fast strong mode					
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in slow strong mode	10		70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT fall time in slow strong mode					
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–		33	MHz	
SID.GPIO_20VT_GIO#50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V≤V_{DDD}≤5.5V. Slow strong mode.			7		
SID.GPIO_20VT_GIO#52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V			8		All V_{DDD}

6.2.4 XRES

Table 11 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH_XRES}	Input voltage high threshold on XRES pin	0.7 × V_{DDD}	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage low threshold on XRES pin	–		0.3 × V_{DDD}		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin			7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin		0.05 × V_{DDD}	–	mV	

6.3 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the timer mode.

6.3.1 Pulse-width modulation (PWM) for GPIO pins

Table 12 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc		–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.4	T_{CRES}	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5	PWM_{RES}	PWM resolution					Minimum pulse width of PWM output

6.3.2 I^2C

Table 13 Fixed I^2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.3.3 UART

Table 14 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

6.3.4 SPI

Table 15 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 16 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20		–		Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0				Referred to slave capturing edge

Table 17 Fixed SPI slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–		48 + (3 × T_{CPU})		$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in ext clk mode			48		–
SID172	T_{HSO}	Previous MISO data hold time	0		–		
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100				

6.3.5 Memory

Table 18 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (Erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ +85°C, all V_{DDD}
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)			35		–
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	FLASH_ENPB	Flash write endurance	100k		–	cycles	25°C ≤ T_A ≤ 55°C, all V_{DDD}
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10				

6.4 System resources

6.4.1 Power-on-reset (POR) with brown out

Table 19 Imprecise power-on reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–40°C ≤T_A ≤ +105°C, all V_{DDD}
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70		1.4		

Table 20 Precise POR

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in Active/Sleep modes	1.48	–	1.62	V	–40°C ≤T_A ≤ +105°C, all V_{DDD}
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1		1.5		

6.4.2 SWD interface

Table 21 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.0 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	–
SID.SWD#3	T_SWDI_HOLD						
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		

6.4.3 Internal main oscillator

Table 22 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	3.0 V ≤ V_{DDD} < 5.5 V. –40°C ≤ T_A ≤ 105°C
SID226	$T_{STARTIMO}$	IMO start-up time			7	µs	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.CLK#1	F_{IMO}	IMO frequency	24		48	MHz	

6.4.4 Internal low-speed oscillator

Table 23 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO start-up time	–	–	2	ms	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID238	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

6.4.5 PD

Table 24 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage	–		0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	W	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10			MΩ	
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64		96	µA	
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	166		194		
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	304		356		
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108				
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-standard USB	0.15		0.25	V	
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35		0.45		
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75		0.85		
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45		2.75		
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-standard USB	0.61		0.7		
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep Sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

6.4.6 Analog-to-digital converter

Table 25 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap.
SID.ADC.3	DNL	Differential non-linearity	–2.5		2.5		Reference voltage generated from V_{DDD}.
SID.ADC.4	Gain Error	Gain error	–1.5		1.5		Reference voltage generated from bandgap.
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}		V_{DDDmax}	V	Reference voltage generated from V_{DDD}.
SID.ADC.6	VREF_ADC2		1.96	2.0	2.04		Reference voltage generated from Deep Sleep reference.

Table 26 12-bit SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC12.DC.2	A_RES_1	Resolution	–	–	12	bits	IMO/HFCLK at 48 MHz
SID.ADC12.DC.3	A_CHNLS_S	Number of channels - single ended			8		8 full speed
SID.ADC12.DC.4	A-CHNKS_D	Number of channels - differential			4		Differential inputs use adjacent I/O.
SID.ADC12.DC.5	A-MONO	Monotonicity			–		Yes
SID.ADC12.DC.6	A_GAINERR	Gain error			±0.1	%	With external reference.
SID.ADC12.DC.7	A_OFFSET	Input offset voltage			2	mV	Measured with 1 V reference.
SID.ADC12.DC.8	A_ISAR	Current consumption			1	mA	–
SID.ADC12.DC.9	A_VINS	Input voltage range - single ended	V_{SS}		V_{DDD}	V	
SID.ADC12.DC.10	A_VIND	Input voltage range - differential					
SID.ADC12.DC.11	A_INRES	Input resistance	–		2.2	kΩ	
SID.ADC12.DC.12	A_INCAP	Input capacitance			10	pF	

Table 27 12-bit SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC12.AC.1	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID.ADC12.AC.2	A_CMRR	Common mode rejection ratio	66				Measured at 1 V.
SID.ADC12.AC.3	A_SAMP_1	Sample rate with external reference bypass cap.	–		1	Msps	–
SID.ADC12.AC.4	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}.			500	Ksps	
SID.ADC12.AC.5	A_SAMP_3	Sample rate with no bypass cap. Internal reference.			100		
SID.ADC12.AC.6	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65		–	dB	Fin = 10 kHz
SID.ADC12.AC.7	A_BW	Input bandwidth without aliasing	–		A_samp/2	kHz	–
SID.ADC12.AC.8	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	-1.7		2	LSB	Vref = 1 to V_{DD}
SID.ADC12.AC.9	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	-1.5		1.7		Vref = 1.71 to V_{DD}
SID.ADC12.AC.10	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps					Vref = 1 to V_{DD}

6.4.7 HS CSA

Table 28 HS CSA DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.1	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.HSCSA.2	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10		10		
SID.HSCSA.3	Csa_Acc3	CSA accuracy 15 mV < Vsense < 25 mV	–5		5		
SID.HSCSA.4	Csa_Acc4	CSA accuracy 25 mV < Vsense	–3		3		
SID.HSCSA.7	Csa_SCP_Acc1	CSA SCP at 6A with 5-mΩ sense resistor	–10		10		
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10A with 5-mΩ sense resistor					
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1A with 5-mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5-mΩ sense resistor	123		137		

Table 29 HS CSA AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3 nF NFET gate

6.4.8 UV/OV

Table 30 UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold accuracy, 4 to 11 V	–3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold accuracy, 11 to 21.5 V	–3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold accuracy, 3 to 3.3 V	–4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold accuracy, 3.3 to 4.0 V	–3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold accuracy, 4.0 to 21.5 V	–3		3		

6.4.9 VCONN switch

Table 31 VCONN switch DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.VCONN.1	VCONN_OUT	VCONN output voltage with 20 mA load current	4.5	–	5.5	V	–
DC.VCONN.2	I_{LEAK}	Connector side pin leakage current	–		10	µA	
DC.VCONN.3	I_{OCP}	VCONN overcurrent protection threshold	22.5	30	42.5	mA	

Table 32 VCONN switch AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	600	µs	–
AC.VCONN.2	T_{OFF}	VCONN switch turn-off time			10		

6.4.10 V_{BUS}

Table 33 V_{BUS} discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	R1	20-V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V.
SID.VBUS.DISC.2	R2	20-V NMOS ON resistance for DS = 2	250		1000		
SID.VBUS.DISC.3	R4	20-V NMOS ON resistance for DS = 4	125		500		
SID.VBUS.DISC.4	R8	20-V NMOS ON resistance for DS = 8	62.5		250		
SID.VBUS.DISC.5	R16	20-V NMOS ON resistance for DS = 16	31.25		125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V.

6.4.11 Voltage regulation

Table 34 Voltage regulation DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	VOUT	CSNO output voltage range	3.3	–	21.5	V	–
SID.DC.VR.2	VR	CSNO voltage regulation accuracy	–	±3	±5	%	
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	

Table 35 Voltage regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.1	T_{START}	Total startup time for the regulator supply outputs	–	–	200	µs	–

6.4.12 VBUS gate driver

Table 36 VBUS gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on VBUS_CTRL to turn off external NFET.
SID.GD.5	GD_drv	Programmable typical gate current	0.3		9.75	µA	–

Table 37 VBUS gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.3	T_{ON}	VBUS_CTRL low to high (1V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	CSNO = 5 V
SID.GD.4	T_{OFF}	VBUS_CTRL high to low (90% to 10%) with 3 nF external capacitance	–	7	–	µs	CSNO = 21.5 V

6.4.13 PWM controller

Table 38 Buck-boost PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM.1	F_{SW}	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	
PWM.3	Ratio_buck_BB	Buck to buck boost ratio		1.16		V/V	
PWM.4	Ratio_boost_BB	Boost to buck boost ratio		0.84			

6.4.14 NFET gate driver

Table 39 Buck-boost NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DR.1	R_HS_PU	Top-side gate driver on-resistance-gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance-gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance-gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance-gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
DR.9	Tr_LS	Bottom-side gate driver rise time		25			
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

6.4.15 LS-SCP

Table 40 LS-SCP DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSSCP.DC.1	SCP_6A	Short circuit current detect @ 6A	5.4	6	6.6	A	Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.1A	SCP_6A_SE	Short circuit current detect @ 6A	4.5	6	7.5		Using single ended inputs (CSP_GPIO2) and internal ground
SID.LSSCP.DC.2	SCP_10A	Short circuit current detect @10A	9	10	11		Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.2A	SCP_10A_SE	Short circuit current detect @10A	7.5	10	12.5		Using single ended inputs (CSP_GPIO2) and internal ground

6.4.16 Thermal

Table 41 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

7 Ordering information

Table 42 lists the EZ-PD™ PMG1-B1 part numbers and features.

Table 42 EZ-PD™ PMG1-B1 ordering information

MPN	Termination resistor	Role	Switching frequency	Package type
CYPM1115-48LQXI	R_P, R_D	Sink and DRP power sourcing will be supported	150 to 600 kHz	48-pin QFN
CYPM1116-48LQXI	R_P, R_D, R_{D-DB}			

7.1 Ordering code definition

The part numbers are of the form CYPM1ABC-DEFGHIJ where the fields are defined as follows.

Table 43 EZ-PD™ PMG1-B1 ordering code definitions

Field	Description	Values	Meaning
CY	CYPRESS prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU family generation	1	Product family generation
A	Family	0	S0
		1	S1, B1
		2	S2
		3	S3
B	PD Ports	1	1-PD port
		2	2-PD port
C	Application specific	5	R_P, R_D (no dead battery support)
		6	R_P, R_D, R_{D-DB} (dead battery support)
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

8 Packaging

Table 44 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	-40	25	125	°C
T_{JA}	Package θ_{JA}		–	–	18.81	°C/W
T_{JC}	Package θ_{JC}				10.1	

8.1 Package diagram

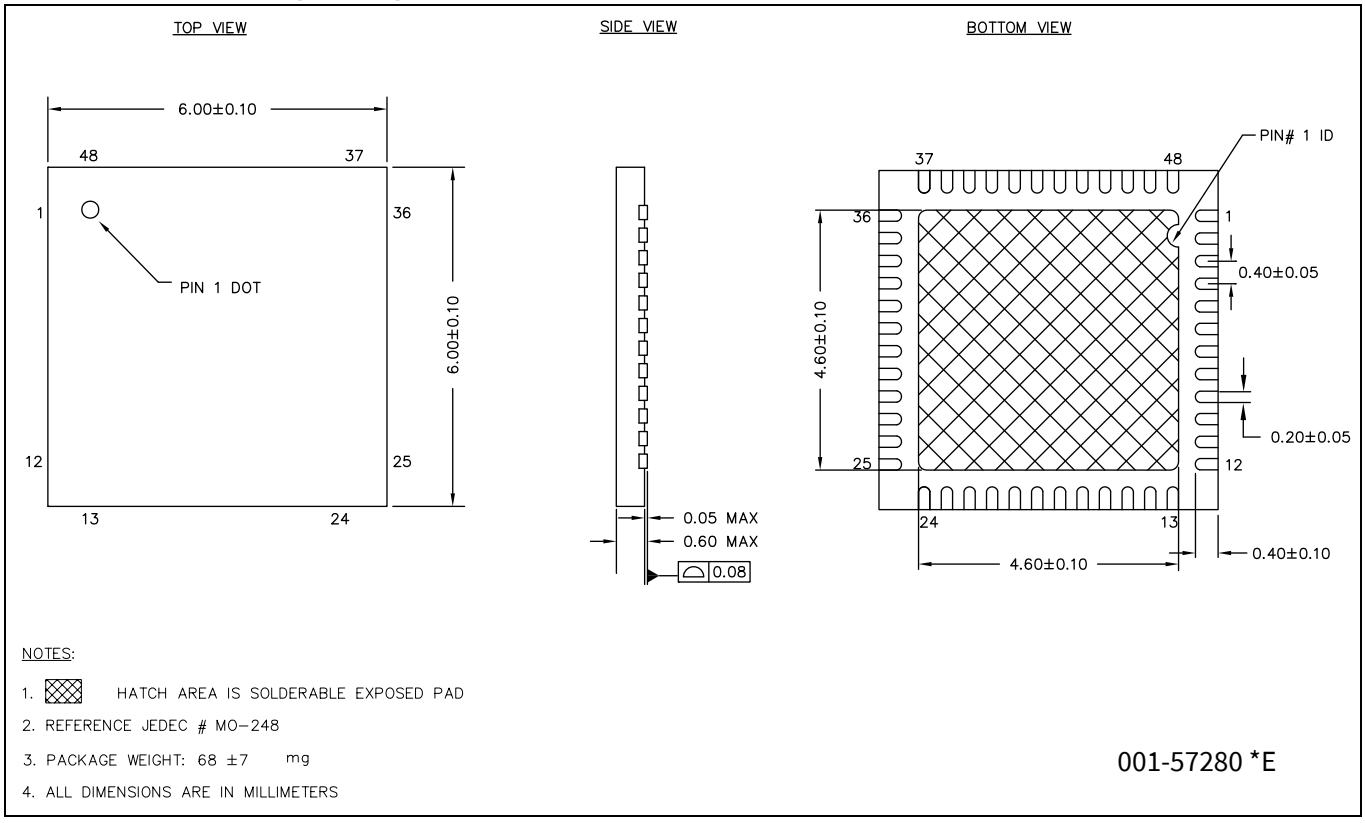

Figure 11 48-QFN package outline

9 Acronyms

Table 45 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	Samsung adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
FCCM	forced continuous current/conduction mode
GPIO	general-purpose input/output
HSDR	high-side driver
I^2C, or IIC	inter-integrated circuit, a communications protocol
IDAC	current DAC
I/O	input/output, see also GPIO
LSDR	low-side driver
MCU	microcontroller unit
OCP	overcurrent protection
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PSoC™	programmable system-on-chip
PSM	pulse skipping mode
PWM	pulse-width modulator
RAM	random-access memory
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	universal asynchronous transmitter receiver, a communications protocol
UFP	upstream facing port
UVP	undervoltage protection
USB	universal serial bus
UVLO	under-voltage lockout
VPA	VCONN powered accessories
ZCD	zero crossing detector

10 Document conventions

10.1 Units of measure

Table 46 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second

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