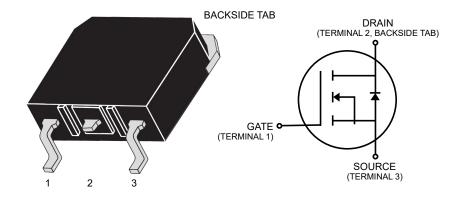
700V, 15 mΩ N-Channel mSiC[™] MOSFET

MSC015SMA070S



Product Overview

700V, 15 m Ω typical at V_{GS} = 20V, 17 m Ω typical at V_{GS} = 18V, Silicon Carbide (SiC) N-Channel MOSFET, D3PAK (TO-268).



Features

- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, T_{I(max)} = 175 °C
- · Fast and reliable body diode
- Superior avalanche ruggedness
- · RoHS compliant

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Improved thermal capabilities and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- · Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	700	V
I _D	Continuous drain current at T _C = 25 °C	112	Α
	Continuous drain current at T _C = 100 °C	94	
I _{DM}	Pulsed drain current ¹	450	
V_{GS}	Gate-source voltage	23 to -10	V
	Transient gate-source voltage	25 to -12	
P _D	Total power dissipation at T _C = 25 °C	477	W
	Linear derating factor	3.2	W/°C

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Тур.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	_	0.24	0.31	°C/W
T _J	Operating junction temperature	-55	_	175	°C
T _{STG}	Storage temperature	-55	_	150	°C
_	Reflow temperature	_	_	260	°C
Wt	Package weight	_	4.0	_	g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. $T_J = 25$ °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0V$, $I_D = 100 \mu A$	700	_	_	٧
R _{DS(on)}	Drain-source on resistance ¹	$V_{GS} = 20V, I_D = 40A$	_	15	19	mΩ
		V _{GS} = 18V, I _D = 40A	_	17	_	
V _{GS(th)}	Gate-source threshold voltage	$V_{GS} = V_{DS}$, $I_D = 4 \text{ mA}$	1.9	3.0	5.0	V
I _{DSS}	Zero gate voltage drain current	$V_{DS} = 700V, V_{GS} = 0V$	_	0.3	35	μΑ
		$V_{DS} = 700V$, $V_{GS} = 0V$, $T_{J} = 175$ °C	_	3.5	_	
I _{GSS}	Gate-source leakage current	V _{GS} = 20V/–10V	_	_	±100	nA

Note:

1. Pulse test: pulse width < 380 μ s, duty cycle < 2%.



The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified. The dynamic characteristics are characterized, not 100% tested, at the recommended operating V_{GS} = 20V/–5V.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0V	_	4324	_	pF
C _{rss}	Reverse transfer capacitance	V _{DD} = 700V	_	44	_	
C _{oss}	Output capacitance	$V_{AC} = 25 \text{ mV}$ f = 200 kHz	_	506	_	
Q _G	Total gate charge	V _{GS} = -5V/20V		215	_	nC
Q _{GS}	Gate-source charge	V _{DD} = 470V	_	58	_	
Q_{GD}	Gate-drain charge	I _D = 40A	_	35	_	
t _{d(on)}	Turn-on delay time	V _{DD} = 470V	_	25	_	ns
t _r	Voltage rise time	$V_{GS} = -5V/20V$	_	34	_	
t _{d(off)}	Turn-off delay time	I _D = 50A	_	53	_	
t _f	Voltage fall time	$R_{G(ext)} = 4\Omega$	_	20	_	
E _{on}	Turn-on switching energy	Freewheeling diode =	_	856	_	μJ
E _{off}	Turn-off switching energy	MSC015SMA070S (V _{GS} = -5V); reference Figure 1-18	_	129	_	
ESR	Gate equivalent series resistance	f = 1 MHz, 25 mV, drain short	_	0.69	_	Ω
SCWT	Short circuit withstand time	$V_{DS} = 560V, V_{GS} = 20V$	_	3.0	_	μs
E _{AS}	Avalanche energy, single pulse	I _D = 40A	_	6400	_	mJ

The following table shows the body diode characteristics of this device. T_J = 25 °C unless otherwise specified. The body diode reverse recovery is characterized, not 100% tested.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Тур.	Max.	Unit
V_{SD}	Diode forward voltage	$I_{SD} = 40A, V_{GS} = 0V$	_	3.3	_	V
		I _{SD} = 40A, V _{GS} = -5V	_	3.6	5.0	
t _{rr}	Reverse recovery time	I_{SD} = 50A, V_{GS} = –5V, Drive R_G = 4Ω , V_{DD} =	_	37	_	ns
Q _{rr}	Reverse recovery charge	470V, dI/dt = –6800 A/μs	_	631	_	nC
I _{RRM}	Reverse recovery current		_	68	_	Α

1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Drain Current vs. V_{DS} at T_{J}

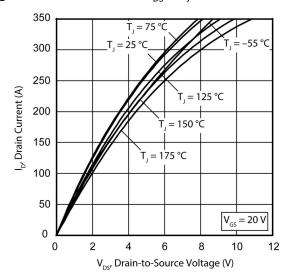


Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

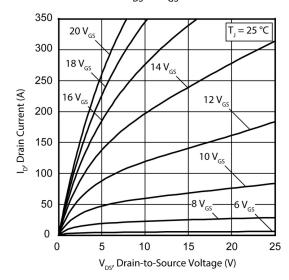


Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

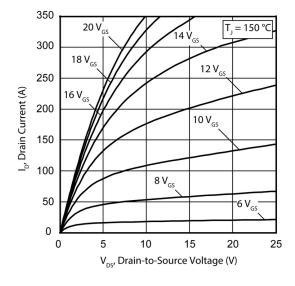


Figure 1-4. Drain Current vs. V_{DS} at V_{GS}

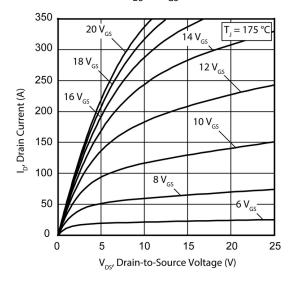


Figure 1-5. R_{DS(on)} vs. Junction Temperature

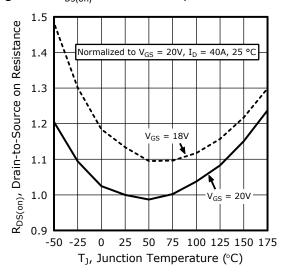


Figure 1-6. Gate Charge Characteristics

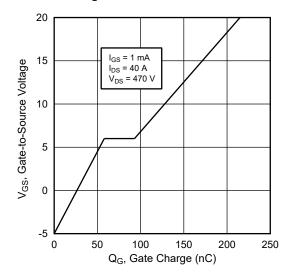


Figure 1-7. Capacitance vs. Drain-to-Source Voltage

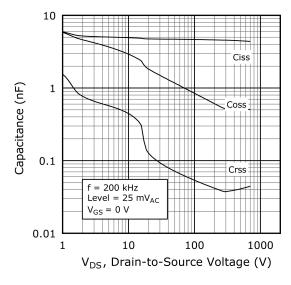


Figure 1-8. Output Charge vs. Drain-to-Source Voltage

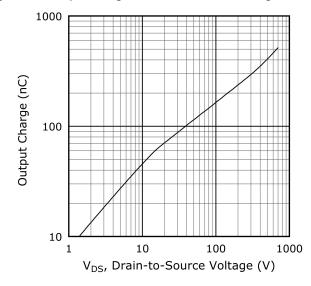


Figure 1-9. I_D vs. V_{DS} 3rd Quadrant Conduction

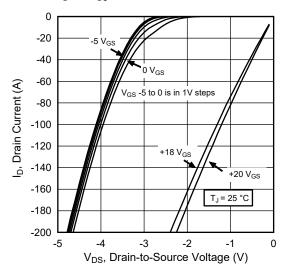


Figure 1-10. I_D vs. V_{DS} 3^{rd} Quadrant Conduction

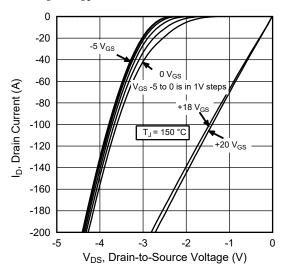


Figure 1-11. Switching Energy E_{on} vs. $V_{DS} \& I_{D}$

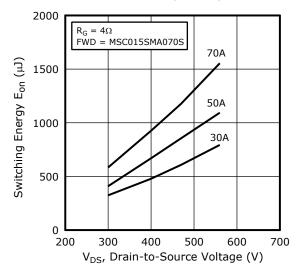


Figure 1-12. Switching Energy E_{off} vs. $V_{DS} \& I_{D}$

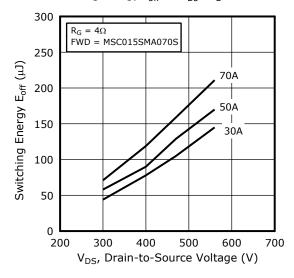


Figure 1-13. Switching Energy vs. R_G

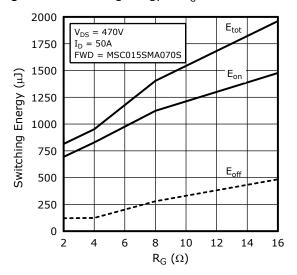


Figure 1-14. Switching Energy vs. Junction Temperature

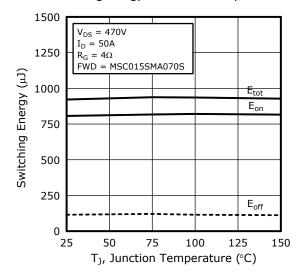
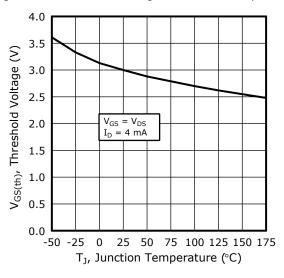


Figure 1-15. Threshold Voltage vs. Junction Temperature Figure 1-16. Forward Safe Operating Area



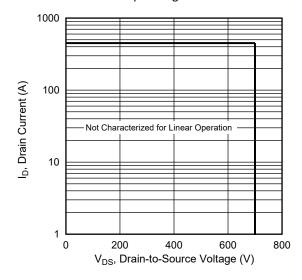
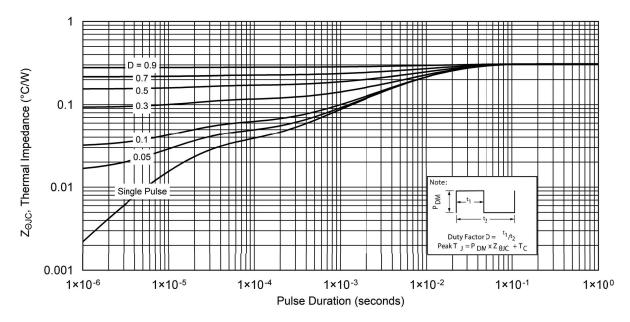
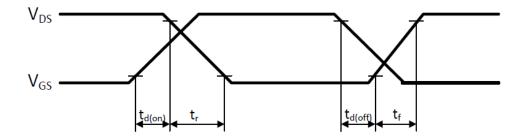


Figure 1-17. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-18. Switching Waveform



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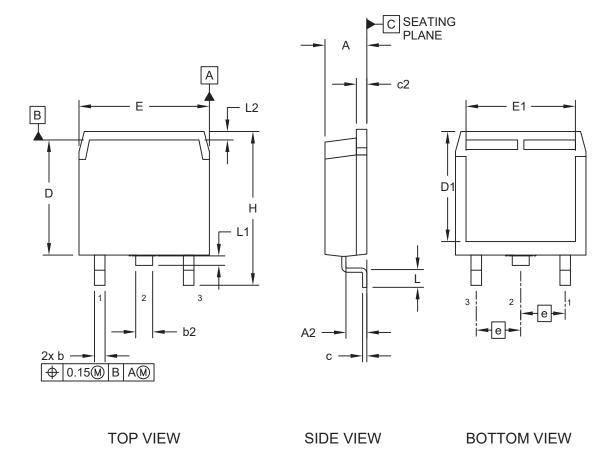
2. Package Specification

This section shows the package specification of this device.

2.1 Package Outline Drawing

The following figure illustrates the D3PAK (TO-268) package outline of this device.

Figure 2-1. Package Outline Drawing



The following table shows the D3PAK (TO-268) dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. D3PAK (TO-268) Dimensions

Symbol	Description	Min. (mm)	Max. (mm)
N	Number of leads	3	
е	Pitch	5.46 BSC	
Α	Overall height	4.90	5.11
A2	Seating plane to lead	2.69	2.90
b	Lead width	1.14	1.45
b2	Center lead width	1.96	2.21
Н	Overall package length	18.69	19.10
С	Lead thickness	0.41	0.61
c2	Tab thickness	1.45	1.60

continued				
Symbol	Description	Min. (mm)	Max. (mm)	
L	Foot length	2.39	2.69	
L1	Center lead length	0.94	1.40	
L2	Tab length	0.99	1.24	
D	Molded body length	13.79	14.00	
D1	Thermal pad length	12.40	12.70	
Е	Total width	15.85	16.21	
E1	Thermal pad width	13.31	13.59	

Note:

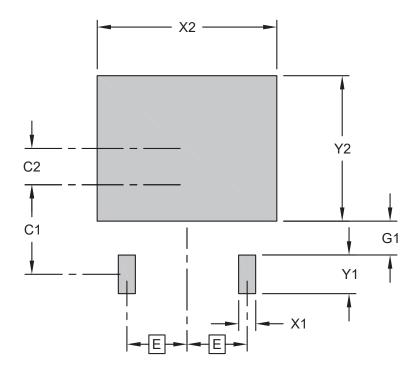
Dimensioning and tolerancing per ASME Y14.5M.

• BSC: Basic dimension. Theoretically exact value shown without tolerances.

2.2 Recommended Land Pattern

The following figure illustrates the recommended land pattern of this device.

Figure 2-2. Recommended Land Pattern



The following table shows the recommended land pattern dimensions.

Table 2-2. Recommended Land Pattern Dimensions

	Table 2 21 Recommended Land 1 determ 5 mensions				
Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)	
Е	Contact pitch	5.46 BSC	•	-	
X2	Center pad width	_	-	16.28	
Y2	Center pad length	_	_	13.18	
C1	Contact pad spacing	_	8.13	_	
C2	Contact pad spacing	_	3.28	_	
X1	Contact pad width (X2)	_	-	1.55	

continued				
Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
Y1	Contact pad length (X2)	_	_	3.48
G1	Contact pad to center pad (X2)	7.87	_	_

Notes:

- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process.

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
С	09/2024	The following changes are made in this revision of the document:
		• Updated value for I _{DM} in Table 1-1.
		• Updated Table 1-2.
		• Added V _{GS(th)} (Max.) value in Table 1-3.
		• Updated I _D value (Test Conditions) in Table 1-4.
		• Added V _{SD} (Max.) value in Table 1-5.
		• Updated I _{SD} value (Test Conditions) in Table 1-5.
		Updated Typical Performance Curves and Package Outline Drawing.
		Added Recommended Land Pattern.
В	09/2023	The following changes are made in this revision of the document:
		• Replaced the lead temperature with reflow temperature in the Table 1-2.
		Added Figure 1-8, Figure 1-9, Figure 1-10, and Figure 1-18.
		Updated Figure 1-5 and Figure 1-16.
A	05/2023	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00004987A, which replaces the previous Microsemi literature number 050-7750.
Initial releases (Microsemi Revisions A and B)	08/2019 – 10/2019	Initial releases.

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