Dual, 35 dB Range, 1 dB Step Size DGA

Data Sheet **ADL5205**

FEATURES

- Dual, independent, digitally controlled gain amplifier (DGA)
- −9 dB to +26 dB gain range
- 1 dB step size, ±0.2 dB accuracy at 200 MHz
- 100 Ω differential input resistance
- 10 Ω differential output resistance
- 1.2 dB change in noise figure for first 12 dB of gain reduction
- Output third-order intercept (OIP3): 48.5 dBm at 200 MHz, 5 V, high performance mode
- −3 dB bandwidth: 1700 MHz typical in high performance mode
- Multiple control interface options
  - Parallel 6-bit control interface with latch
  - Serial peripheral interface (SPI) with fast attack
  - Gain step up/down interface
- Wide input dynamic range
- Low power mode
- Power-down control
- Single 3.3 V or 5 V supply operation
- 40-lead, 6 mm × 6 mm LFCSP package

APPLICATIONS

- Differential analog-to-digital converter (ADC) drivers
- High intermediate frequency (IF) sampling receivers
- High output power IF amplification
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

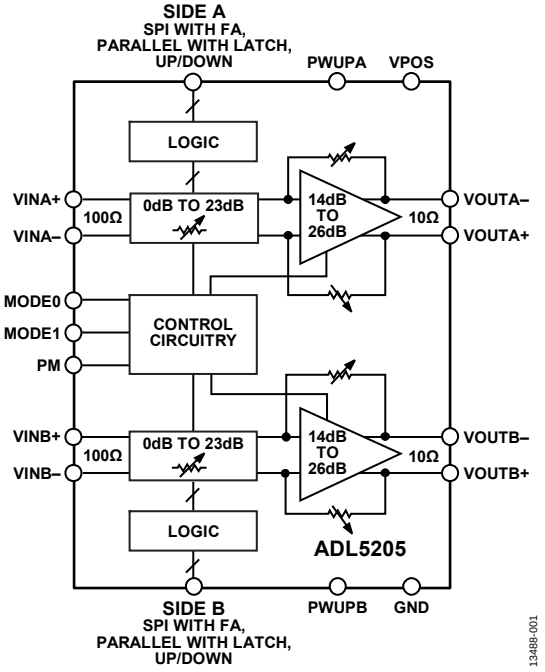


Figure 1.

GENERAL DESCRIPTION

The ADL5205 is a digitally controlled, wide bandwidth, variable gain dual amplifier (DGA) that provides precise gain control, high output third-order intercept (OIP3) and a near constant noise figure for the first 12 dB of attenuation. The excellent OIP3 performance of 48.5 dBm (at 200 MHz, 5 V, high performance mode, and maximum gain) makes the ADL5205 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the ADL5205 provides a broad 35 dB gain range with a 1 dB step size. The gain is adjustable through multiple gain control and interface options: parallel, SPI, or gain step up/down control.

The two channels of the ADL5205 can be powered up independently by applying the appropriate logic level to the PWUPA and PWUPB pins. The quiescent current of the ADL5205 is typically 175 mA for high performance mode and 135 mA for low power mode. When disabled, the ADL5205 consumes only 14 mA and offers excellent input to output isolation. The gain setting is preserved when the device is disabled.

Fabricated on the Analog Devices, Inc., high speed, silicon germanium (SiGe) complementary BiCMOS process, the ADL5205 provides precise gain adjustment capabilities with good distortion performance. The ADL5205 amplifier comes in a compact, thermally enhanced, 6 mm × 6 mm, 40-lead LFCSP package and operates over the temperature range of −40°C to +85°C.

Note that throughout this data sheet, multifunction pins, such as $\overline{\text{CSA}}$/A3, are referred to by the entire pin name or by a single function of the pin, for example, $\overline{\text{CSA}}$, when only that function is relevant.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/2019—Rev. 0 to Rev. A

Changes to Table 1 ... 4
Changes to Table 3 ... 6

4/2016—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_{POS}) = 3.3 V or 5 V, T_A = 25°C, Z_{LOAD} = 200 Ω, maximum gain (Gain code = 000000), frequency = 200 MHz, PM = 0 V, 2 V p-p differential output, unless otherwise noted.

Table 1.

		3.3 V Supply			5 V Supply			
Parameter[1]	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	High performance mode		1700			1700		MHz
	Low power mode		1500			1500		MHz
Slew Rate			5			5		V/ns
INPUT STAGE	VINx+ and VINx− pins							
Maximum Input Swing[2]	Gain code = 111111		8			8		V p-p
Differential Input Resistance	Differential		100			100		Ω
Input Common-Mode Voltage			1.65			2.5		V
Common-Mode Rejection Ratio (CMRR)	Gain code = 000000		48			48		dB
GAIN								
Voltage Gain Range			35			35		dB
Maximum Gain	Gain code = 000000		26			26		dB
Minimum Gain	Gain code = 100011 to 111111		−9			−9		dB
Gain Step Size			1			1		dB
Gain Step Accuracy			±0.2			±0.2		dB
Gain Flatness	From 30 MHz to 200 MHz		0.2			0.2		dB p-p
Gain Temperature Sensitivity	Gain code = 000000		2.4			4		mdB/°C
Fast Attack Step Response Delay	For V_{IN} = 0.1 V, FA_A or FA_B changing from 0 to 1 with 16 dB step		15			80		ns
COMMON-MODE INPUTS								
VCMA and VCMB Input Resistance			2.6			2.6		kΩ
OUTPUT STAGE	VOUTx+ and VOUTx− pins							
Output Voltage Swing	At P1dB, gain code = 000000		4.5			5.4		V p-p
Common-Mode Voltage Reference	VCMA, VCMB	1.2	1.65	1.8	1.4	2.5	2.7	V
Output Common-Mode Offset	((VOUTx+) + (VOUTx−))/2 − VCMx/2	−10		+10	−10		+10	mV
Differential Output Resistance	Differential		10			10		Ω
Short-Circuit Current	High performance mode		22			22		mA
	Low power mode		17			17		mA
NOISE/HARMONIC PERFORMANCE	Gain code = 000000, high performance mode							
10 MHz								
Noise Figure			6.3			6.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		−103			−103		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−101			−100		dBc
Output Third-Order Intercept (OIP3)	V_{OUT} = 2 V p-p composite		48.5			47		dBm
Output 1 dB Compression Point (P1dB)			13.7			17.5		dBm
100 MHz								
Noise Figure			6.3			6.6		dB
Second Harmonic	V_{OUT} = 2 V p-p		−86			−90		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−87			−94		dBc
OIP3	V_{OUT} = 2 V p-p composite		45			46		dBm
Output P1dB			13.2			17.4		dBm

Parameter[1]	Test Conditions/Comments	3.3 V Supply Min	3.3 V Supply Typ	3.3 V Supply Max	5 V Supply Min	5 V Supply Typ	5 V Supply Max	Unit
200 MHz								
Noise Figure Increase for First 12 dB of Gain Reduction	Gain code = 000000 to 001100		1.2			1.2		dB
Noise Figure			6.6			6.6		dB
Second Harmonic	V_{OUT} = 2 V p-p		−75.5			−75		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−77			−87.5		dBc
OIP3	V_{OUT} = 2 V p-p composite		44			48.5		dBm
Output P1dB			13			17		dBm
300 MHz								
Noise Figure			6.6			6.9		dB
Second Harmonic	V_{OUT} = 2 V p-p		−63			−64		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−68			−78		dBc
OIP3	V_{OUT} = 2 V p-p composite		43			43.5		dBm
Output P1dB			12.8			17.3		dBm
500 MHz								
Noise Figure			7.8			8.2		dB
Second Harmonic	V_{OUT} = 2 V p-p		−58			−61.5		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−57.5			−67.5		dBc
OIP3	V_{OUT} = 2 V p-p composite		37			36		dBm
Output P1dB			13.1			17.7		dBm
DIGITAL INTERFACE								
Input Pins	A0 to A5, B0 to B5, MODE1, MODE0, PWUPA, PWUPB, PM, LATCHA, LATCHB, SDIO							
V_{IH}	Logic high	2		VPOS	2		3.3	V
V_{IL}	Logic low	0		1.0	0		1.0	V
Input Leakage Current	Digital input voltage = 0 V to 3.3 V		±3			±3		µA
Output Pins	SDIO							
Logic High (V_{OH})	I_{OH} = −2 mA	2.4			2.4			V
Logic Low (V_{OL})	I_{OL} =2 mA			0.5			0.5	V
POWER-INTERFACE								
Supply Voltage (V_{POS})	VPOS	3.15	3.3	3.45	4.75	5	5.25	V
Quiescent Current								
High Performance Mode	PM = low		175			175		mA
Low Power Mode	PM = high		135			135		mA
Power-Down Current	PWUPA and PWUPB = low		14			14		mA

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] The maximum input swing of 8 V p-p is for the lowest gain setting of −9 dB. As the gain setting increases, the maximum input swing must be reduced correspondingly to maintain the same maximum output swing.

TIMING SPECIFICATIONS

Table 2. SPI Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CSA}$ or $\overline{CSB}$ to SCLK Setup Time	$t_{\overline{CS}}$	20			ns	
SDIO to SCLK Setup Time	t_{DS}	10			ns	
SCLK to SDIO Hold Time	t_{DH}	10			ns	
SCLK Pulse Width	t_{PW}	25			ns	
SCLK Cycle Time	t_{SCLK}	50			ns	
SCLK to $\overline{CSA}$ or $\overline{CSB}$ Setup Time	t_{CH}	10			ns	
SCLK to SDIO Output Valid Delay	t_{DV}			20	ns	During readback

Timing Diagrams

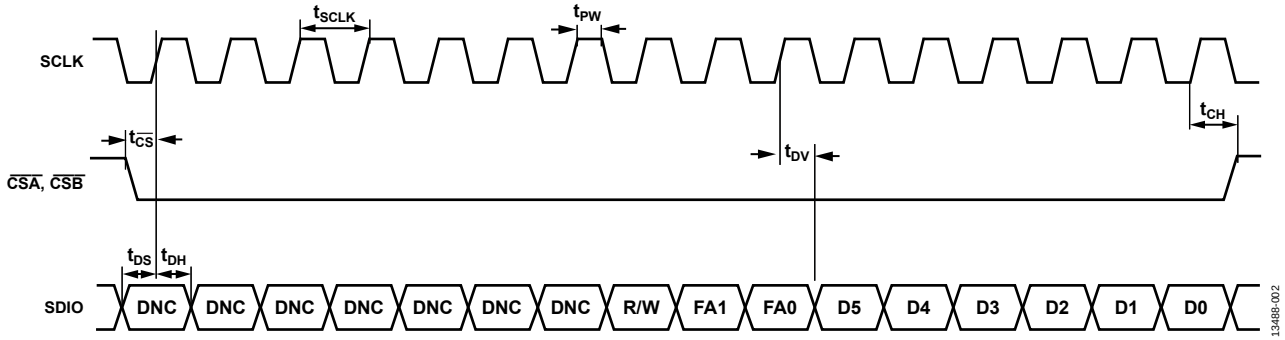


Figure 2. SPI Interface Read/Write Mode Timing Diagram

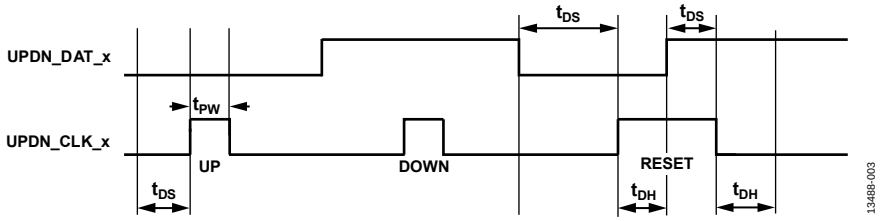


Figure 3. Up/Down Gain Control Timing Diagram

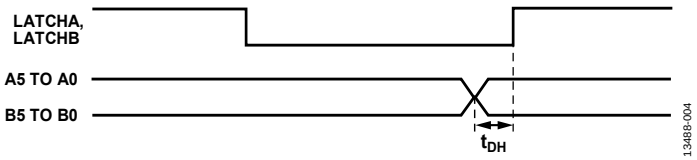


Figure 4. Parallel Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Differential Output Voltage Swing × Bandwidth Product	3 V-GHz
Supply Voltage, V_{POS}	5.4 V
PWUPA, PWUPB, A0 to A5, B0 to B5, MODE0, MODE1, PM, LATCH A, LATCH B	−0.5 V to +3.6 V
Input Voltage (VINx+ ,VINx−)	−0.5 V to +3.1 V
Differential Input Voltage ((VINx+) − (VINx−))[1]	±1 V
Internal Power Dissipation	1000 mW
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] The differential input voltage limit is significantly lower than the maximum input swing of 8 V p-p. The maximum input swing is for the lowest gain setting of −9 dB. As the gain setting is increased, the maximum input swing must be reduced correspondingly to maintain the same maximum output swing. The differential input voltage limit takes effect at greater than ~14 dB, at which point there is no more resistive attenuation on the input and the signal presented on the pins goes directly on an input ESD protection circuit. Therefore, the input signal swing must be limited to a low value.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 4 shows the thermal resistance from the die to ambient (θ_{JA}), die to board (θ_{JB}), and die to lead (θ_{JC}), respectively.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
40-Lead LFCSP	47.7	24.4	15.4	°C/W

JUNCTION TO BOARD THERMAL IMPEDANCE

The junction to board thermal impedance (θ_{JB}) is the thermal impedance from the die to the leads of the ADL5205. The value given in Table 4 is based on the standard printed circuit board (PCB) described in the JESD51-7 standard for thermal testing of surface-mount components. PCB size and complexity (number of layers) affect θ_{JB}; more layers tend to reduce thermal impedance slightly.

If the PCB temperature is known, use the junction to board thermal impedance to calculate the die temperature (also known as the junction temperature) to ensure that the die temperature does not exceed the specified limit of 135°C. For example, if the PCB temperature is 85°C, the die temperature is given by

$$T_J = T_B + (P_{DISS} \times \theta_{JB})$$

The worst case power dissipation for the ADL5205 is 919 mW (5.25 V × 175 mA, see Table 1). Therefore, T_J is

$$T_J = 85°C + (0.919\ W \times 24.4°C/W) = 107.4°C$$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

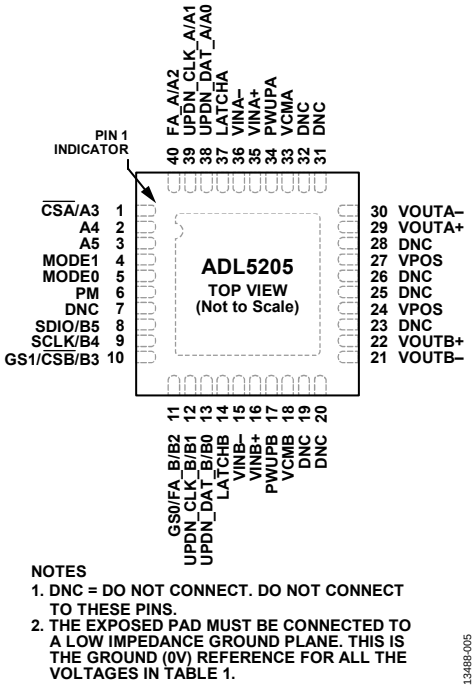


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CSA}}$/A3	Channel A Select in Serial Mode ($\overline{\text{CSA}}$). When serial mode is enabled, a logic low selects Channel A.
		Bit 3 for Channel A in Parallel Gain Control Interface Mode (A3).
2	A4	Bit 4 for Channel A in Parallel Gain Control Interface Mode (A4).
3	A5	Bit 5 for Channel A in Parallel Gain Control Interface Mode (A5).
4	MODE1	MSB for Mode Control. Use both the MODE0 and MODE1 pins to select parallel, SPI, or up/down interface mode.
5	MODE0	LSB for Mode Control. Use both the MODE1 and MODE0 pins to select parallel, SPI, or up/down interface mode.
6	PM	Power Mode. Set this pin to logic low to enable high performance mode, or logic high to enable low power mode.
7, 19, 20, 23, 25, 26, 28, 31, 32	DNC	Do Not Connect. Do not connect to these pins.
8	SDIO/B5	Serial Data Input and Output in SPI Mode (SDIO).
		Bit 5 for Channel B in Parallel Gain Control Interface Mode (B5).
9	SCLK/B4	Serial Clock Input in SPI Mode (SCLK).
		Bit 4 for Channel B in Parallel Gain Control Interface (B4).
10	GS1/$\overline{\text{CSB}}$/B3	MSB for the Gain Step Size Control in Up/Down Mode (GS1).
		Channel B Select in Serial Mode ($\overline{\text{CSB}}$). When serial mode is enabled, a logic low selects Channel B.
		Bit 3 for Channel B in Parallel Gain Control Mode (B3).
11	GS0/FA_B/B2	LSB for the Gain Step Size Control in Up/Down Mode (GS0).
		Fast Attack for Channel B (FA_B). In serial mode, a logic high on this pin attenuates Channel B according to the FA bit values in the control register.
		Bit 2 for Channel B in Parallel Gain Control Interface (B2).
12	UPDN_CLK_B/B1	Clock Interface for the Channel B Up/Down Function (UPDN_CLK_B).
		Bit 1 for Channel B in Parallel Gain Control Interface Mode (B1).
13	UPDN_DAT_B/B0	Data Pin for the Channel B Up/Down Function (UPDN_DAT_B).
		Bit 0 for Channel B in Parallel Gain Control Interface Mode (B0).

Pin No.	Mnemonic	Description
14	LATCHB	Latch B. A logic low on this pin allows the gain to change on Channel B in parallel gain control interface mode. A logic high on this pin prevents gain changes.
15	VINB−	Channel B Negative Analog Input.
16	VINB+	Channel B Positive Analog Input.
17	PWUPB	Channel B Power-Up. A logic high on this pin powers up Channel B, and a logic low on this pin disables it.
18	VCMB	Channel B Common-Mode Output.
21	VOUTB−	Channel B Negative Analog Output.
22	VOUTB+	Channel B Positive Analog Output.
24, 27	VPOS	Positive Power Supply.
29	VOUTA+	Channel A Negative Analog Output.
30	VOUTA−	Channel A Positive Output.
33	VCMA	Channel A Common-Mode Output.
34	PWUPA	Channel A Power-Up. A logic high on this pin powers up Channel A, and a logic low on this pin disables it.
35	VINA+	Channel A Positive Analog Input.
36	VINA−	Channel A Negative Analog Input.
37	LATCHA	Latch A. A logic low on this pin allows the gain to change on Channel A in the parallel gain control interface mode. A logic high on this pin prevents gain changes.
38	UPDN_DAT_A/A0	Data Pin for the Channel A Up/Down Function (UPDN_DAT_A). Bit 0 for Channel A in Parallel Gain Control Interface Mode (A0).
39	UPDN_CLK_A/A1	Clock Interface for the Channel A Up/Down Function (UPD_CLK_A). Bit 1 for Channel A in Parallel Gain Control Interface Mode (A1).
40	FA_A/A2	Fast Attack for Channel A (FA_A). In serial mode, a logic high on this pin attenuates Channel A according to an FA SPI word. Bit 2 for Channel A in Parallel Gain Control Interface (A2).
EP	GND	Exposed Pad Ground. The exposed pad must be connected to a low impedance ground plane. This is the ground (0 V) reference for all the voltages in Table 1.

TYPICAL PERFORMANCE CHARACTERISTICS

Supply voltage (V_{POS}) = 3.3 V or 5 V, T_A = 25°C, Z_{LOAD} = 200 Ω, maximum gain (gain code = 000000), 2 V p-p composite differential output for intermodulation distortion (IMD) and OIP3, 2 V p-p differential output for second harmonic distortion (HD2) and third harmonic distortion (HD3), VCMA = VCMB = V_{POS}/2, unless otherwise noted.

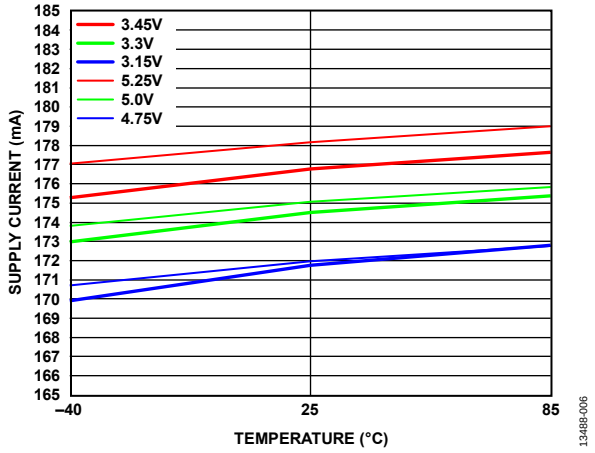


Figure 6. Supply Current vs. Temperature, PM = 0

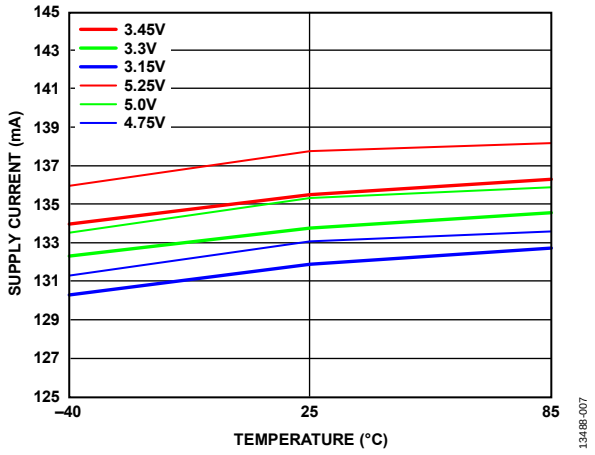


Figure 7. Supply Current vs. Temperature, PM = 1

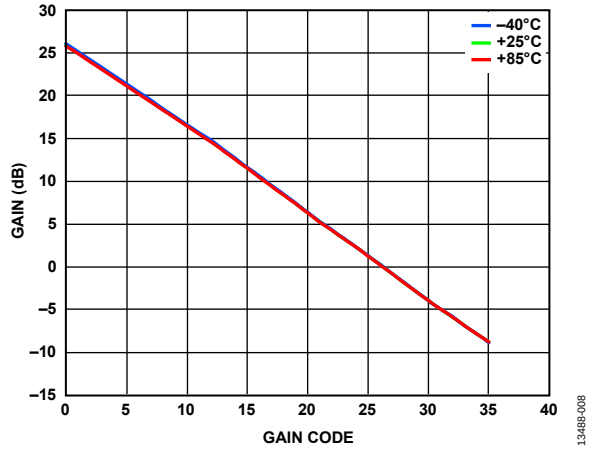


Figure 8. Gain vs. Gain Code over Temperature at 200 MHz

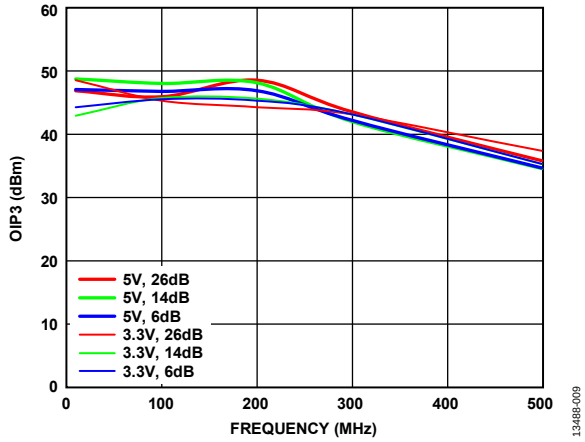


Figure 9. Output Third-Order Intercept (OIP3) vs. Frequency over V_{POS} at Three Gain Codes, High Performance Mode

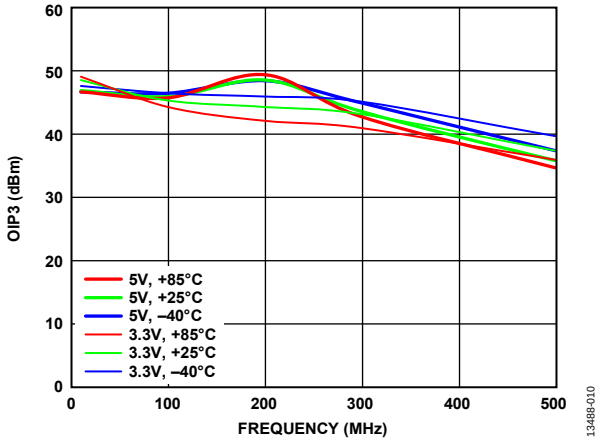


Figure 10. Output Third-Order Intercept (OIP3) vs. Frequency over V_{POS} for Three Temperatures at Maximum Gain, High Performance Mode

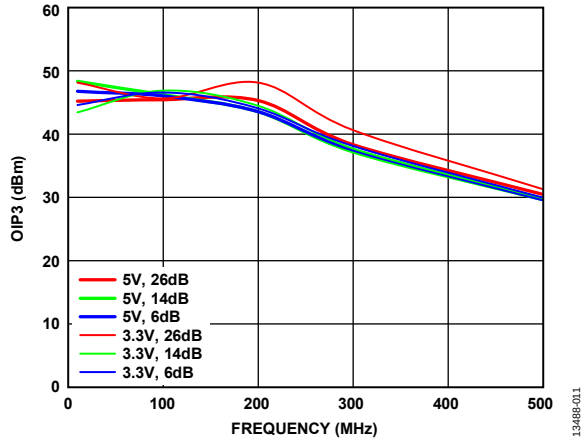


Figure 11. Output Third-Order Intercept (OIP3) vs. Frequency over V_{POS} at Three Gain Codes, Low Power Mode

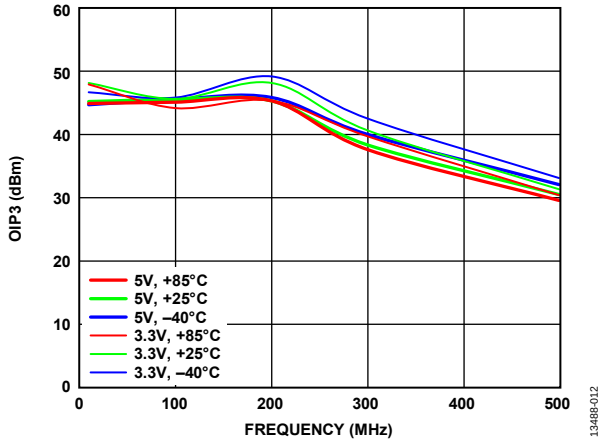


Figure 12. Output Third-Order Intercept (OIP3) vs. Frequency over V_{POS} for Three Temperatures at Maximum Gain, 2 V p-p Composite, Low Power Mode

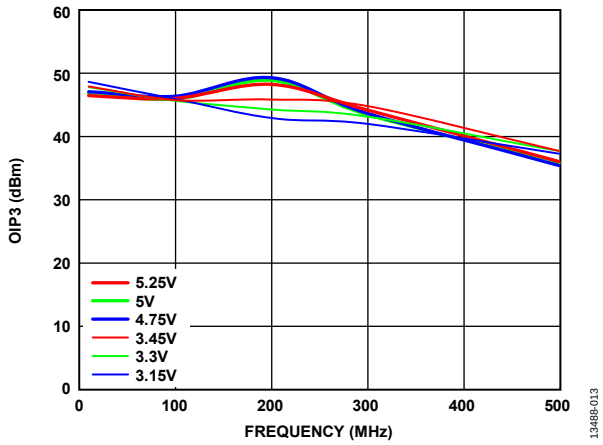


Figure 13. Output Third-Order Intercept (OIP3) vs. Frequency and V_{POS} Variance (±5%), Maximum Gain, High Performance Mode

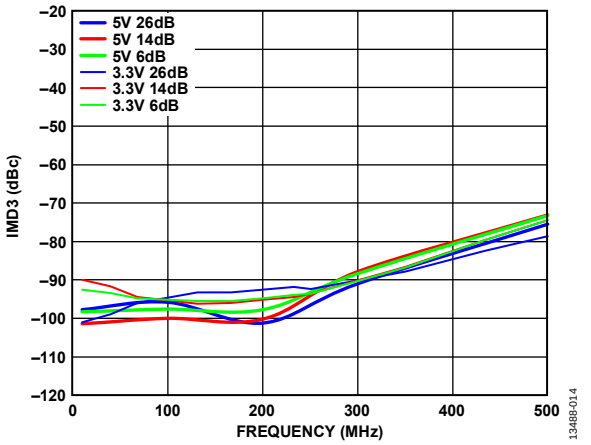


Figure 14. Two-Tone Output IMD3 vs. Frequency over V_{POS} for Three Gain Codes at 2 V p-p Composite, Low Power Mode

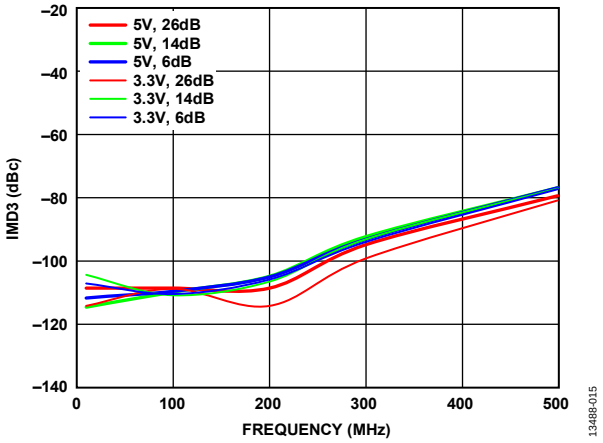


Figure 15. Two-Tone Output IMD3 vs. Frequency over V_{POS} for Three Gain Codes at 2 V p-p, High Performance Mode

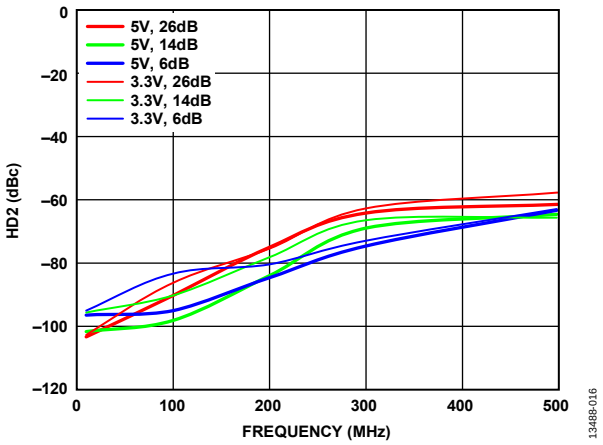


Figure 16. Second Harmonic Distortion (HD2) vs. Frequency over V_{POS} for Three Gain Codes, High Performance Mode

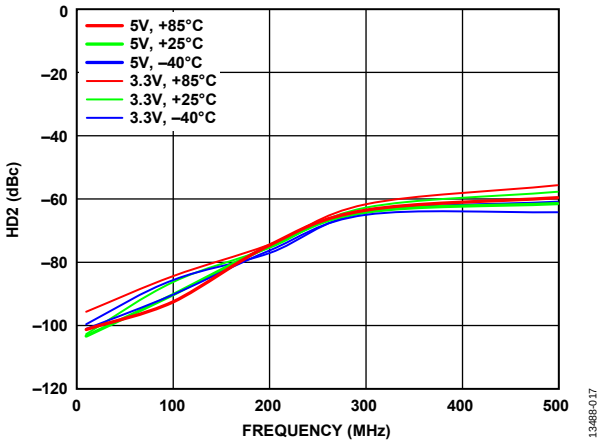


Figure 17. Second Harmonic Distortion (HD2) vs. Frequency over V_{POS} for Three Temperatures at Maximum Gain, 2 V p-p, High Performance Mode

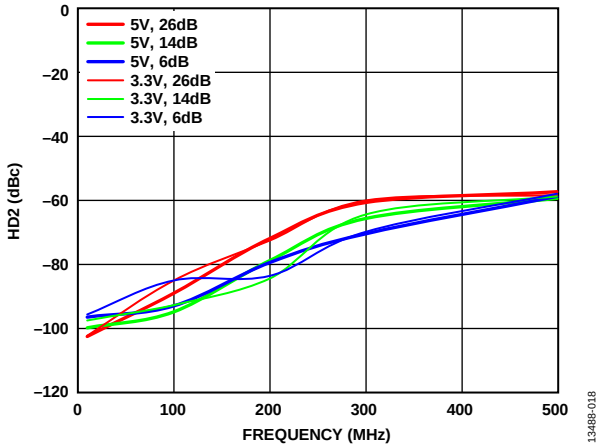


Figure 18. Second Harmonic Distortion (HD2) vs. Frequency over V_{POS} for Three Gain Codes at 2 V p-p Composite, Low Power Mode

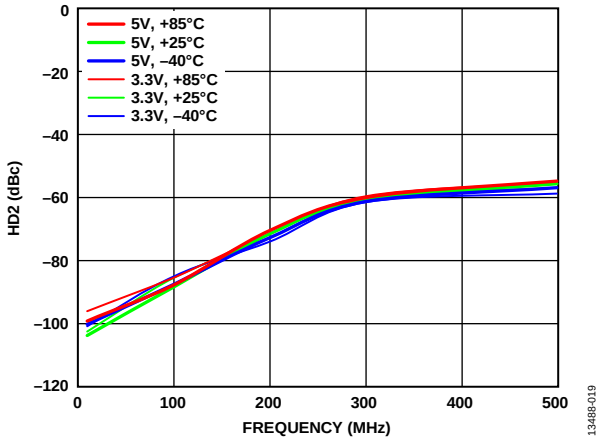


Figure 19. Second Harmonic Distortion (HD2) vs. Frequency over V_{POS} for Three Temperatures at Maximum Gain, 2 V p-p Composite, Low Power Mode

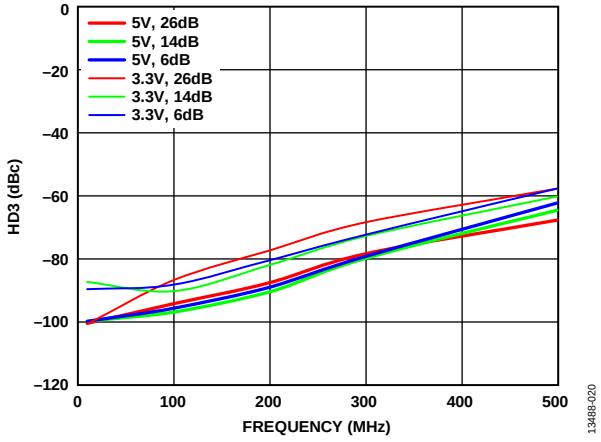


Figure 20. Third Harmonic Distortion (HD3) vs. Frequency over V_{POS} for Three Gain Codes at 2 V p-p Composite, High Performance Mode

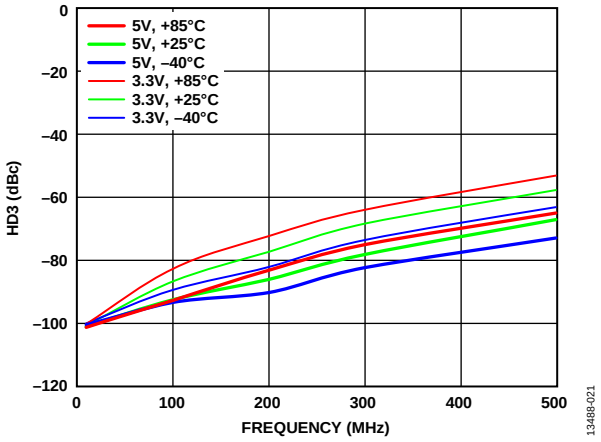


Figure 21. Third Harmonic Distortion (HD3) vs. Frequency vs. V_{POS} for Three Temperatures at Maximum Gain, 2 V p-p Composite, High Performance Mode

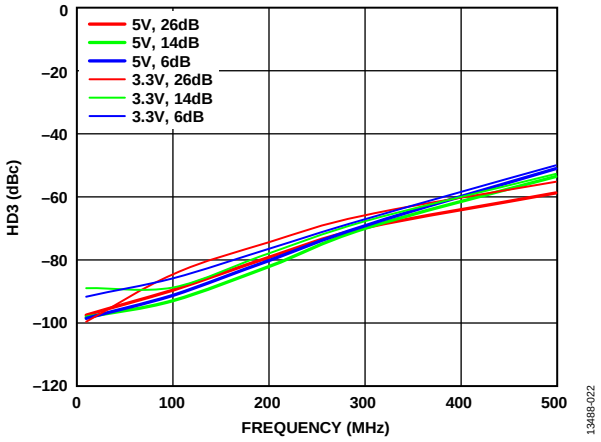


Figure 22. Third Harmonic Distortion (HD3) vs. Frequency over V_{POS} for Three Gain Codes at 2 V p-p Composite, Low Power Mode

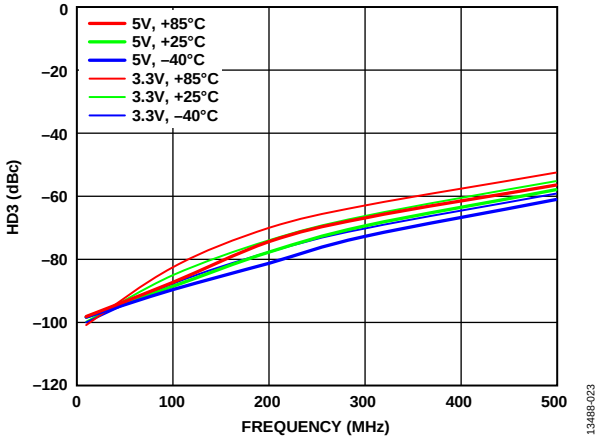


Figure 23. Third Harmonic Distortion (HD3) vs. Frequency over V_{POS} for Three Temperatures at Maximum Gain, 2 V p-p Composite, Low Power Mode

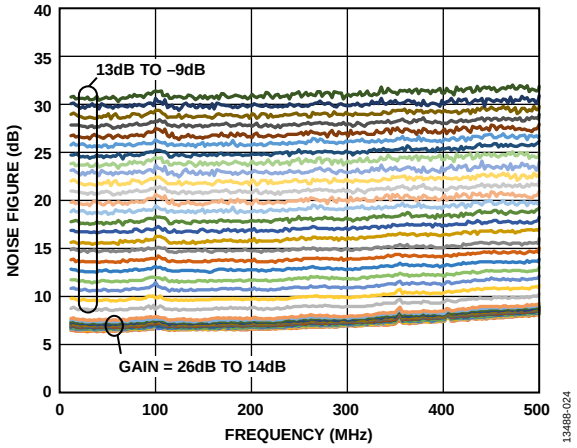


Figure 24. Noise Figure vs. Frequency for 35 dB Gain Range at V_{POS} = 5 V, High Performance Mode

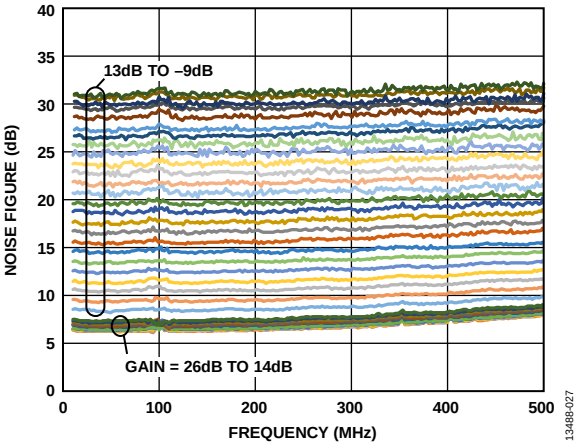


Figure 27. Noise Figure vs. Frequency for 35 dB Gain Range at V_{POS} = 3.3 V, Low Power Mode

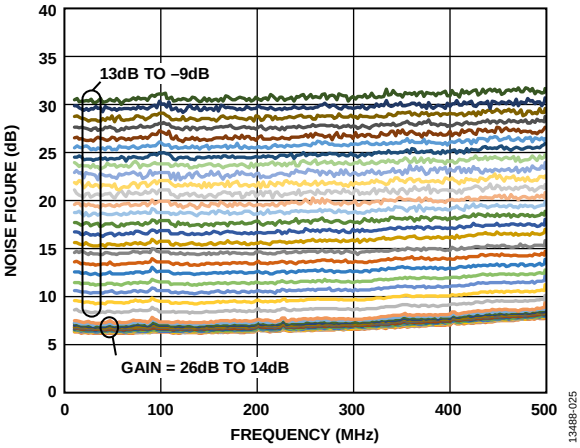


Figure 25. Noise Figure vs. Frequency for 35 dB Gain Range at V_{POS} = 3.3 V, High Performance Mode

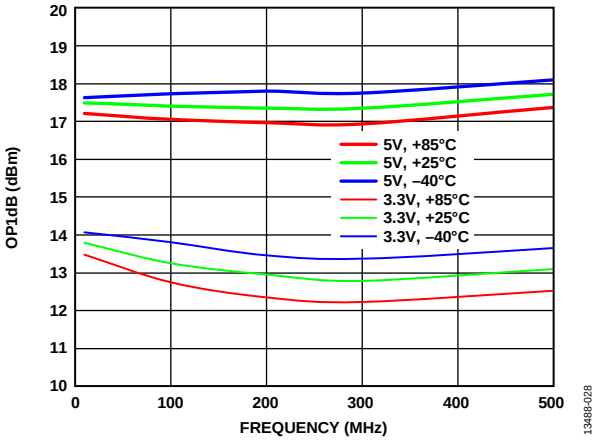


Figure 28. Output 1 dB Compression Point (OP1dB) vs. Frequency at Maximum Gain, High Performance Mode

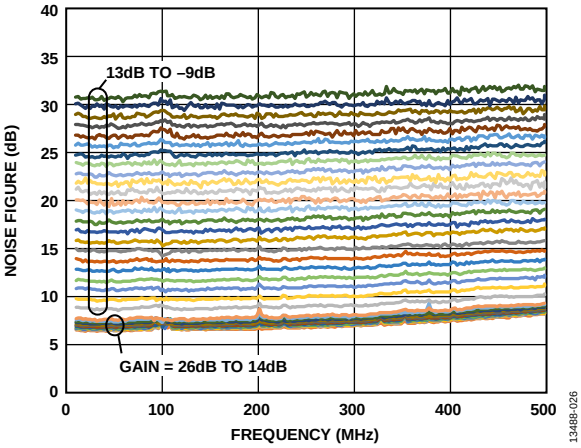


Figure 26. Noise Figure vs. Frequency for 35 dB Gain Range at V_{POS} = 5 V, Low Power Mode

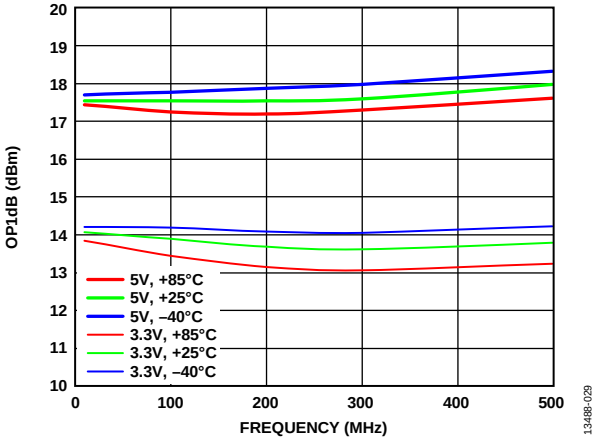


Figure 29. Output 1 dB Compression Point (OP1dB) vs. Frequency at Maximum Gain, Low Power Mode

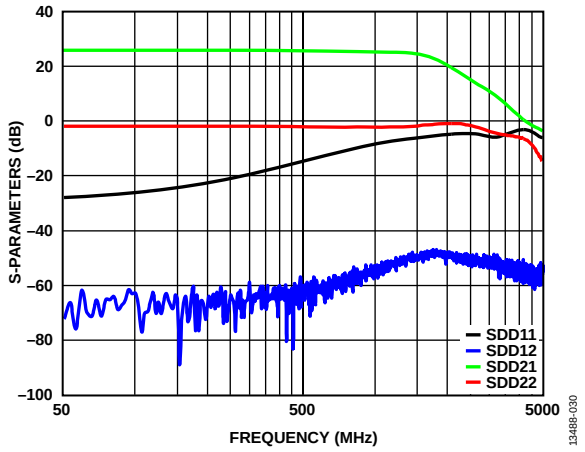


Figure 30. Differential S-Parameters (SDD21, SDD12, SDD11, SDD22) vs. Frequency

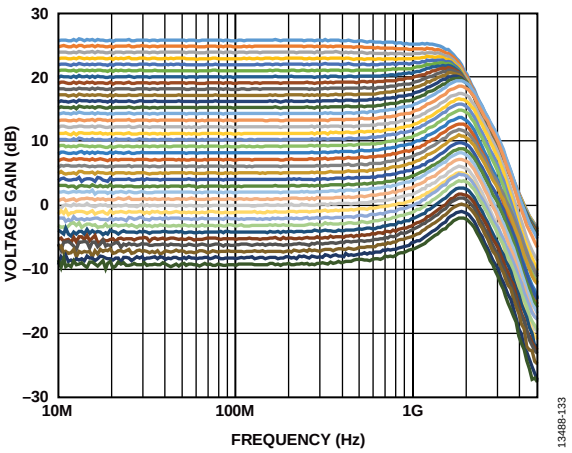


Figure 33. Voltage Gain vs. Frequency for Various Gain Steps at V_{POS} = 5 V, High Performance Mode

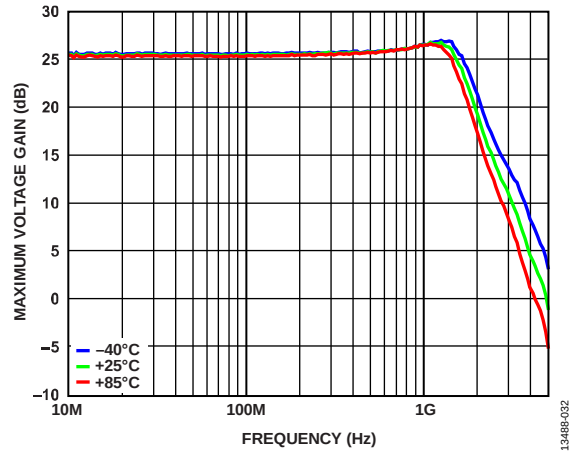


Figure 31. Maximum Voltage Gain vs. Frequency over Temperature at V_{POS} = 3.3 V

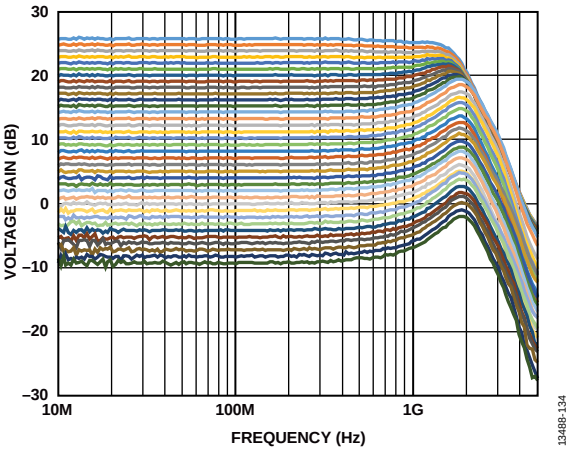


Figure 34. Voltage Gain vs. Frequency for Various Gain Steps at V_{POS} = 3.3 V, High Performance Mode

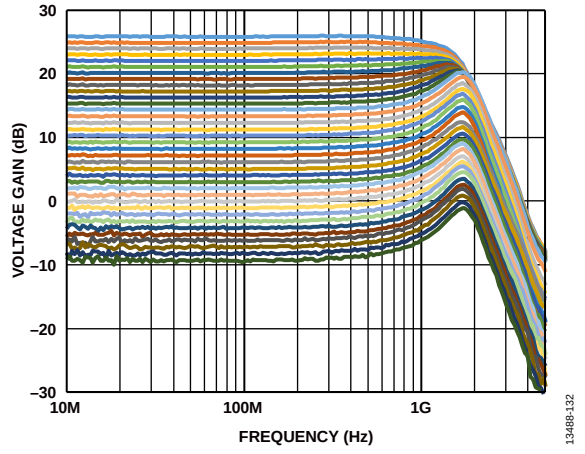


Figure 32. Voltage Gain vs. Frequency for Various Gain Steps at V_{POS} = 3.3 V, Low Power Mode

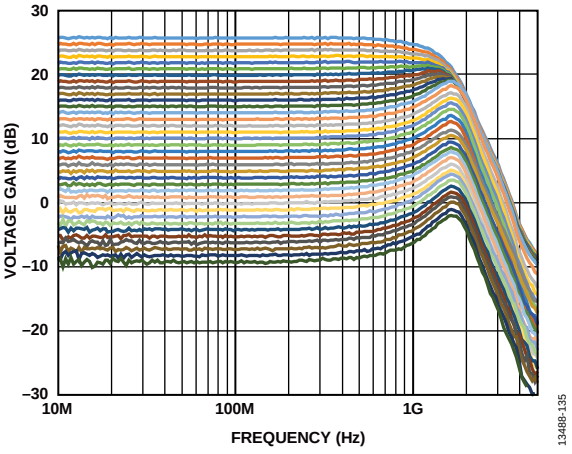


Figure 35. Voltage Gain vs. Frequency for Various Gain Steps at V_{POS} = 5 V, Low Power Mode

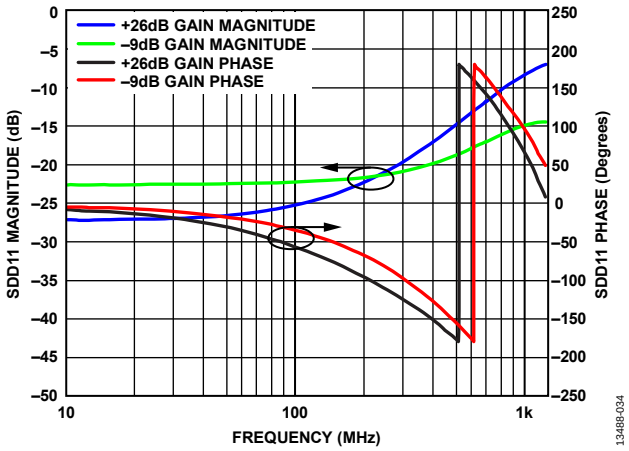


Figure 36. Differential Input Reflection (SDD11) Magnitude and Phase vs. Frequency

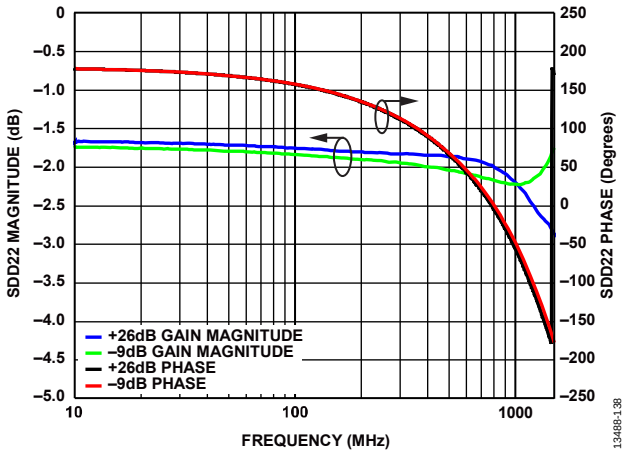


Figure 37. Differential Output Reflection (SDD22) Magnitude and Phase vs. Frequency

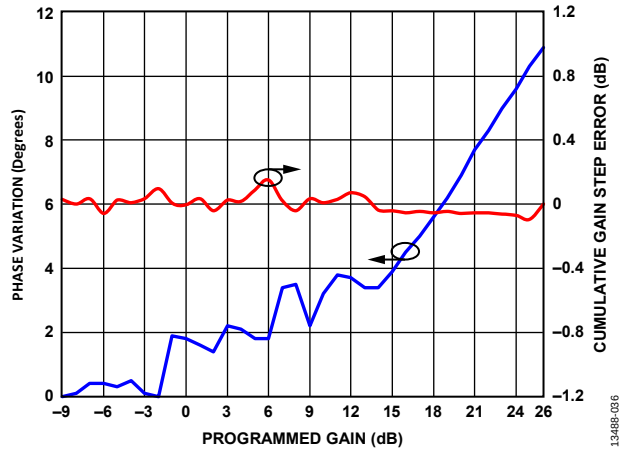


Figure 38. Phase Variation and Cumulative Gain Step Error vs. Programmed Gain, Frequency = 200 MHz, V_{POS} = 3.3 V, 2 V p-p Composite

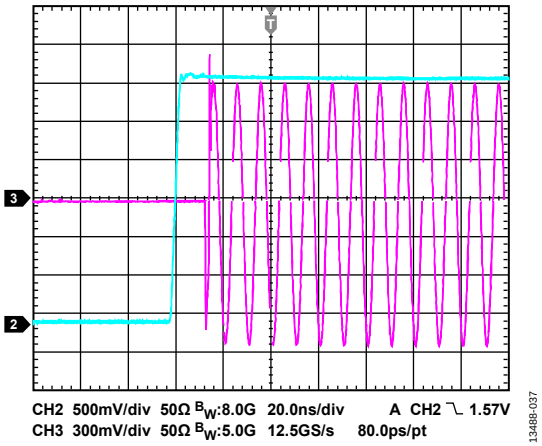


Figure 39. Enable Time Domain Response at V_{POS} = 5 V

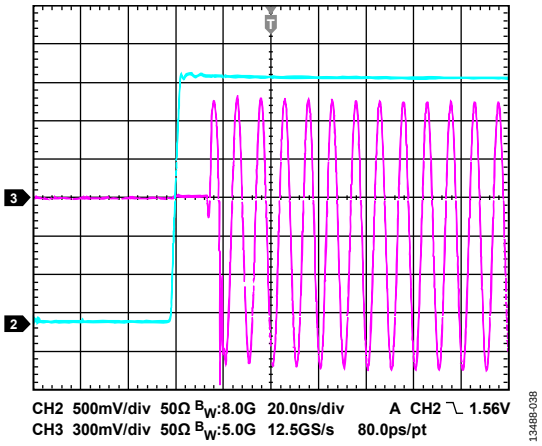


Figure 40. Enable Time Domain Response at V_{POS} = 3.3 V

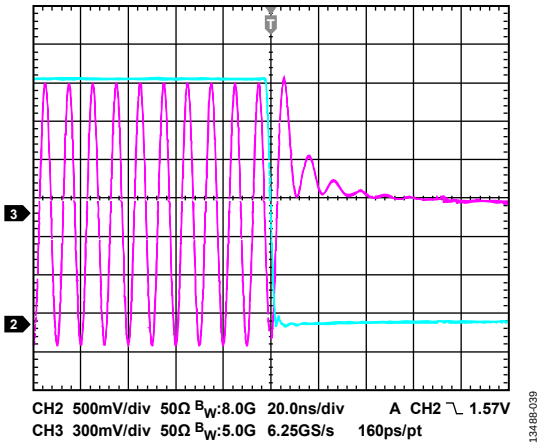


Figure 41. Disable Time Domain Response at V_{POS} = 5 V

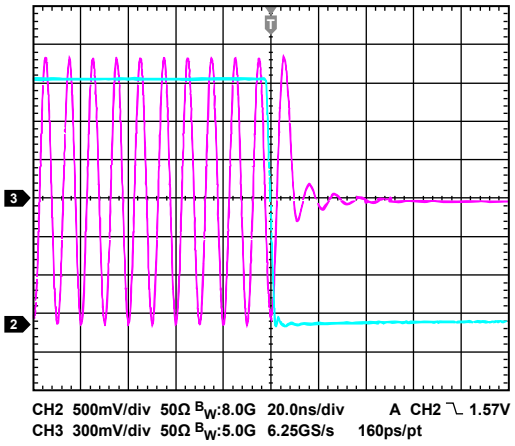


Figure 42. Enable Time Domain Response at V_{POS} = 3.3 V

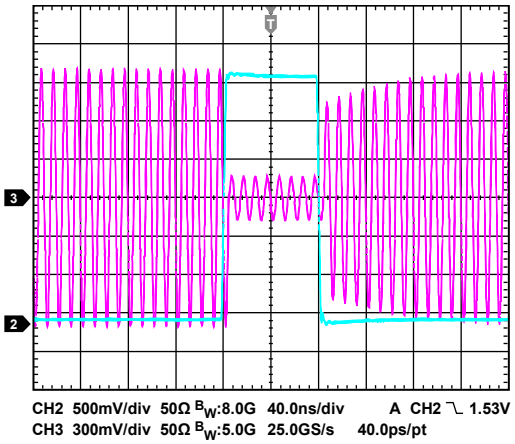


Figure 43. Fast Attack Step Time Domain Response at V_{POS} = 5 V

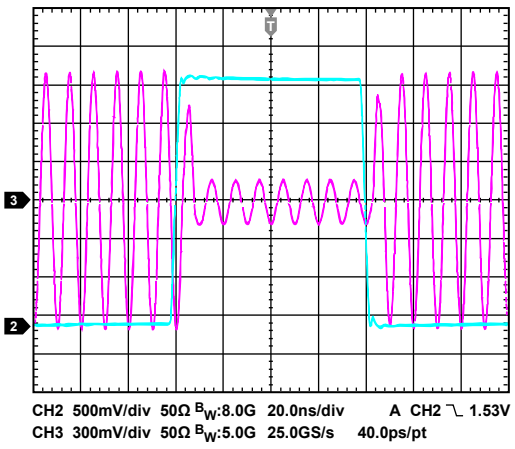


Figure 44. Fast Attack Step Time Domain Response at V_{POS} = 3.3 V

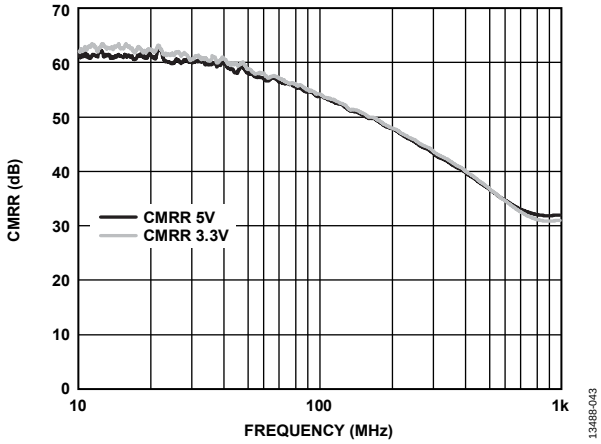


Figure 45. CMRR vs. Frequency at Maximum Gain

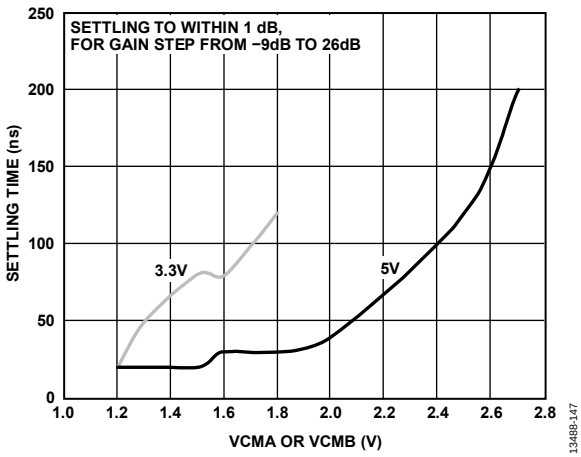


Figure 46. Maximum Gain Transition Settling Time vs. Output Common-Mode Voltage (VCMA or VCMB)

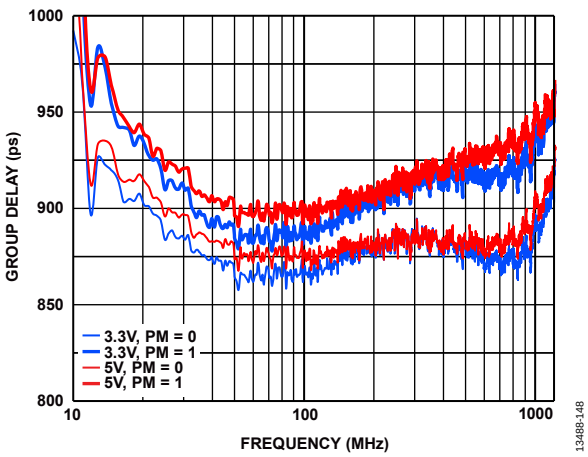


Figure 47. Group Delay at Maximum Gain vs. Frequency over V_{POS} and Power Modes

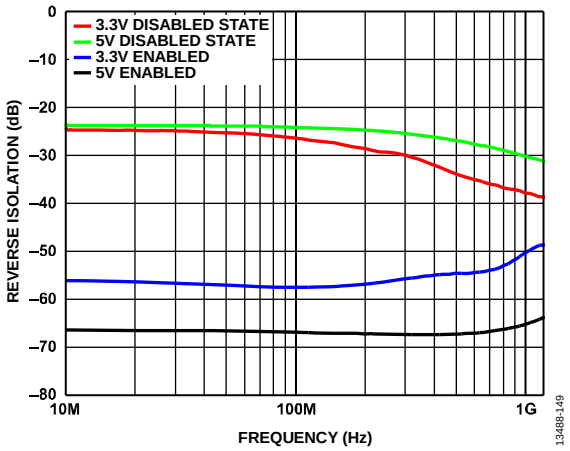


Figure 48. Reverse Isolation vs. Frequency

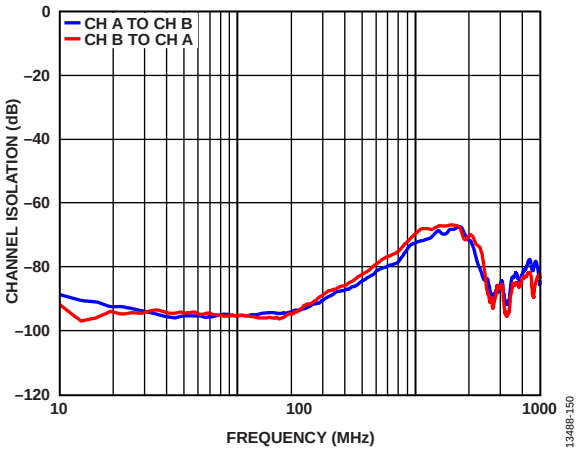


Figure 49. Channel Isolation vs. Frequency for Channel A and Channel B

THEORY OF OPERATION

BASIC STRUCTURE

The ADL5205 is a dual differential, digitally controlled variable gain amplifier (DGA). Each DGA consists of a 100 Ω differential input, digitally controlled passive attenuator followed by a digitally controlled gain amplifier. The input, digitally controlled, binary weighted attenuator has a range of 0 dB to 23 dB with 1 dB steps, and the amplifier has a range of 14 dB to 26 dB, also with 1 dB steps. On-chip logic circuitry maps the gain codes such that the first 12 dB of gain reduction from the maximum gain are accomplished using the digitally controlled gain amplifier, only. This topology allows the first 12 dB of gain reduction to be accompanied by typically 1.2 dB of total noise figure degradation (at 200 MHz). The OIP3 also remains nearly constant over the first 12 dB of gain range. The noise figure for the DGA increases by 1 dB for each decibel of attenuation within the remaining 23 dB attenuation range. The differential output impedance of the amplifier is 10 Ω.

CONTROL/LOGIC CIRCUITRY

The ADL5205 features three different gain control interfaces: serial, parallel, or up/down control, determined by the combination of the MODE1 and MODE0 pins. For details on controlling the gain in each of these modes, see the Digital Interface Overview section. In general, the gain step size is 1 dB; however, larger step sizes can be programmed as described in the Digital Interface Overview section. Each amplifier has a maximum gain of +26 dB (Gain Code 000000) to −9 dB (Gain Code 100011 to Gain Code 111111). Using the performance mode (PM) pin, users can lower the power consumption of the device with a slight degradation in linearity performance.

COMMON-MODE VOLTAGE

The ADL5205 is flexible in terms of input/output coupling. It can be ac-coupled or dc-coupled at the inputs and/or outputs within the specified output common-mode levels of 1.2 V to 2.7 V, depending on the supply voltage. If no external output common-mode voltage is applied, the input and output common-mode voltages are set internally to half of the supply voltage.

The output common-mode voltages of the ADL5205 are controlled by the voltages on the VCMA and VCMB pins. Each of these pins is connected internally through 5 kΩ resistors to the VPOS pin as well as to the exposed pad (EP). As a result, the common-mode output voltage at each channel is preset internally to half of the supply voltage at VPOS. Alternatively, the VCMA and VCMB pins can be connected to the common-mode voltage reference output from an ADC, and thus the common-mode levels between the two devices can be matched without requiring any external components.

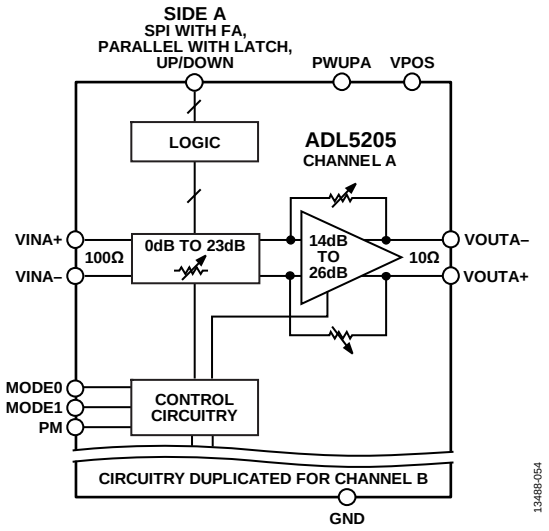


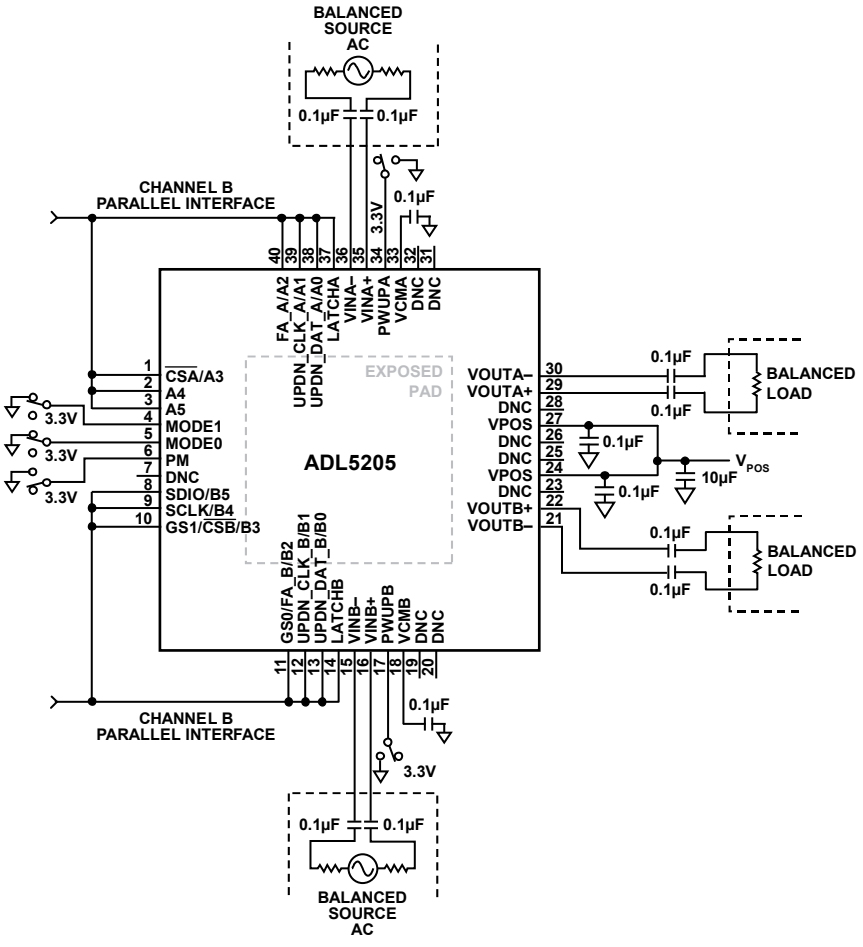
Figure 50. Basic Structure

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 51 shows the basic connections for operating the ADL5205. Apply a voltage of 3.3 V or 5 V to the VPOS pins. Decouple each supply pin with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close to the device as possible. The differential outputs have a dc common-mode voltage that is approximately half of the supply; therefore, decouple these outputs using 0.1 µF capacitors to the balanced load. The balanced differential inputs have the same dc common-mode voltage as the outputs; the inputs are decoupled using 0.1 µF capacitors as well. The digital pins, mode control pins, associated SPI pins, and parallel gain control pins, (PM, PWUPA, and PWUPB) operatefrom a 3.3 V voltage.

To enable each channel of the ADL5205, pull the PWUPA pin or the PWUPB pin high (2.0 V ≤ PWUPA/PWUPB ≤ 3.3 V). A logic low on the PWUPA pin or the PWUPB pin sets the channel to sleep mode, reducing the current consumption to approximately 7 mA per channel. The VCMA and the VCMB pins are the reference inputs for the output common-mode voltage of each channel, and they must be decoupled with 0.1 µF capacitors.



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. THE EXPOSED PAD MUST BE CONNECTED TO A LOW IMPEDANCE GROUND PLANE. THIS IS THE GROUND (0V) REFERENCE FOR ALL THE VOLTAGES IN TABLE 1.

13488-053

Figure 51. Basic Connections

DIGITAL INTERFACE OVERVIEW

The three digital control interface options of the ADL5205 DGA are, respectively,

- Parallel control interface
- Serial peripheral interface
- Gain step up/down interface

The digital control interface selection is made via two digital pins, MODE1 and MODE0, as shown in Table 6. Additionally, there are three power mode control pins, PM, PWUPA, and PWUPB. PM selects between the high performance and low power modes, whereas PWUPA and PWUPB enable (power-up) the corresponding channel. The gain in each channel is controlled by a 6-bit binary code (A5 to A0 and B5 to B0).

The same physical pins are shared between three interfaces, resulting in as many as three different functions per digital pin (see Table 5).

Table 6. Digital Control Interface Selection Truth Table

MODE1	MODE0	Interface
0	0	Parallel
0	1	Serial (SPI)
1	0	Up/down
1	1	Up/down

Parallel Digital Interface

The parallel digital interface uses six gain control bits and a latch pin per amplifier. The latch pin controls whether the input data latch is transparent (logic low) or latched (logic high). In transparent mode, the gain changes as the input gain control bits change. In latched mode, the gain is determined by the latched gain setting and is not changed by changing the input gain control bits.

Serial Peripheral Interface (SPI)

The SPI uses three pins (SDIO, SCLK, and $\overline{CSA}$ or $\overline{CSB}$). The SPI data register consists of two bytes: six gain control bits (D0 to D5), two attenuation step size address bits (FA0 and FA1), one read/write bit (R/$\overline{W}$), and seven don't care bits (X), as shown in Figure 53.

The SPI uses a bidirectional pin (SDIO) for writing to the SPI register and for reading from the SPI register. To write to the SPI register, pull the $\overline{CSA}$ or the $\overline{CSB}$ pin low and apply 16 clock pulses to shift the 16 bits into the corresponding SPI register, MSB first. Individual channel SPI registers can be selected by pulling $\overline{CSA}$ or $\overline{CSB}$ low. By simultaneously pulling the $\overline{CSA}$ and $\overline{CSB}$ pins low, the same data can be written to both SPI registers.

SPI register read back operation is described in the SPI Read section. Because there is only one SDIO line, the control register of each channel must be read back individually.

SPI fast attack mode is controlled by the FA_A or FA_B pins. A logic high on the FA_A pin or FA_B pin results in an attenuation selected by the FA1 and the FA0 bits in the SPI register.

Table 7. SPI 2-Bit Attenuation Step Size Truth Table

FA1	FA0	Step Size (dB)
0	0	2
0	1	4
1	0	8
1	1	16

Up/Down Interface

The up/down interface uses two digital pins to control the gain. When the UPDN_DAT_x pin is low, the gain for the corresponding channel is increased by a clock pulse on the UPDN_CLK_x pin (rising and falling edges). When the UPDN_DAT_x pin is high, the corresponding gain is decreased by a clock pulse on the UPDN_CLK_x pin. Reset is detected when the rising edge of UPDN_CLK_x latches one polarity on UPDN_DAT_x, and the falling edge latches the opposite polarity. Reset results in the minimum gain code of 111111.

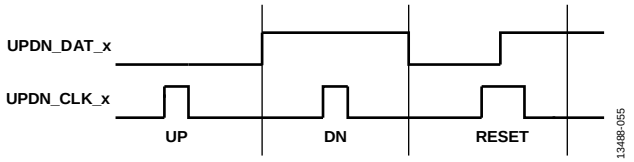


Figure 52. Up/Down Gain Control Timing

The step size is selectable by the GS1 and GS0 pins. The default step size is 1 dB. The gain code count rails at the top and bottom of the control range.

Table 8. Step Size Control Truth Table

GS1	GS0	Step Size (dB)
0	0	1
0	1	2
1	0	4
1	1	8

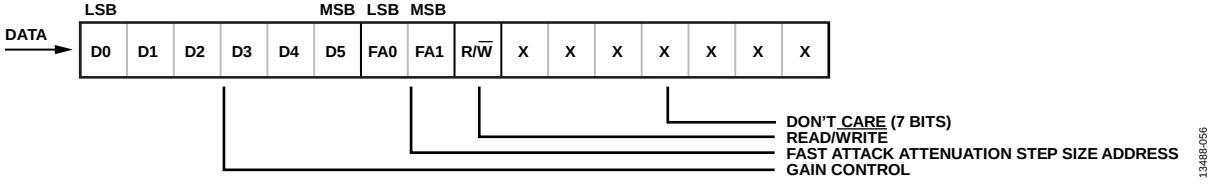


Figure 53. 16-Bit SPI Register

Table 9. Gain Code vs. Voltage Gain

6-Bit Binary Gain Code, D5 to D0	Voltage Gain (dB)
000000	+26
000001	+25
000010	+24
000011	+23
000100	+22
000101	+21
000110	+20
000111	+19
001000	+18
001001	+17
001010	+16
001011	+15
001100	+14
001101	+13
001110	+12
001111	+11
010000	+10
010001	+9
010010	+8
010011	+7
010100	+6
010101	+5
010110	+4
010111	+3
011000	+2
011001	+1
011010	0
011011	−1
011100	−2
011101	−3
011110	−4
011111	−5
100000	−6
100001	−7
100010	−8
100011 to 111111	−9

SPI READ

The ADL5205 can be read back only in the serial mode, during a read cycle (from $\overline{CSA}/\overline{CSB}$ low to $\overline{CSA}/\overline{CSB}$ high) after the R/$\overline{W}$ bit is set high in the previous cycle. During the read cycle, data changes at each rising edge of SCLK, and can be latched using the falling edge of SCLK. There is no continual read operation. A logic high (1) must be written into the R/$\overline{W}$ bit to enable the subsequent read cycle. The sequence for reading back is shown in Figure 54 to Figure 57, showing the operation of the input and output functions of the SDIO pin. The actual waveforms during the readback process are shown in Figure 57 to Figure 59. SDIO is enabled as an output only during the read cycle in Figure 57.

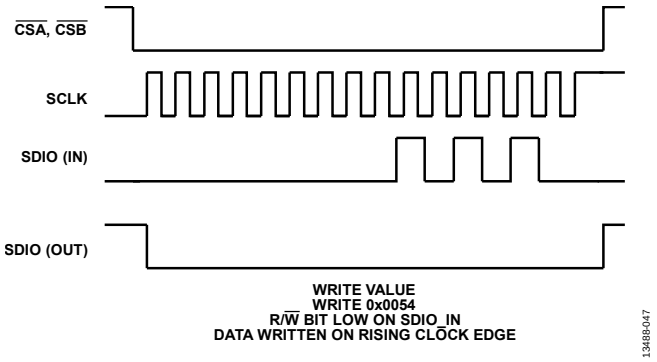


Figure 54. Write Gain Control Word

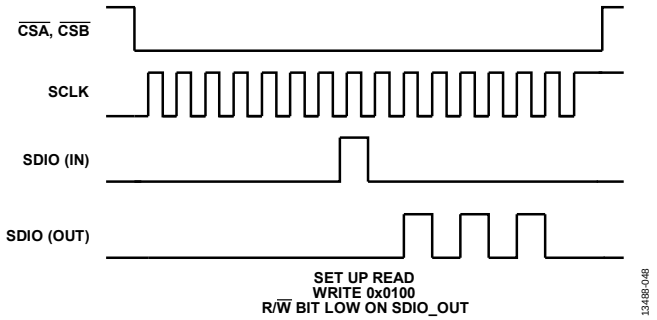


Figure 55. Write Logic 1 into R/$\overline{W}$ Bit

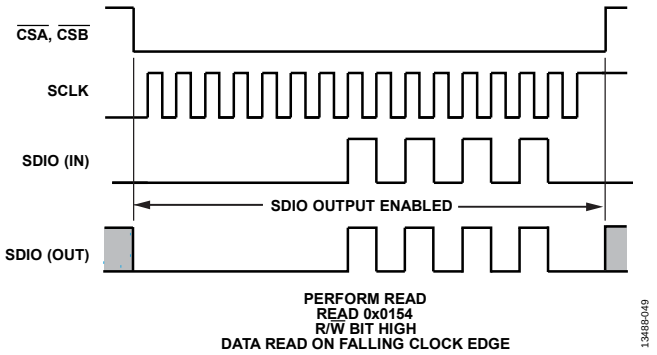


Figure 56. Perform Read

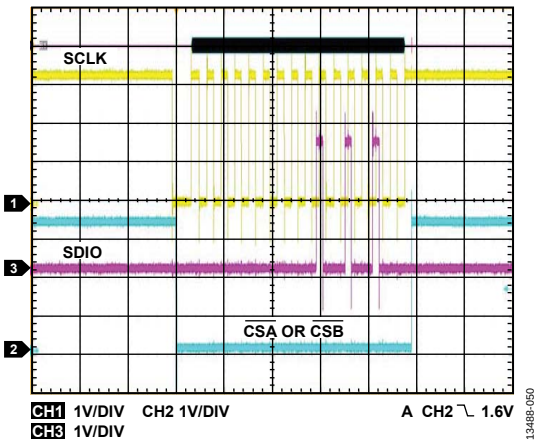


Figure 57. Write Gain Control Value, 0x0054

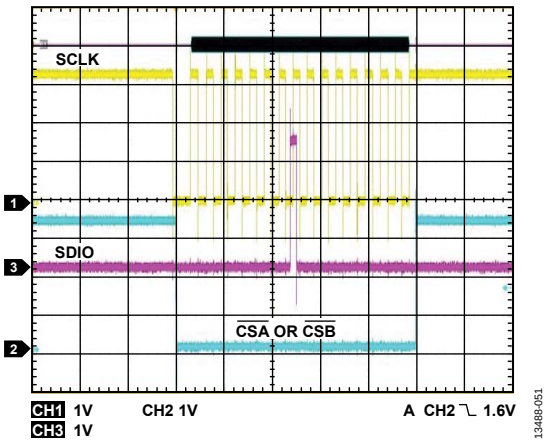


Figure 58. Write Read Setup Value, 0x0100

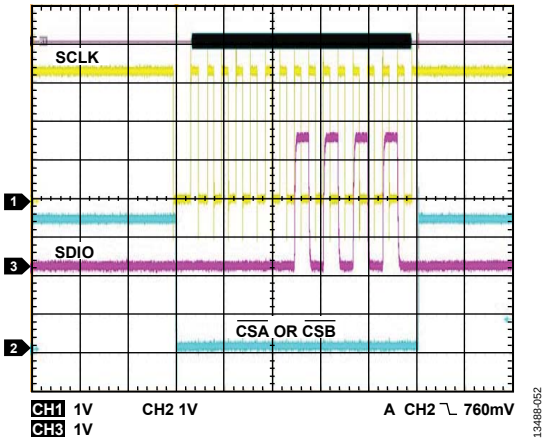


Figure 59. Read Back Value, 0x0154

ADC INTERFACING

A typical data acquisition system using the ADL5205 together with an antialiasing filter and an ADC is shown in Figure 60. The main role of the filter after the amplifier is for attenuating the broadband noise and out-of-band harmonics generated by the amplifier. Component values for a 500 MHz acquisition bandwidth are listed in Table 10. Without this filter, the out-of-band noise and distortion components alias back into the Nyquist band, resulting in a reduction of signal-to-noise ratio. The design of the filter preceding the ADL5205 amplifier is more specific to the system rejection requirements for the acquisition system,

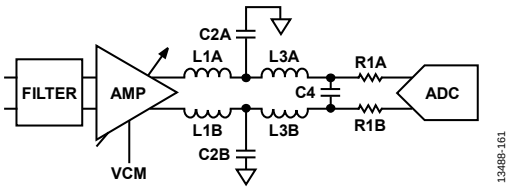


Figure 60. ADC Interface (One of Two Channels Shown)

Table 10. Component Values for a 500 MHz Acquisition System

Component	Value	Description/Comments
Amplifier	½ ADL5205	One channel
L1A, L1B	22 nH	Q ≥ 50 at 500 MHz
C2A, C2B	6.8 pF	Final value depends on PCB parasitics
L3A, L3B	22 nH	Q ≥ 50 at 500 MHz
C4	1.5 pF	Final value depends on PCB parasitics
R1A, R1B	10 Ω	Not applicable
ADC	½ AD9680	One channel, input impedance set to 100 Ω

NOISE FIGURE vs. GAIN SETTING

Because of the architecture of the ADL5205, the noise figure does not degrade significantly for the first 12 dB of gain reduction from the maximum gain setting. The noise figure increases by 2 dB only during the first 12 dB of gain reduction, after which it resumes the 1 dB degradation for each dB of gain reduction.

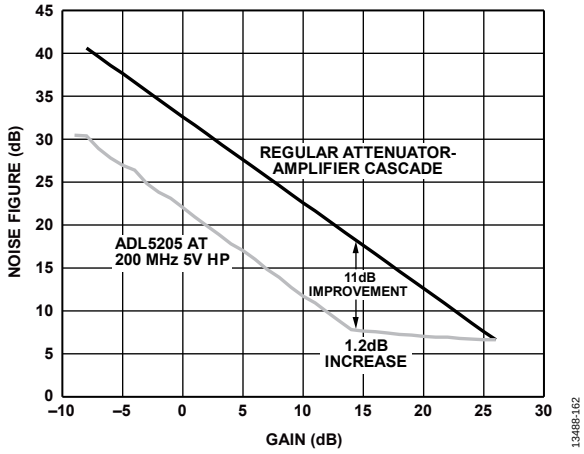


Figure 61. Noise Figure vs. Gain

EVALUATION BOARD

OVERVIEW

The ADL5205-EVALZ evaluation board allows the manual control of the ADL5205 device through the serial and the parallel interface ports, as well as the control of the device through the USB port on a Microsoft® Windows® PC via the system demonstration platform (SDP) interface board. A 3.3 V low dropout (LDO) voltage regulator supplies the logic circuits when the device is running on a 5 V supply.

On-board baluns convert single-ended input signals to differential form for input to the device and convert the differential output signals of the device to single-ended form for output. To bypass these baluns, rearrange the 0 Ω resistors on the board as described in the Signal Inputs and Outputs section.

The ADL5205-EVALZ provides all of the support circuitry required to operate the ADL5205 in its various modes and configurations. Figure 62 shows the typical bench setup used to evaluate the performance of the ADL5205.

POWER SUPPLY INTERFACE

The ADL5205-EVALZ evaluation board requires either a 3.3 V or 5 V power supply, and an optional negative supply to pull down the output common-mode dc level to match the ADCs that require a lower common-mode level. If an external 3.3 V supply is used, connect it to the test point labeled 3P3V. If a 5 V supply is used, connect it to the test point labeled 5V. Similarly, if an external negative supply is used, connect it to the VNEG test point shown in Figure 62.

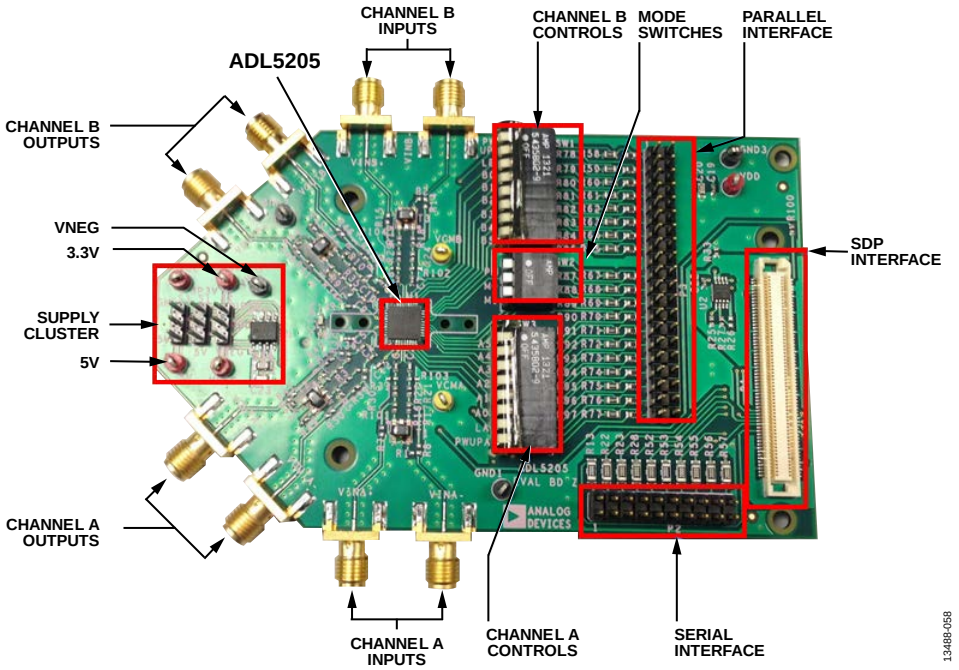


Figure 62. ADL5205-EVALZ Evaluation Board

The power supply jumper configurations (S1 to S3) required for selecting the evaluation board analog supply (V_{CC}) and digital supply (V_{DD}) from the external 3.3 V or 5 V power supply are shown in Table 11. When using a 5 V supply, enable the on-board 3.3 V voltage regulator and select it using the S3 and S2 jumpers, respectively, to provide digital supply (V_{DD}) to the pull-up resistors for logic signals.

Table 11. Power Supply Selection Jumpers

Jumper	Function	Supply Selection	
		V_{CC} = 3.3 V	V_{CC} = 5 V
S1	V_{CC} selection	3P3V	5V
S2	V_{DD} selection	3P3V	VREG
S3	V_{DD} LDO enable	AGND	5V

SIGNAL INPUTS AND OUTPUTS

Signal inputs and outputs for each channel come through a pair of SMA connectors. In the default configuration, on-board baluns convert single-ended signals from VINA− and VINB− into differential signals to the device. Similarly, differential output signals from the device are converted through the on-board baluns into single-ended form to the VOUTA+ and VOUTB+ connectors.

MANUAL CONTROLS

Three sets of switches provide the manual control of the states of the device. Their functions are listed in Table 12. When the individual switch is in the up position, the signal controlled by the switch is set to logic high.

Table 12. Switch Block Functions

Switch Block	Function	Device Pin No.
SW1	Channel B control (eight positions)	
Position 1	PWUPB	17
Position 2	LATCHB	14
Position 3	B0	13
Position 4	B1	12
Position 5	B2	11
Position 6	B3	10
Position 7	B4	9
Position 8	B5	8
SW2	Mode control (three positions)	
Position 1	Power mode (PM)	6
Position 2	MODE0 (M0)	5
Position 3	MODE1 (M1)	4
SW3	Channel A control (eight positions)	
Position 1	A5	3
Position 2	A4	2
Position 3	A3	1
Position 4	A2	40
Position 5	A1	39
Position 6	A0	38
Position 7	LATCHA	37
Position 8	PWUPA	34

Mode Switches

When the power mode (PM) switch is up (logic high or Logic 1), the device is in low power mode. When the switch is down (logic low or Logic 0), the device is in high performance mode.

MODE1 and MODE0 (labeled M1 and M0 on the PCB) select one of three interface modes for the device (parallel, serial/SPI, or up/down mode), as shown in Table 13. There is no functional difference between the mode switch settings of 10 and 11.

Table 13. Mode Switch Settings

MODE1, MODE0	Interface
00	Parallel
01	Serial (SPI)
10	Up/down
11	Up/down

Channel Control Switches

The channel control switches include PWUPA, LATCHA, and A5 to A0 for Channel A and PWUPB, LATCHB, and B5 to B0 for Channel B.

PWUPA and PWUPB are the up positions (logic high) that turn on their respective channels. When PM is set to logic low (high performance mode), the total current consumption increases by approximately 81 mA (that is, one half of the difference between the enabled current of 175 mA and the disabled current of 14 mA) when each channel is enabled. When the PM is set to logic high (low power mode), the total current consumption increases by approximately 61 mA (that is, one half of the difference between the enabled current of 135 mA and the disabled current of 14 mA) when each channel is enabled.

The LATCHA and LATCHB switches are used with the gain control input bits (A5 to A0 and B5 to B0) to control the corresponding channel voltage gain. When these switches are in the down (logic low) position, the gain changes with the position of the gain control switches. When these switches are in the up position, the last gain setting is latched into the corresponding channel of the ADL5205, and the gain stops changing.

For Bits[A5:A0] and Bits[B5:B0], the following equation determines the voltage gain of each channel of the ADL5205:

$$Gain = 26 - [A5:A0] \text{ dB}$$

where [*A5:A0*] is the value representing the binary string formed by Bits[A5:A0] from 0 to 35. When this value exceeds 35, the gain is set to minimum (−9 dB). The voltage gain for Channel B is changed by Bits[B5:B0] in the same manner.

PARALLEL INTERFACE

The functions of Parallel Interface Connector P3 are identical to those of the switches in the switch block. The pinout of the Parallel Interface Connector P3 is listed in Table 14. Logic levels on the P3 pins override the corresponding switch setting. As a result, the switches for PWUPA and PWUPB must be in the up position when using the parallel interface to control the device.

Table 14. Parallel Interface Pinout (P3)

Pin Number	Function
1	PWUPB
2	AGND
3	LATCHB
4	AGND
5	B0
6	AGND
7	B1
8	AGND
9	B2
10	AGND
11	B3
12	AGND
13	B4
14	AGND
15	B5
16	AGND
17	V_{DD}
18	AGND
19	Power mode (PM)
20	AGND
21	MODE0
22	AGND
23	MODE1
24	AGND
25	A5
26	AGND
27	A4
28	AGND
29	A3
30	AGND
31	A2
32	AGND
33	A1
34	AGND
35	A0
36	AGND
37	LATCHA
38	AGND
39	PWUPA
40	AGND

SERIAL INTERFACE

When the mode switches are in the 01 position, the ADL5205 operates in the serial/SPI mode. The pins that are relevant in the serial/SPI mode are brought out to Serial Interface Connector P2. The pinout for Serial Interface Connector P2 is listed in Table 15. Note that only four pins (plus AGND) are used for the SPI, and they include the following:

- $\overline{CSA}$ and $\overline{CSB}$ are the active low serial port enable pins for Channel A and Channel B, respectively.
- SDIO is the serial data input and output line. SDIO is a bidirectional pin.
- SCLK is the serial clock pin.

For detailed operations and timing diagrams of the serial port interface, see the Serial Peripheral Interface (SPI) section. These signals operate at 3.3 V logic levels.

The $\overline{CSA}$ and $\overline{CSB}$ lines can be tied together to program both channels at the same time.

Table 15. Serial Interface Connector (P2) Pinout

Pin Number	Function
1	PWUPA
2	Not applicable
3	FA_A
4	Not applicable
5	$\overline{CSA}$
6	Not applicable
7	PM
8	Not applicable
9	SDIO
10	Not applicable
11	SCLK
12	Not applicable
13	$\overline{CSB}$
14	Not applicable
15	FA_B
16	Not applicable
17	PWUPB
18	Not applicable
19	AGND
20	Not applicable

STANDARD DEVELOPMENT PLATFORM (SDP) INTERFACE

The ADL5205-EVALZ connects to the universal serial bus (USB) port on a Windows-based PC through an SDP board. The SDP interface board plugs into the P1 connector on the ADL5205-EVALZ evaluation board and provides all the digital handshaking to communicate with the USB. Use the SDP with the ADL5205 control software on the PC.

To control the ADL5205 through the USB to SDP interface, nine jumpers must be inserted from the odd numbered pins (Pin 1, Pin 3, Pin 5, Pin 7, Pin 9, Pin 11, Pin 13, Pin 15, and Pin 17) to the even numbered pins (Pin 2, Pin 4, Pin 6, Pin 8, Pin 10, Pin 12, Pin 14, Pin 16, and Pin 18 on the P2 connector, as shown in Figure 63. No jumper is needed for Pin 19 and Pin 20.

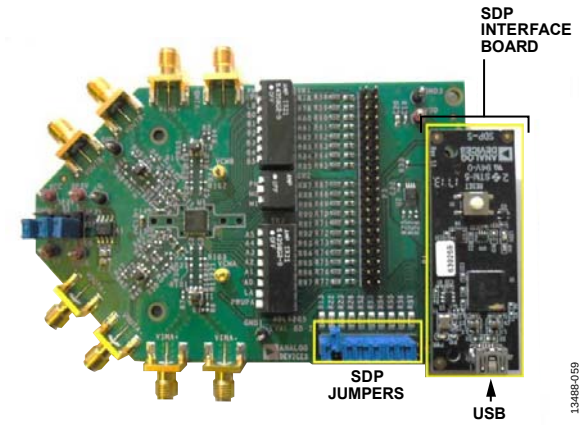


Figure 63. SDP Interface Board

A dynamically loadable library (DLL), sdpApi1.dll, provides the software interface to the actual hardware. The control program, using the USB interface, can communicate with the hardware through interface functions in this DLL.

EVALUATION BOARD CONTROL SOFTWARE

Two separate programs are available for use with a Windows-based PC to control the ADL5205 through the USB to SDP interface: a command line control program and a program with a graphical user interface.

COMMAND LINE CONTROL PROGRAM

The adl5205_regw_x_x.exe, where x_x represents the revision of the program, is a command line program that takes the 8-bit value represented by the command line argument and writes into the control register of the ADL5205. The syntax for the program is shown in Figure 64, which contains a sample run of the command line control program, showing the help listing.

GRAPHICAL USER INTERFACE (GUI) PROGRAM

The adl5205_ctrlsw_y_y.exe, where y_y represents the revision of the program, is a GUI program that allows the control of the ADL5205 functions through an on-screen display. The ADL5205 gain and modes of operation can be controlled interactively using icons on the computer screen. A typical display from the GUI control is shown in Figure 65, and the corresponding control functions are listed in Table 16.

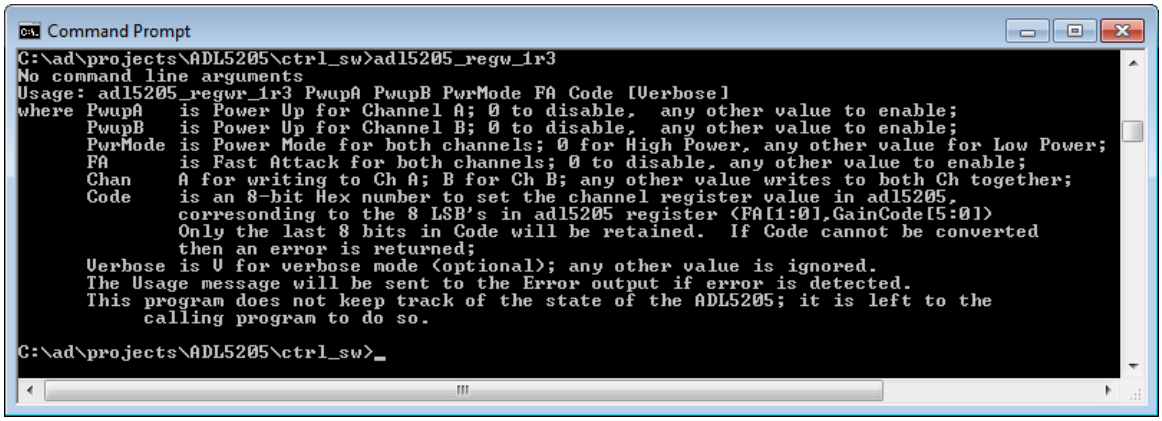


Figure 64. Sample Listing Showing Usage of the Command Line Program

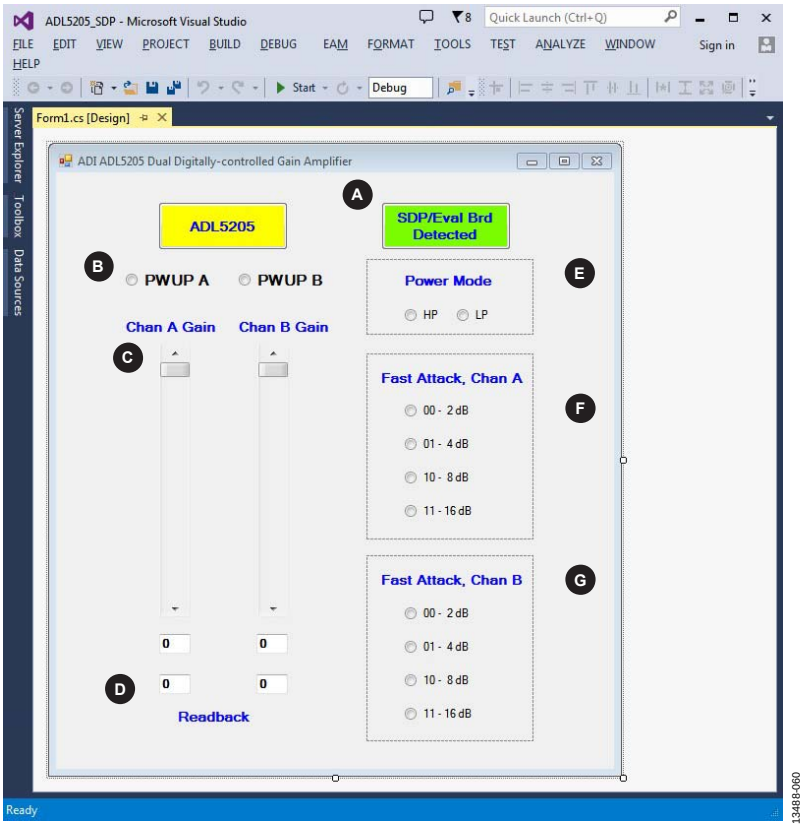


Figure 65. Main Screen of the ADL5205 Control Software

Table 16. Features on the Control Software Main Screen

Feature	Description
A	SDP and evaluation board connection status
B	Gain setting displays
C	Gain control for Channel A and Channel B
D	Gain setting readback
E	Power mode (high performance (HP) or low power (LP))
F	Channel A Fast attack step size
G	Channel B fast attack step size

EVALUATION BOARD SCHEMATICS AND LAYOUT

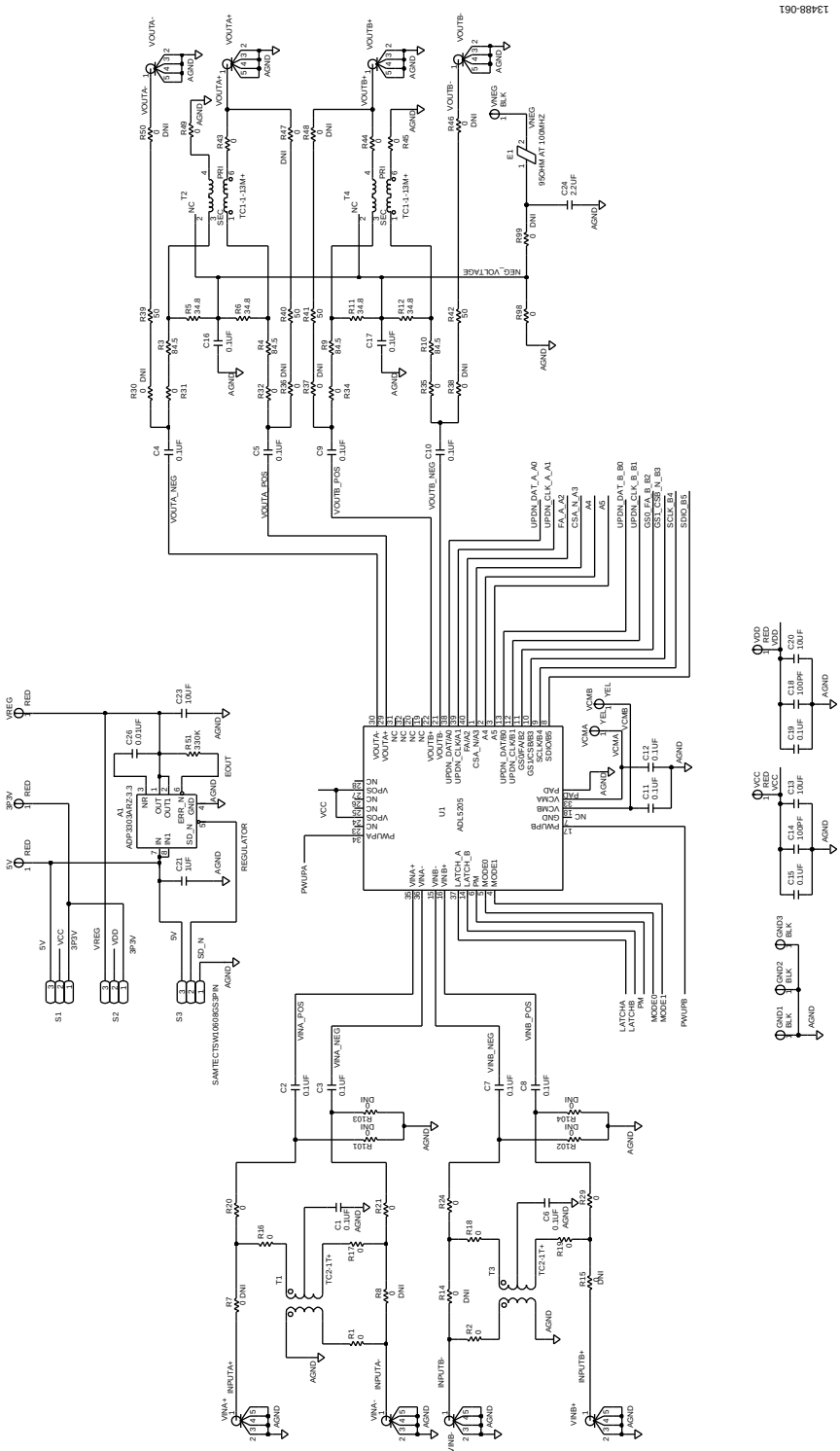


Figure 66. ADL5205-EVALZ Evaluation Board Schematic, Page 1

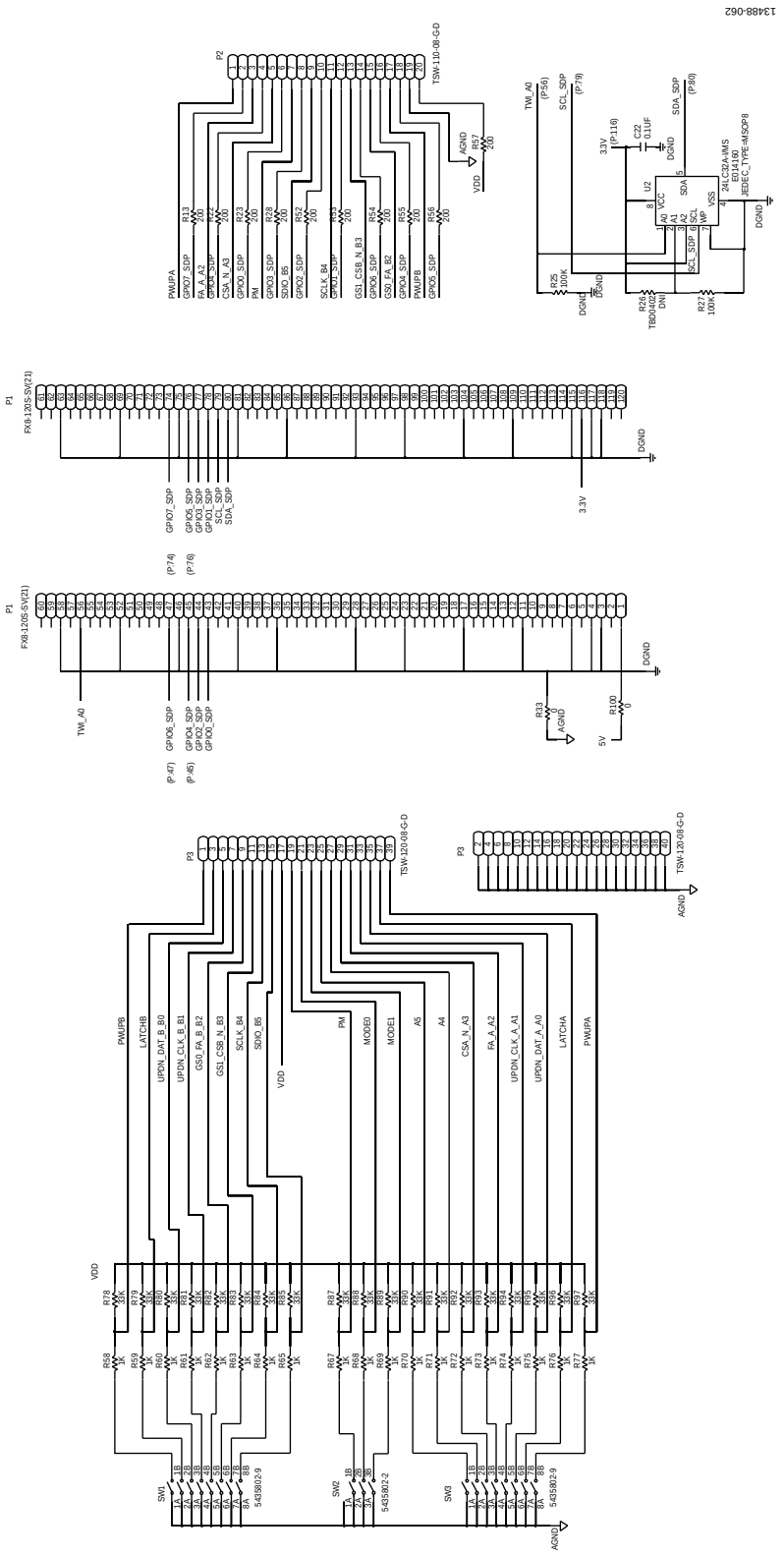


Figure 67. ADL5205-EVALZ Evaluation Board Schematic, Page 2

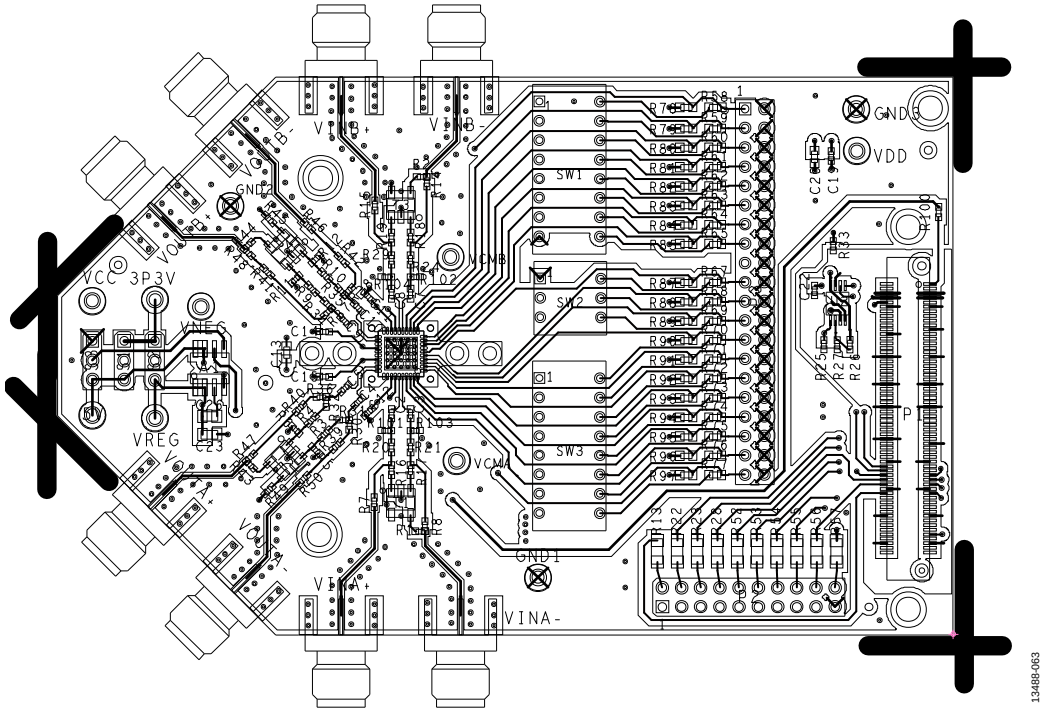


Figure 68. ADL5205-EVALZ Evaluation Board Side A

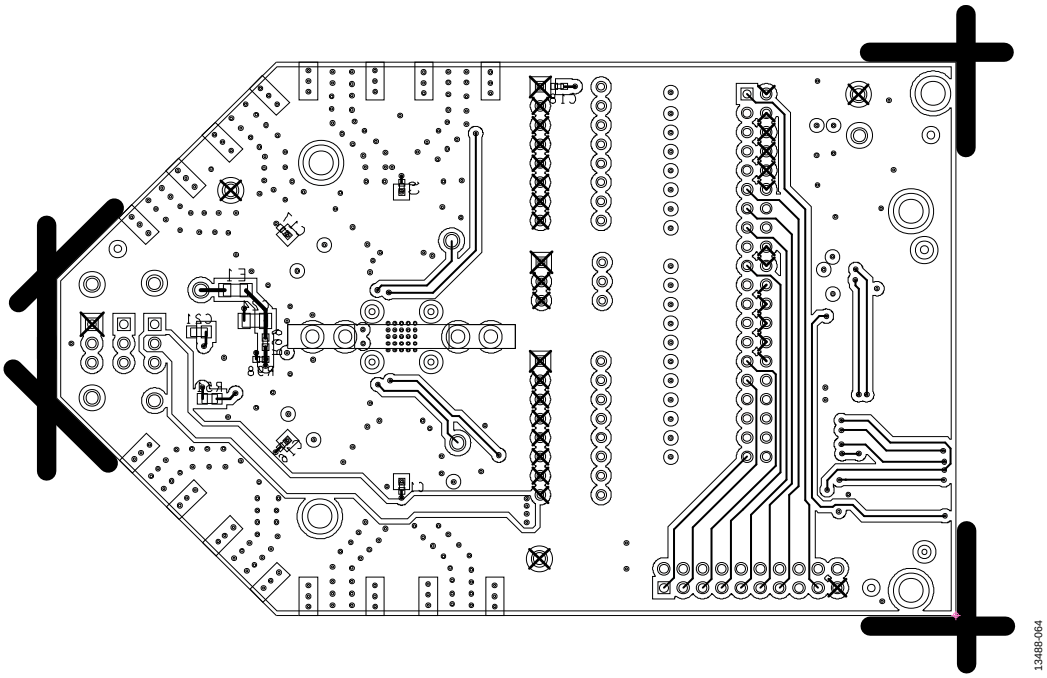


Figure 69. ADL5205-EVALZ Evaluation Board Side B

BILL OF MATERIALS

Table 17. Bill of Materials

Qty.	Description	Reference Designator	Manufacturer	Part No.
1	PCB	Not applicable	Analog Devices	08_039771B
5	Connectors, PCB test points, red, CNLOOPTP	5V, VCC, VDD, 3P3V, VREG	Components Corporation	TP-104-01-02
1	IC, high accuracy, 200 mA, low dropout linear regulator, SO8	A1	Analog Devices	ADP3303ARZ-3.3
17	Capacitors, ceramic, X7R 0402, 0.1 µF, C0402, 10%, 16 V	C1 to C12, C15 to C17, C19, C22	Murata	GRM155R71C104KA88D
2	Capacitors, ceramic, X5R 0603, 10 µF, C0603, 20%, 6.3 V	C13, C20	Murata	GRM188R60J106ME47D
2	Capacitors, ceramic, monolithic chip, C0G, 100 pF, C0402, 5%, 50 V	C14, C18	Murata	GRM1555C1H101JA01D
1	Capacitors, ceramic, 0805 X7R, 1 µF, C0805H53, 10%, 50 V	C21	Murata	GRM21BR71H105KA12L
1	Capacitor, ceramic, X5R, 10 µF, C0805H60, 10%, 10V	C23	KEMET	C0805C106K8PACTU
1	Capacitor, ceramic, monolithic X7R, 2.2 µF, C1206H71, 10%, 50 V	C24	Murata	GRM31CR71H225KA88L
1	Capacitor, ceramic, C0G 0805, 0.01 µF, C0805, 5%, 50 V	C26	Murata	GCM2195C1H103JA16D
1	Inductor chip ferrite bead, 0.3 Ω, maximum dc resistance, 0.5 A, 95 Ω at 100 MHz, L1206-3	E1	Laird Technologies, Inc.	LF1206E152R-10
4	Connectors, PCB test point black, CNLOOPTP	GND1to GND3, VNEG	Components Corporation	TP-104-01-00
1	Connectors, PCB vertical type receptacle SMD, FX8-120S-SV(21), CNHRSFX8-120S-SV	P1	Hirose	FX8-120S-SV(21)
1	Connectors, PCB BERG header ST male 20P, TSW-110-08-G-D, CNBERG2X10H330LD36	P2	Samtec	TSW-110-08-G-D
1	Connectors, PCB header 40P male, TSW-120-08-G-D, CNSAMTECTSW-120-08-T-D	P3	Samtec	TSW-120-08-G-D
21	Resistors, chip SMD jumper, 0 Ω, R0402, 5%	R1, R2, R16 to R21, R24, R29, R31 to R35, R43 to R45, R49, R98, R100	Panasonic	ERJ-2GE0R00X
4	Resistors, chip SMD ,0402, 84.5 Ω, R0402, 1%	R3, R4, R9, R10	Panasonic	ERJ-2RKF84R5X
8	Resistors, high frequency chip, 0402, 50 Ω, R0402, 1%	R39 to R42, R101 to R104	Vishay	FC0402E50R0FST1
4	Resistors, precision thick film chip, 34.5 Ω, R0402, 1%	R5, R6, R11, R12	Panasonic	ERJ-2RKF34R5X
10	Resistors, film SMD 1206, 200 Ω, R1206, 2%	R13, R22, R23, R28, R52 to R57	Welwyn	200R WCR 1206
2	Resistors, precision thick film chip, R0402, 100 kΩ, R0402, 1%	R25, R27	Panasonic	ERJ-2RKF1003X
1	Resistors, film SMD 0805, 330 kΩ, R0805, 5%	R51	Panasonic	ERJ-6GEYJ334V
19	Resistors, thick film chip, 1 kΩ, R0603, 1%	R58 to R65, R67 to R77	Vishay	CRCW06031K00FKEAHP
19	Resistors, chip SMD 0603, 33 kΩ, R0603, 0.5%	R78 to R85, R87 to R97	SUSUMU	RR0816P-333-D
3	Connectors, PCB BERG header ST male 3P, SAMTECTSW10608GS3PIN, CNBERG1X3H205LD36	S1 to S3	Samtec	TSW-103-08-G-S
2	Switches, DIP SPST, side actuated, 5435802-9, SWL880W380H310	SW1, SW3	TE Connectivity	5435802-9
1	Switch, SPST DIP, three position AU (ALCOSWITCH-7000), 5435802-2, SWSQ380H310	SW2	TE Connectivity	5435802-2
2	XFMR RF 1:1, TC1-1-13M+, AT224-1	T2, T4	Mini-Circuits	TC1-1-13M+
2	XFMR RF 2:1, TC2-1T+, AT224-1	T1, T3	Mini-Circuits	TC2-1T+
1	IC, 35 dB step size programmable DGA, ADL5205, QFN40_6X6	U1	Analog Devices	ADL5205
1	IC, 32 kb serial EEPROM, 24LC32A-I/MS, MSOP8	U2	Microchip Technology	24LC32A-I/MS
2	Connectors, PCB test point yellow, CNLOOPTP	VCMA, VCMB	Components Corporation	TP-104-01-04
8	Connectors, PCB coaxial SMA end launch, JOHNSON142-0701-801, CNJOHNSON142-0701-801	VINA+, VINA−, VINB+, VINB−, VOUTA+, VOUTA−, VOUTB+, VOUTB−	Johnson	142-0701-801

OUTLINE DIMENSIONS

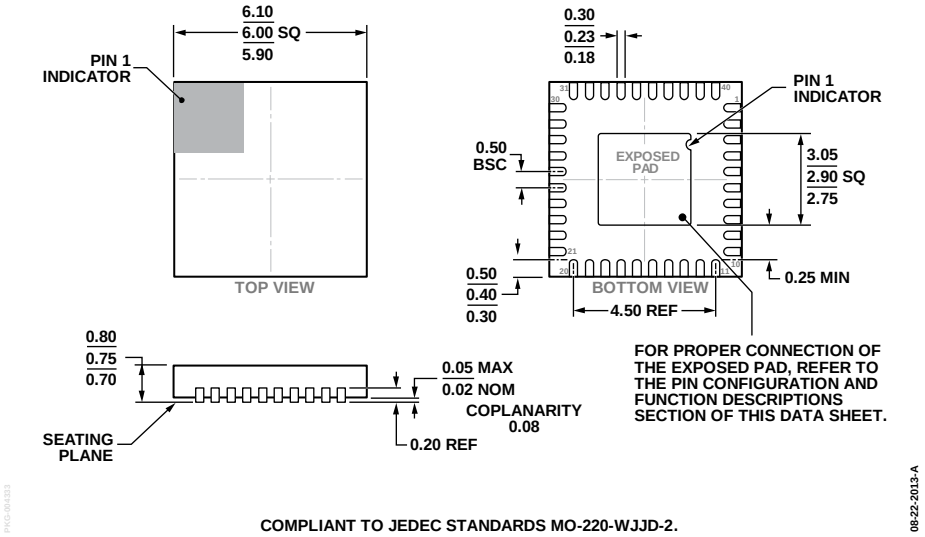


Figure 70. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5205ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-16
ADL5205-EVALZ		Evaluation Board	

[1] Z = RoHS-Compliant Part.