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MC74VHC157

Quad 2-Channel Multiplexer

The MC74VHC157 is an advanced high−speed CMOS quad 2−channel multiplexer, fabricated with silicon gate CMOS technology. It achieves high−speed operation similar to equivalent Bipolar−Schottky TTL, while maintaining CMOS low−power dissipation.

It consists of four 2−input digital multiplexers with common select (S) and enable ($\overline{E}$) inputs. When $\overline{E}$ is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 4.1 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 82 FETs
- These Devices are Pb−Free and are RoHS Compliant

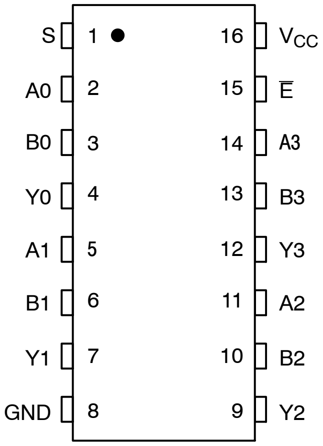

Figure 1. Pin Assignment

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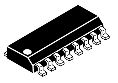
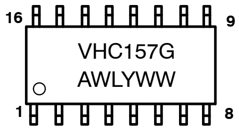
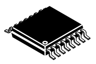
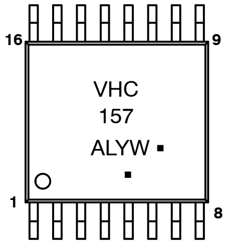


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



VHC157 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC157DR2G	SOIC−16	2500 Units/Reel
MC74VHC157DTR2G	TSSOP−16	2500 Units/Reel

May, 2011 − Rev. 6

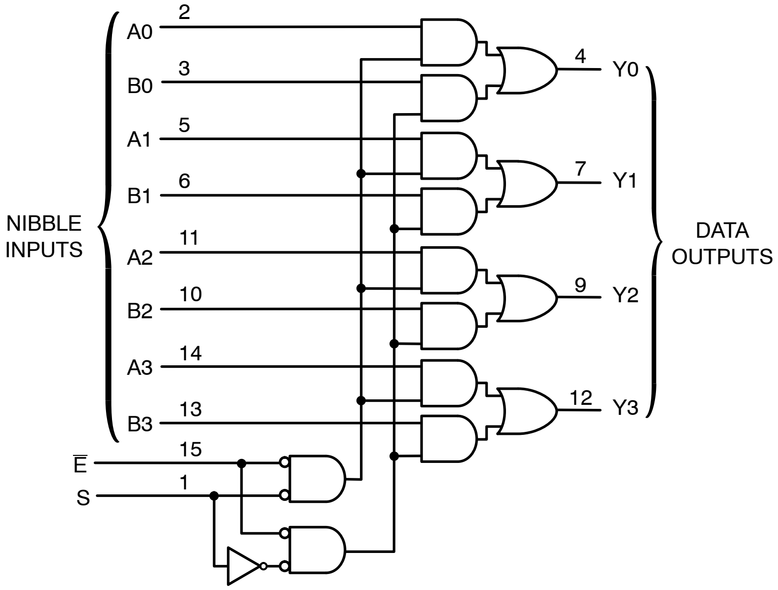


Figure 2. Expanded Logic Diagram

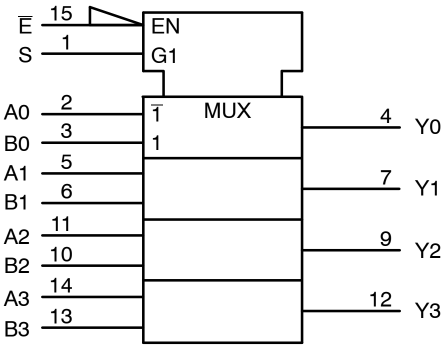


Figure 3. IEC Logic Symbol

FUNCTION TABLE

Inputs		Outputs
$\overline{E}$	S	Y0 – Y3
H	X	L
L	L	A0 – A3
L	H	B0 – B3

A0 – A3, B0 – B3 = the levels of the respective Data–Word Inputs.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V_I	DC Input Voltage		-0.5 to V_{CC} $+7.0$	V
V_O	DC Output Voltage		-0.5 to V_{CC} $+7.0$	V
I_{IK}	DC Input Diode Current	$V_I < GND$	-20	mA
I_{OK}	DC Output Diode Current	$V_O < GND$	±20	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		$+150$	°C
θ_{JA}	Thermal Resistance		250	°C/W
P_D	Power Dissipation in Still Air at 85°C		250	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
$I_{Latch-Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 5)	±500	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage	(Note 6)	0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		-55	125	°C
t_r, t_f	Input Rise or Fall Time	$V_{CC} = 3.3\ V \pm 0.3\ V$ $V_{CC} = 5.0\ V \pm 0.5\ V$	0 0	100 20	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high–logic voltage level or a low–logic input voltage level.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

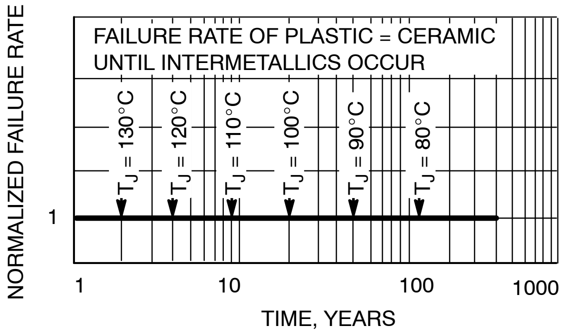


Figure 4. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	T_A = 25°C			$T_A \le 85$°C		–55°C $\le T_A \le$ 125°C		Unit
			(V)	Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0 3.0 to 5.5	1.5 0.7 V_{CC}			1.5 0.7 V_{CC}		1.5 0.7 V_{CC}		V
V_{IL}	Low–Level Input Voltage		2.0 3.0 to 5.5			0.5 0.3 V_{CC}		0.5 0.3 V_{CC}		0.5 0.3 V_{CC}	V
V_{OH}	High–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = –4 mA I_{OH} = –8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V_{OL}	Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = 4 mA I_{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			4.0		40.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Characteristic			T_A = 25°C			$T_A \le 85$°C		–55°C $\le T_A \le$ 125°C		Unit
		Test Conditions		Min	Typ	Max	Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to B to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF C_L = 50 pF		6.2 8.7	9.7 13.2	1.0 1.0	11.5 15.0	1.0 1.0	11.5 15.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15 pF C_L = 50 pF		4.1 5.6	6.4 8.4	1.0 1.0	7.5 9.5	1.0 1.0	7.5 9.5	
t_{PLH}, t_{PHL}	Propagation Delay, S to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF C_L = 50 pF		8.4 10.9	13.2 16.7	1.0 1.0	15.5 19.0	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15 pF C_L = 50 pF		5.3 6.8	8.1 10.1	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{E}$ to Y	V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF C_L = 50 pF		8.7 11.2	13.6 17.1	1.0 1.0	16.0 19.5	1.0 1.0	16.0 19.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15 pF C_L = 50 pF		5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
C_{IN}	Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 7)	20	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns; $C_L = 50$ pF; $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

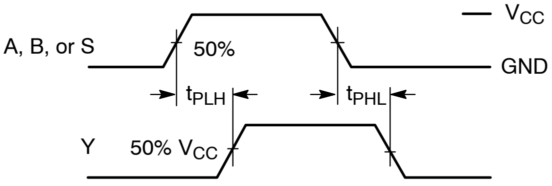


Figure 5. Switching Waveform

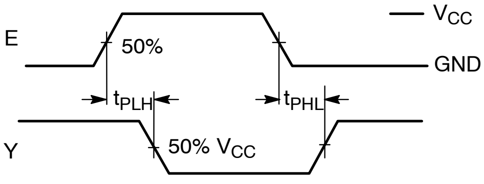
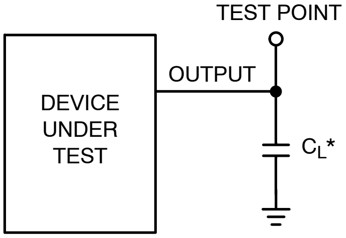


Figure 6. Inverting Switching



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

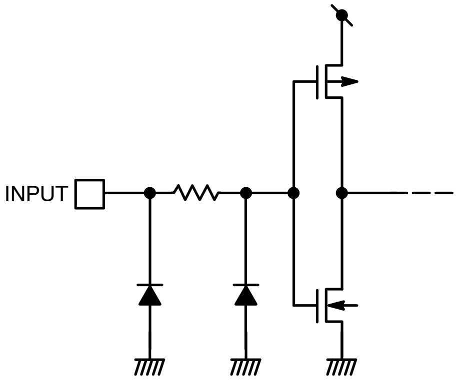


Figure 8. Input Equivalent Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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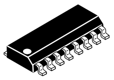
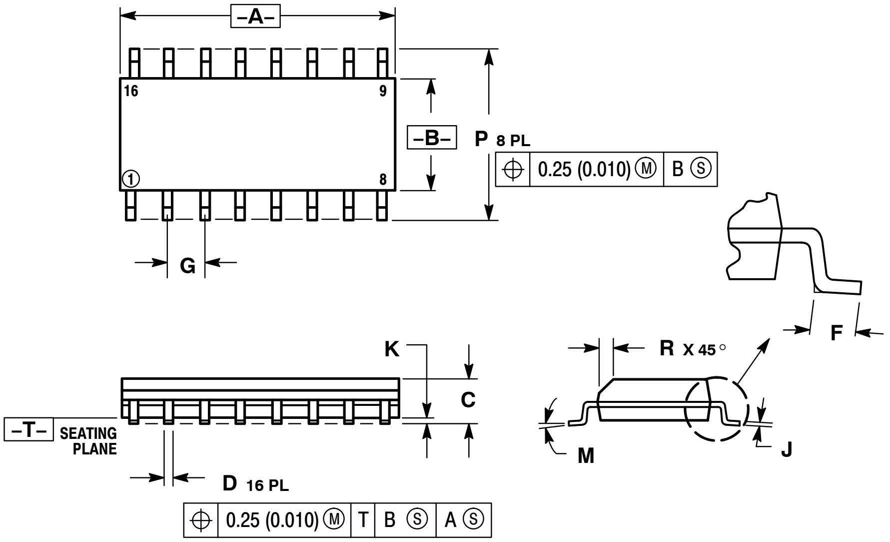


SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

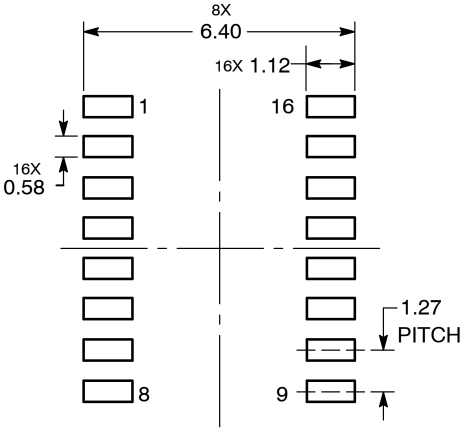
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**SOIC−16**	**PAGE 1 OF 1**

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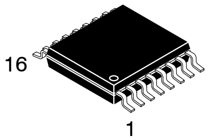
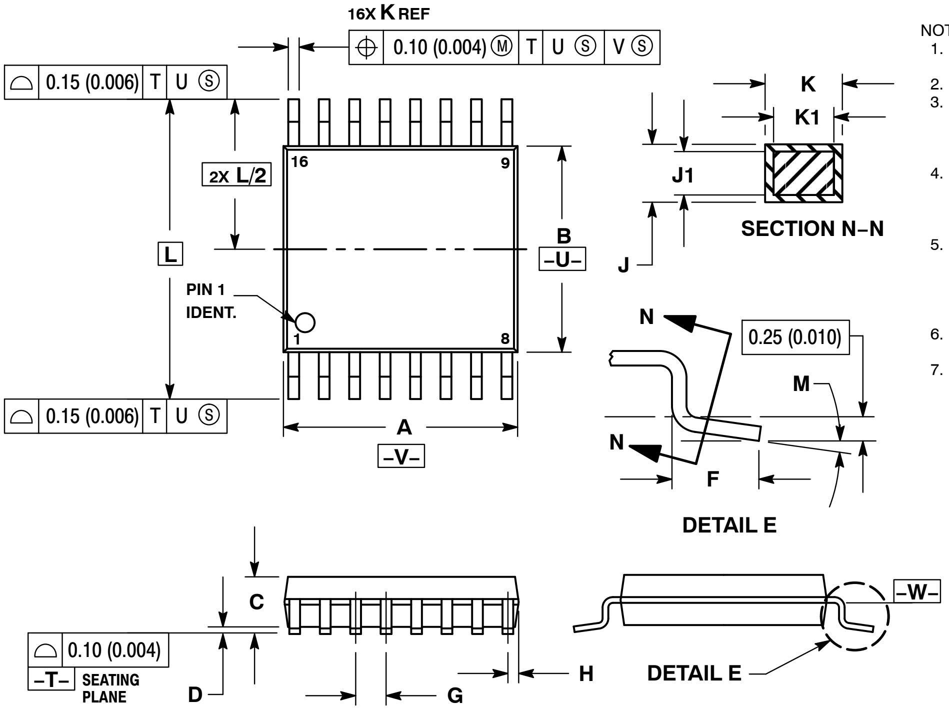


SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

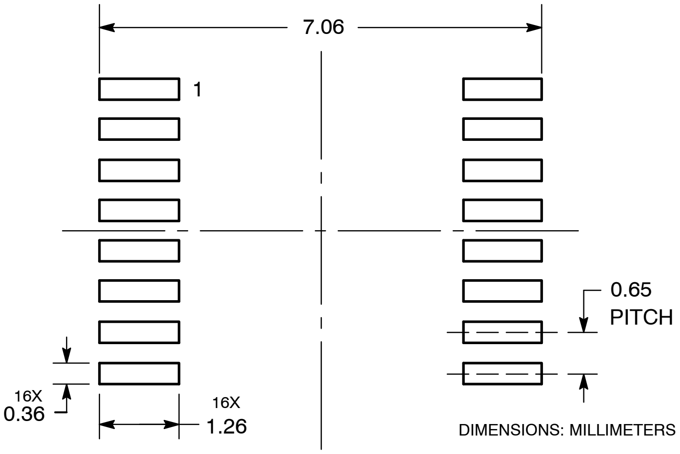
DATE 19 OCT 2006



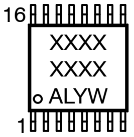
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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