



PSMN2R8-40BS

N-channel 40 V 2.9 mΩ standard level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

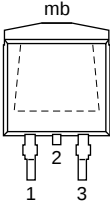
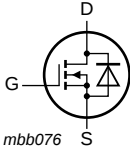
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	40	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	[1]	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	211	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 100 °C; see Figure 13 ; see Figure 14	-	3.58	4.2	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; see Figure 14	-	2.47	2.9	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 10 A; V _{DS} = 20 V; see Figure 15 ; see Figure 16	-	17	-	nC
Q _{G(tot)}	total gate charge		-	71	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 40 V; unclamped; R _{GS} = 50 Ω	-	-	407	mJ

[1] Continuous current rating is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R8-40BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

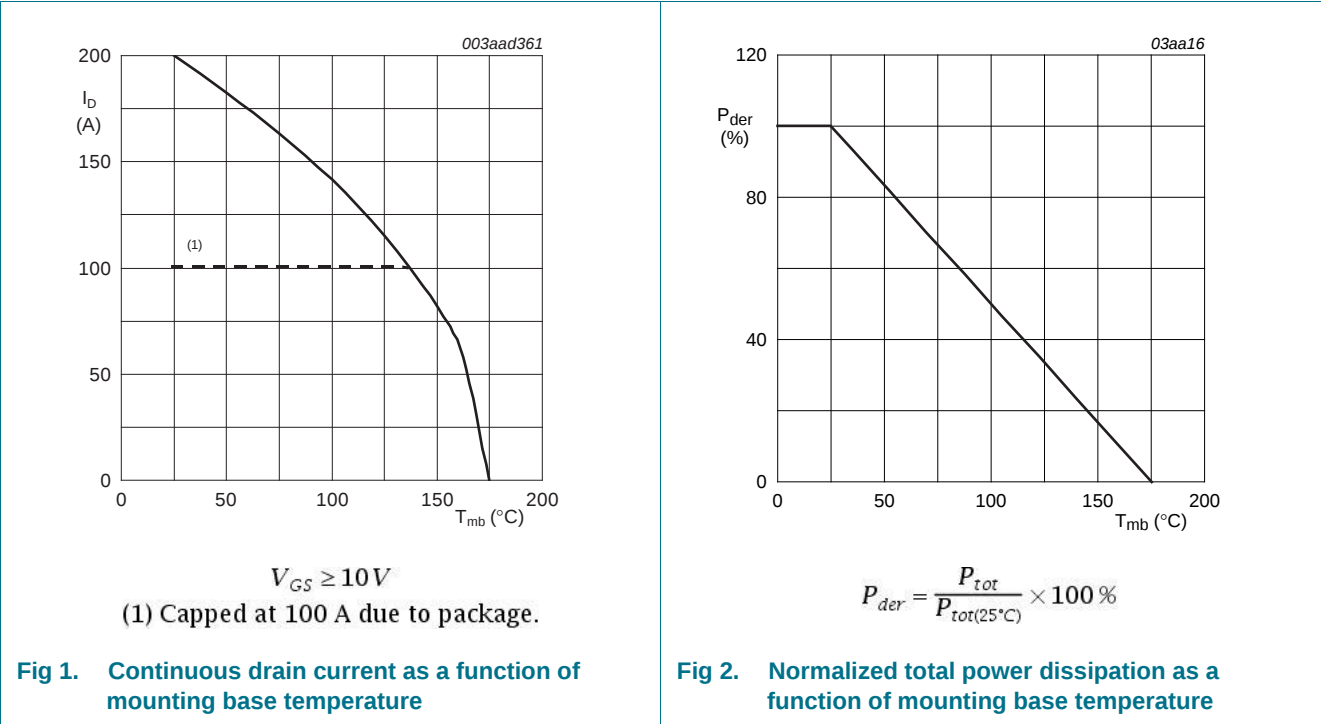
Type number	Marking code
PSMN2R8-40BS	PSMN2R8-40BS

5. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	40	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1]	100	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	797	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	211	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1]	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	797	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 40 V; unclamped; R _{GS} = 50 Ω	-	407	mJ

[1] Continuous current rating is limited by package.



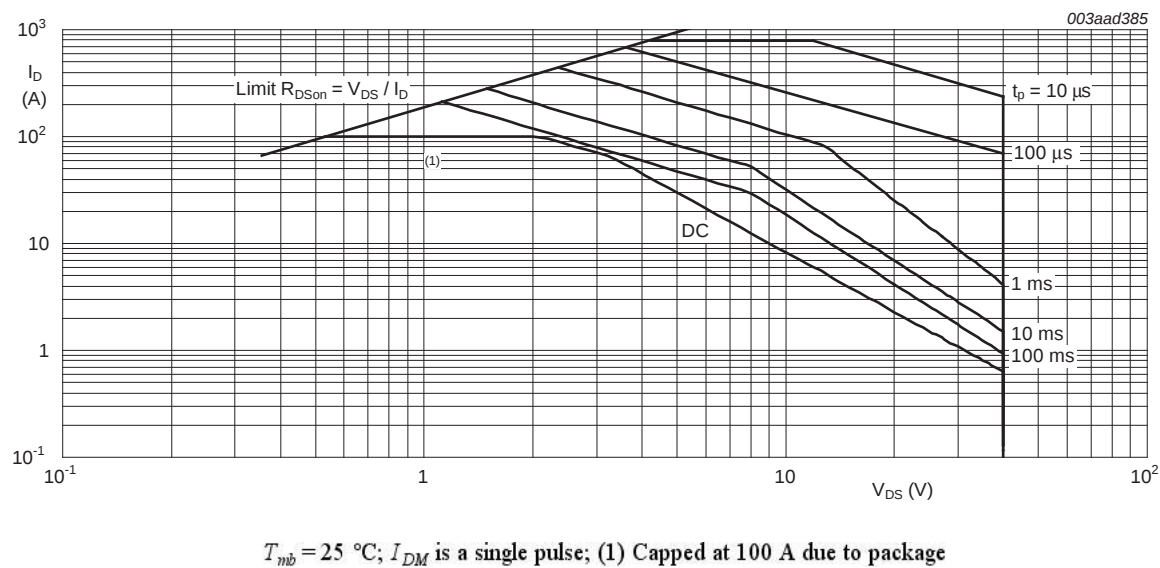


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.4	0.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

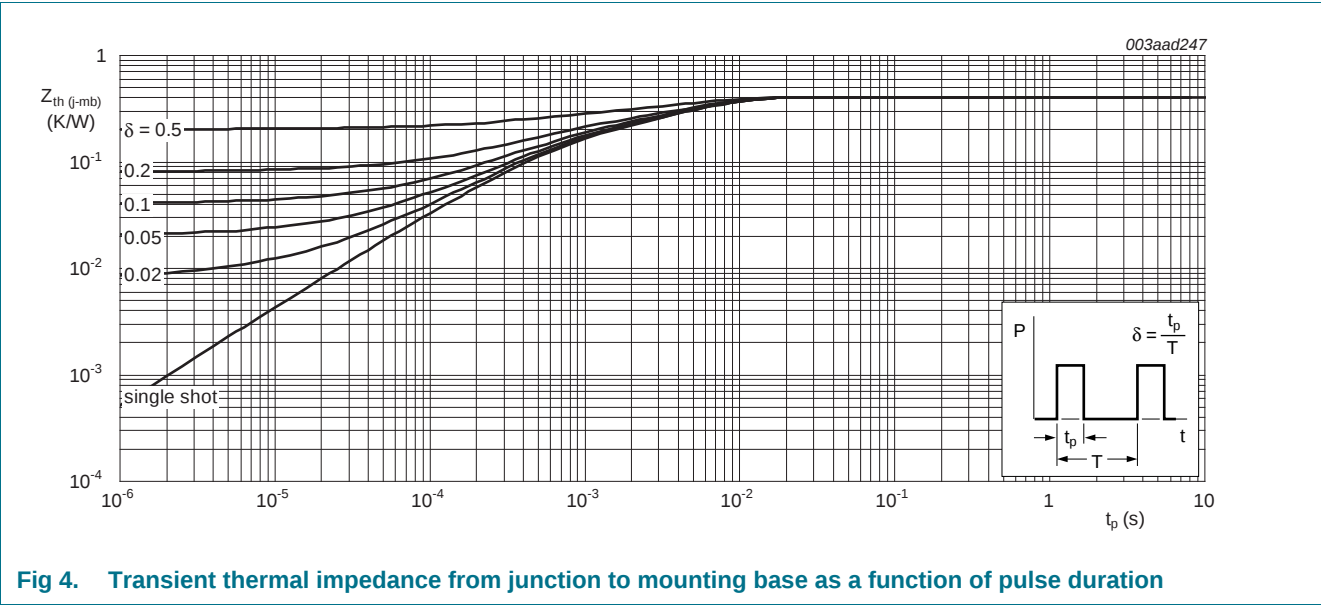


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	36	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 10 ; see Figure 11	-	-	4.6	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 175 ^\circ C$; see Figure 10 ; see Figure 12	1	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 10 ; see Figure 11	2.3	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	0.3	10	μA
		$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 125 ^\circ C$	-	-	150	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 100 ^\circ C$; see Figure 13 ; see Figure 14	-	3.58	4.2	mΩ
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 175 ^\circ C$; see Figure 13 ; see Figure 14	-	4.94	5.8	mΩ
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 25 ^\circ C$; see Figure 14	-	2.47	2.9	mΩ
R_G	internal gate resistance (AC)	$f = 1 MHz$	-	0.7	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	61	-	nC
		$I_D = 10 A$; $V_{DS} = 20 V$; $V_{GS} = 10 V$; see Figure 15 ; see Figure 16	-	71	-	nC
Q_{GS}	gate-source charge		-	21	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	13	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	8.5	-	nC
Q_{GD}	gate-drain charge		-	17	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 A$; $V_{DS} = 20 V$; see Figure 15 ; see Figure 16	-	4.7	-	V
C_{iss}	input capacitance	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $f = 1 MHz$;	-	4491	-	pF
C_{oss}	output capacitance	$T_j = 25 ^\circ C$; see Figure 17	-	937	-	pF
C_{rss}	reverse transfer capacitance		-	464	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 V$; $R_L = 0.8 \Omega$; $V_{GS} = 10 V$;	-	28	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	29	-	ns
$t_{d(off)}$	turn-off delay time		-	52	-	ns
t_f	fall time		-	23	-	ns

Table 7. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _J = 25 °C; see Figure 18	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V	-	47	-	ns
Q _r	recovered charge	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C	-	61	-	nC

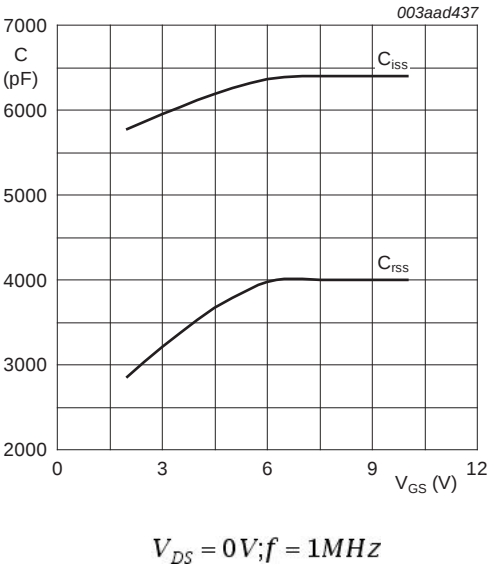


Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

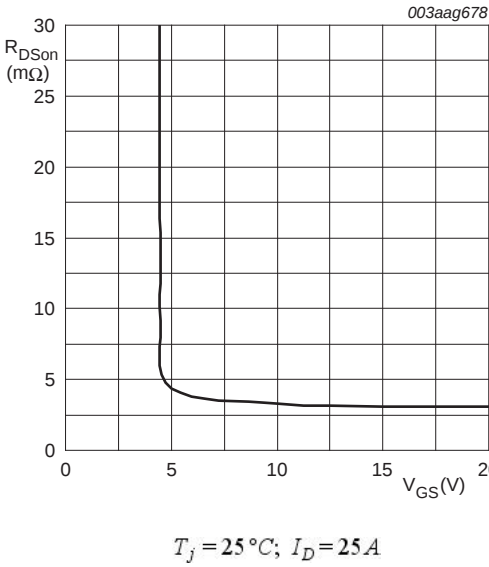


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

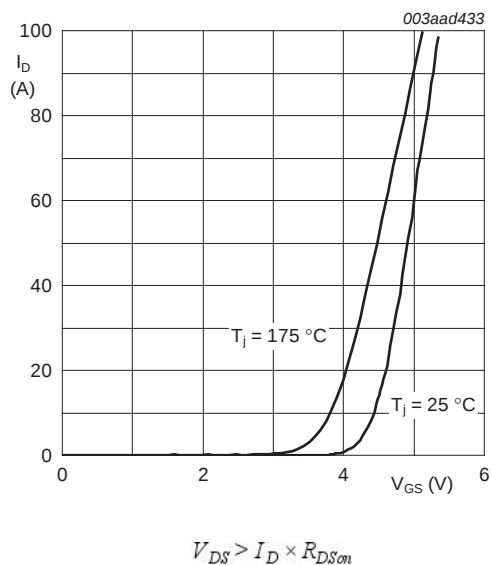


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

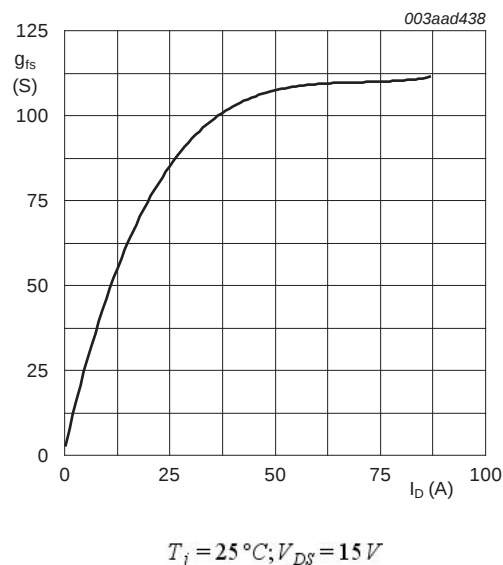


Fig 8. Forward transconductance as a function of drain current; typical values

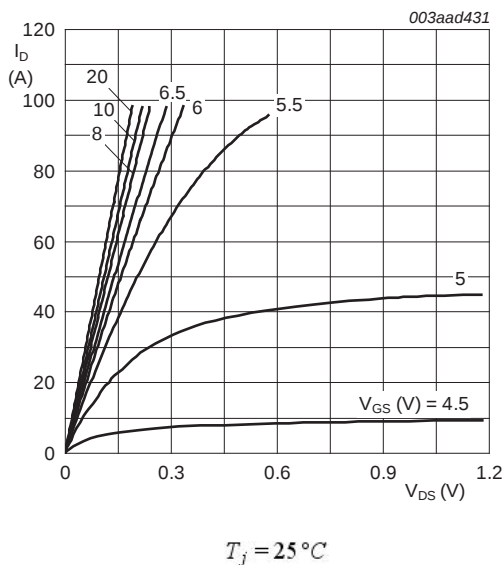


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

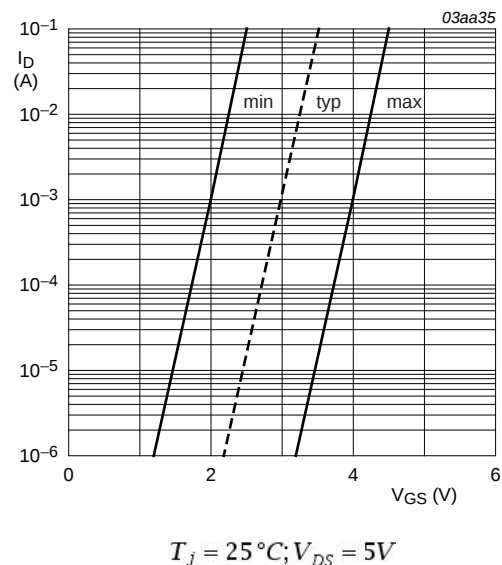
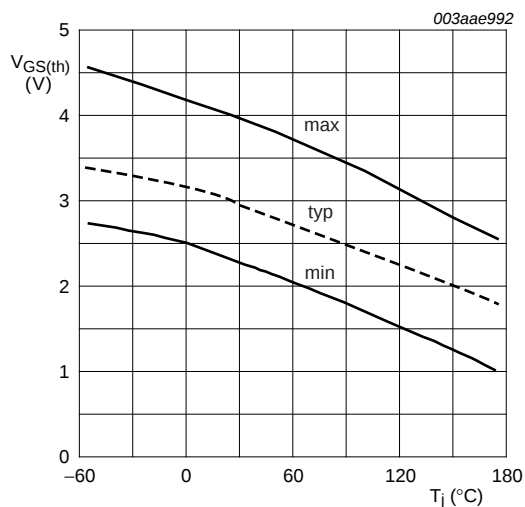
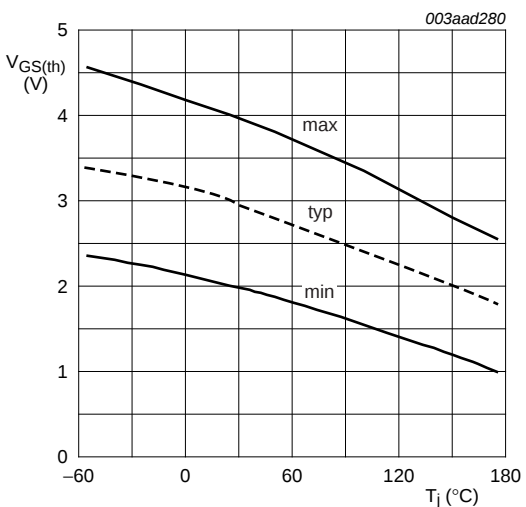


Fig 10. Sub-threshold drain current as a function of gate-source voltage



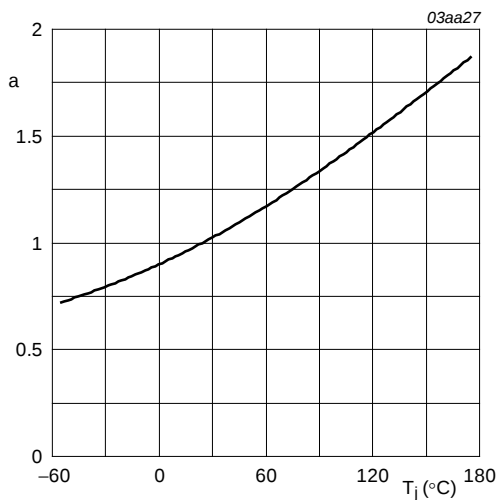
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



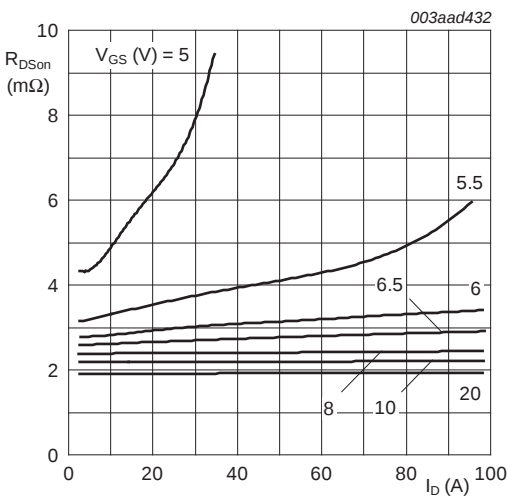
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}C}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}C$

Fig 14. Drain-source on-state resistance as a function of drain current; typical values

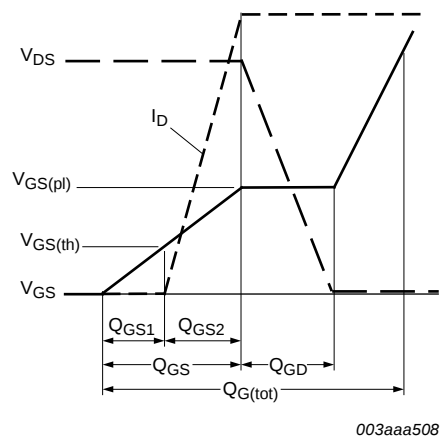


Fig 15. Gate charge waveform definitions

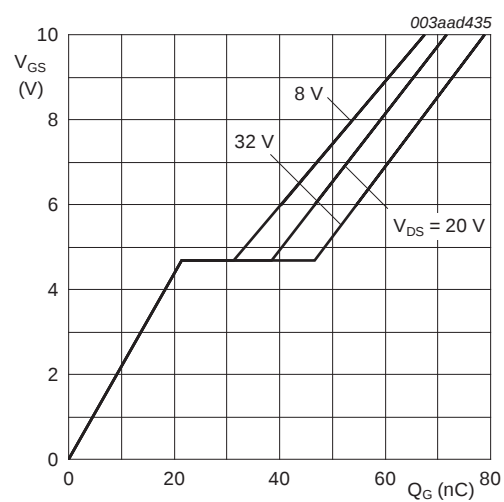


Fig 16. Gate-source voltage as a function of gate charge; typical values

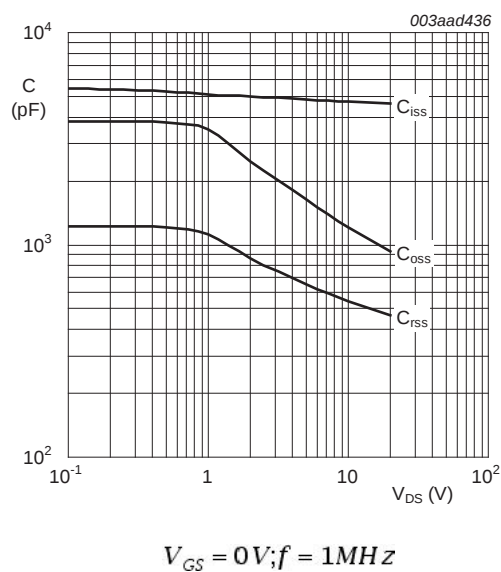


Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

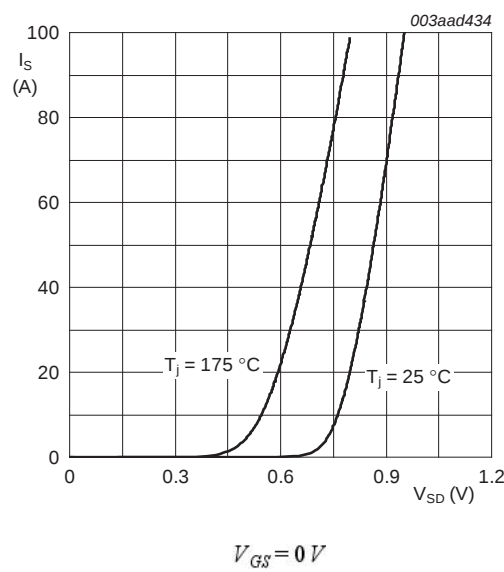


Fig 18. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

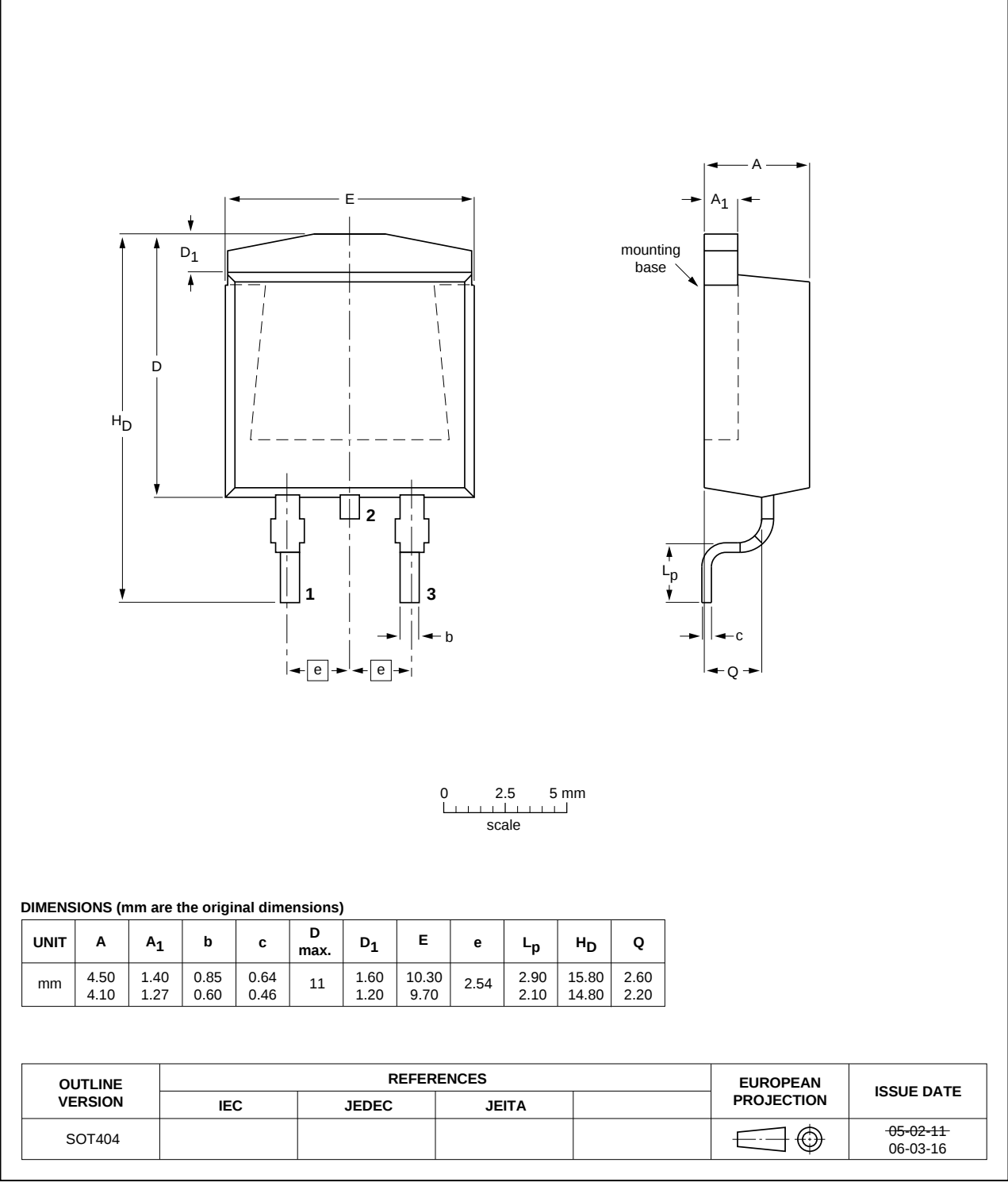


Fig 19. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R8-40BS v.1	20120320	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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