Features

- **192 macrocells in 12 Logic Array Blocks (LABs)**
- **Eight dedicated inputs, 64 bidirectional I/O pins**
- **Programmable interconnect array**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Parametric compatibility with the 5962-92062 SMD**
- **384 expander product terms**
- **Processing in accordance with MIL-PRF-38535 Class Q**
- **Available in the 84-pin Ceramic PGA package**

Functional Description

The TD7C341B is an Erasable Programmable Logic Device (EPLD) which uses CMOS EPROM cells to configure logic functions within the device. The architecture is 100% user-configurable, allowing the devices to accommodate independent logic functions in a variety of ways.

The 192 macrocells in the TD7C341B are divided into 12 Logic Array Blocks (LABs), 16 per LAB. With 32 per LAB, there are 384 expander product terms to be used and shared by the macrocells within each LAB.

Each LAB features being interconnected with a programmable interconnect array. The architecture allows signals to be routed throughout the chip.

The speed and density of the TD7C341B supports a wide range of applications, from replacement of large amounts of 5400-series TTL logic, to complex controllers and multifunction chips. With 37 times the functionality of 20-pin PLDs, the TD7C341B allows the replacement of over 75 TTL-logic devices reducing board space, part count, and increasing system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and eight are buried, while for LABs B, C, D, E, H, I, J, and K, four macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. This results in an enhanced capability of the macrocells without the accompanying increase in the number of product terms in each macrocell.

Selection Guide

	TD7C341B-30
Maximum Access Time	30 ns

Logic Block Diagram

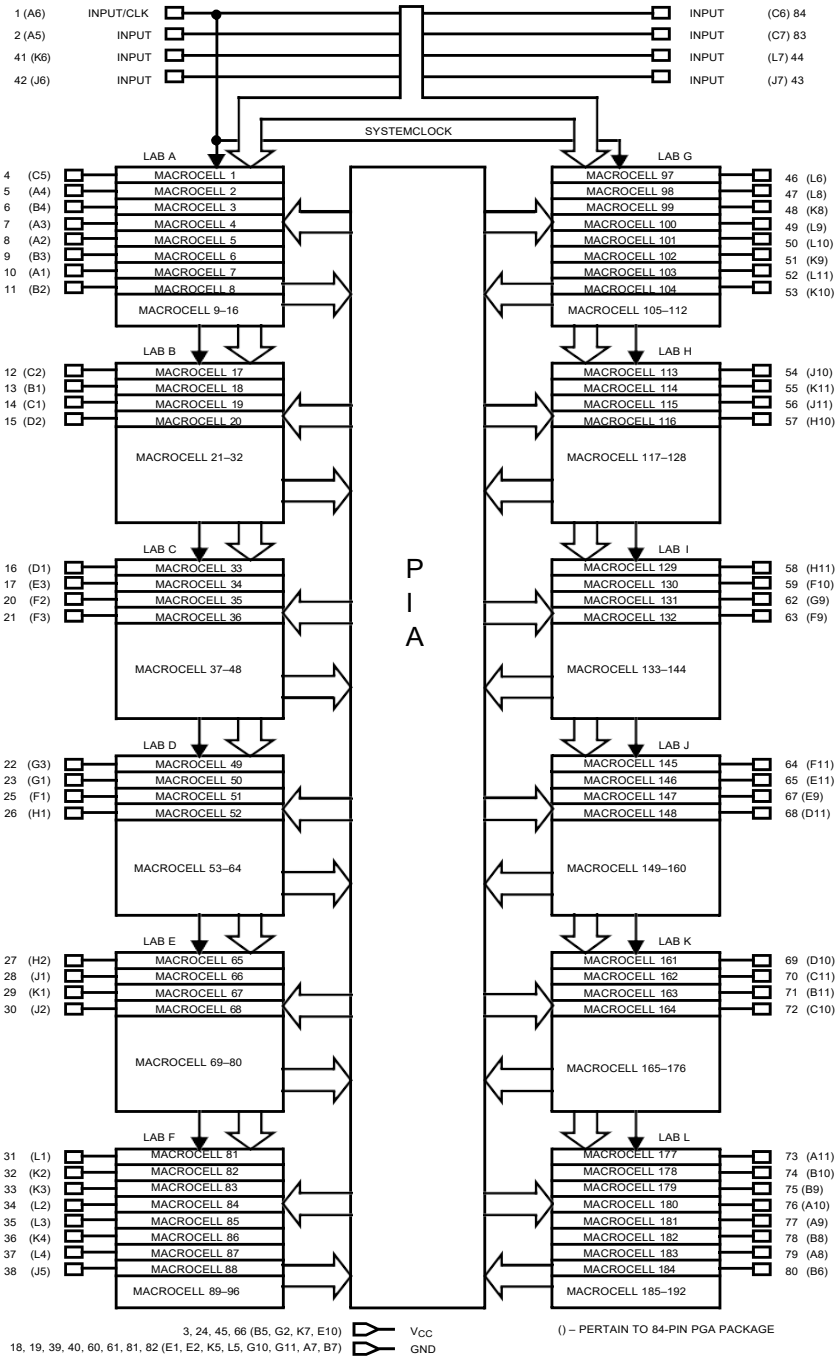


FIGURE 1. TD7C341B Logic Block Diagram

Pin Configurations

PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L	I/O	I/O	I/O	I/O	GND	I/O	INPUT	I/O	I/O	I/O	I/O
K	I/O	I/O	I/O	I/O	GND	INPUT	V_{CC}	I/O	I/O	I/O	I/O
J	I/O	I/O			I/O	INPUT	INPUT			I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	V_{CC}	I/O						I/O	GND	GND
F	I/O	I/O	I/O			7C341B			I/O	I/O	I/O
E	GND	GND	I/O						I/O	V_{CC}	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O	■		I/O	INPUT	INPUT			I/O	I/O
B	I/O	I/O	I/O	I/O	V_{CC}	I/O	GND	I/O	I/O	I/O	I/O
A	I/O	I/O	I/O	I/O	INPUT	INPUT/ CLK	GND	I/O	I/O	I/O	I/O

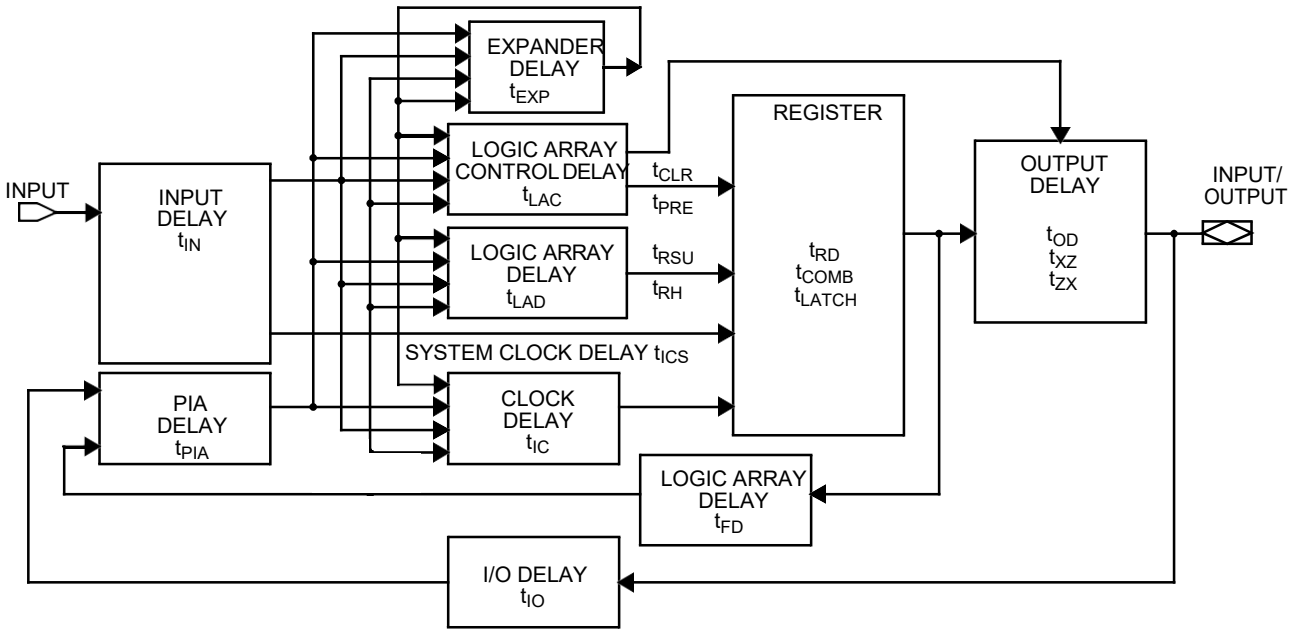
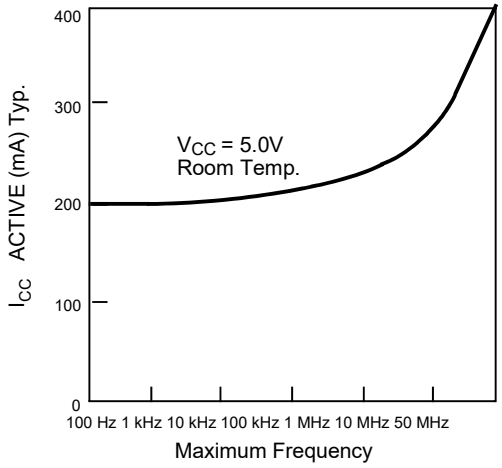


FIGURE 2. TD7C341B Internal Timing Model

Logic Array Blocks

There are 12 logic array blocks in the TD7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the TD7C341B provides eight dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.



Typical I_{CC} vs. f_{MAX}

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Design Recommendations

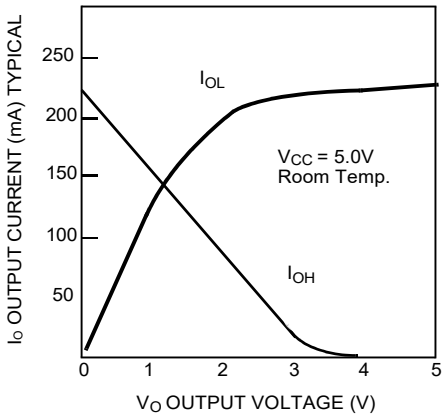
For proper operation, input and output pins must be constrained to the range GND ≤ (VIN or VOUT) ≤ VCC. Unused inputs must always be tied to an appropriate logic level (either VCC or GND). Each set of VCC and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 mF must be connected between VCC and GND. For the most effective decoupling, each VCC pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The TD7C341B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

The TD7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.



Output Drive Current

Ordering Information

Speed (ns)	Ordering Code	Package Letter Designator	Package Type	Operating Range Tcase
30	TD7C341B-30RMB	R	84-lead Windowed Ceramic Pin Grid Array	-55 °C to +125 °C

1. SCOPE

1.1 **Device type(s)**. The device type(s) identify the circuit function as follows:

Part Number	Generic number 1/	Circuit function	Propagation delay time
TD7C341B-30RMB	7C341B	192 Macrocell EPLD	30 ns

1.2 **Case outlines**. The case outline is designated in Figure 8 and as follows:

Package Letter Designator	Descriptive designator	Terminals
R	Ceramic Windowed Pin Grid Array	84-Lead 2/

1.2.1 **Lead finish**. The lead finish is as specified in MIL-PRF-38535 for device classes Q.

1.3 **Absolute maximum ratings**. 3/

Supply voltage range (V_{CC}) ---------- -2.0 V dc to +7.0 V dc
DC input voltage range ---------- -2.0 V dc to +7.0 V dc 4/
Maximum power dissipation ---------- 2.5 W 5/
Lead temperature (soldering, 10 seconds) ---------- +260 °C
Thermal resistance, junction-to-case (θ_{JC}):
Case outlines X, Y, and Z ---------- See MIL-STD-1835
Junction temperature (T_J) ---------- +175 °C
Storage temperature range ---------- 65 °C to +150 °C
Temperature under bias range ---------- 55 °C to +125 °C
Endurance ---------- 25 erase/write cycles (minimum)
Data retention ---------- 10 years (minimum)

1.4 **Recommended operating conditions**.

Supply voltage range (V_{CC}) ---------- +4.5 V dc to +5.5 V dc
Ground voltage (GND) ---------- 0 V dc
Input high voltage (V_{IH})---------- 2.2 V dc minimum
Input low voltage (V_{IL}) ---------- 0.8 V dc maximum
Case operating temperature range (T_C) ---------- -55 °C to +125 °C 6/
Input rise time (t_R) ---------- 100 ns maximum
Input fall time (t_F) ---------- 100 ns maximum

1/ As defined
2/ Lid shall be transparent to permit ultraviolet light erasure.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ Minimum dc input voltage is -0.3 V. During transitions, inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum dc voltage on output pins is V_{CC} + 0.3 V, which may overshoot to +7.0 V for periods less than 20 ns under no load conditions.

5/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).

6/ Case temperatures are instant on.

2. REQUIREMENTS

2.1 **Case outlines**. The case outlines shall be in accordance with the Package Diagram herein.

2.2 **Terminal connections**. The terminal connections shall be as specified on figure 3. 2.3

2.3 **Truth table**. The truth table shall be as specified on figure 4.

2.4 **Unprogrammed devices**. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 4. When required in screening or qualification conformance inspection groups A, B, C, or D, the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of gates shall be programmed or at least 25 percent of the total number of gates to any altered item drawing.

2.5 **Programmed devices**. The truth table for programmed devices shall be as specified by an attached altered item drawing.

2.6 **Electrical performance characteristics**. Unless otherwise specified herein, the electrical performance characteristics parameter limits are as specified in table I and shall apply over the full case operating temperature range.

2.7 **Electrical test requirements**. The electrical tests for each subgroup are defined in table I.

2.8 **Erasure of EPLDs**. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., ultraviolet intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

2.9 **Programmability of EPLDs**. The programming procedures shall be as specified by the device manufacturer of the die.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55\ °C \le T_C \le +125\ °C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1,2,3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V			0.45	
Input high voltage 1/ 2/	V_{IH}			2.2		
Input low voltage 1/ 2/	V_{IL}				0.8	
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND		-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND		-40	+40	
Output short circuit current 3/ 4/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V		-30	-90	mA
Power supply current 4/ 5/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND f = 1.0 MHz			480	
Power supply current (standby)	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} or GND			435	
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, T_A = +25 °C, f = 1 MHz, (see 4.4.1f)	4		10	pF
Output capacitance 2/	C_{OUT}	V_{CC} = 5.0 V, T_A = +25 °C, f = 1 MHz, (see 4.4.1f)	4		20	
Functional testing		See 4.4.1c	7, 8A, 8B			
Dedicated input to combinatorial output delay 7/	t_{PD1}	See figures 3 (circuit A) and 4 6/	9, 10, 11		30	ns
I/O input to combinatorial output delay 8/	t_{PD2}				45	
Dedicated input to combinatorial output delay with expander delay 9/	t_{PD3}				44	
I/O input to combinatorial output delay with expander delay 2/ 4/ 10/	t_{PD4}				59	
Input to output enable delay 4/ 7/	t_{EA}				30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued

Test	Symbol	Conditions -55 °C ≤ T_C ≤ +125 °C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input to output disable delay 4/ 7/	t_{ER}	See figures 3 (circuit B) and 4 6/	9,10,11		30	ns
Synchronous clock input to output delay	t_{CO1}	See figures 3 (circuit A) and 4 6/			35	
Dedicated input or feedback setup time to synchronous clock input 7/ 12/	t_{S1}	See figures 3 (circuit A) and 4 6/		20		
I/O input setup time to synchronous clock input 4/ 7/ 12/	t_{S2}			39		
Input hold time from synchronous clock input 7/	t_H			0		
Synchronous clock input high time 2/	t_{WH}			10		
Synchronous clock input low time 2/	t_{WL}			10		
Asynchronous clear width 2/ 4/ 7/	t_{RW}			30		
Asynchronous clear recovery time 2/ 4/ 7/	t_{RR}			30		
Asynchronous clear to registered output delay 2/ 7/	t_{RO}				30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued

Test	Symbol	Conditions $-55\ °C \le T_C \le +125\ °C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Asynchronous preset width 2/ 4/ 7/	t_{PW}	See figures 3 (circuit A) and 4 6/	9, 10, 11	30		ns
Asynchronous preset to registered output delay 2/ 7/	t_{PO}				30	
Synchronous clock to local feedback input 4/ 13/	t_{CF}				3	
External synchronous clock period ($1/f_{MAX3}$) 4/	t_P			20		
External feedback maximum frequency ($1/(t_{CO1} + t_{S1})$) 4/ 14/	f_{MAX1}			27.7		MHz
Internal local feedback maximum frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$) 4/ 15/	f_{MAX2}			43		
Data path maximum frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$ or ($1/(t_{WL} + t_{WH})$ 4/ 16/	f_{MAX3}			50		
Maximum register toggle frequency ($1/(t_WL + t_{WH})$) 4/ 17/	f_{MAX4}			50		
Output data stable time from synchronous clock input 4/ 18/	t_{OH}			3		ns
External asynchronous switching characteristics						
Dedicated asynchronous clock input to output delay 6/	t_{ACO1}	See figures 3 (circuit A) and 4 6/	9, 10, 11		30	ns
Asynchronous clock input to local feedback to combinatorial output 2/ 19/	t_{ACO2}				46	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued

Test	Symbol	Conditions -55 °C ≤ T_C ≤ +125 °C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Dedicated input or feedback setup time to asynchronous clock input 6/	t_{AS1}	See figures 3 (circuit A) and 4 6/	9, 10, 11	6		ns
I/O input setup time to asynchronous clock input 4/ 6/	t_{AS2}			27		
Input hold time from asynchronous clock input 6/	t_{AH}			8		
Asynchronous clock input high time 2/ 6/	t_{AWH}			14		
Asynchronous clock input low time 2/ 7/ 20/	t_{AWL}			11		
Asynchronous clock to local feedback input 4/ 21/	t_{ACF}				18	
External asynchronous clock period ($1/f_{MAXA4}$) 4/	t_{AP}			25		
External feedback maximum frequency in asynchronous mode $1/(t_{ACO1} + t_{AS1})$ 4/ 22/	f_{MAXA1}			27		MHz
Maximum internal asynchronous frequency 4/ 23/	f_{MAXA2}			40		
Data path frequency in asynchronous mode 4/ 24/	f_{MAXA3}			33.3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued

Test	Symbol	Conditions -55 °C ≤ T_C ≤ +125 °C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Maximum asynchronous register toggle frequency 1/(t_{AWH} + t_{AWL}) 4/ 25/	f_{MAXA4}	See figures 3 (circuit A) and 4 6/	9, 10, 11	40		MHz
Output data stable time from asynchronous clock input 4/ 26/	t_{AOH}			15		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.
4/ May not be tested but shall be guaranteed to the limits specified in table I.
5/ Measured with device programmed as a 16-bit counter in each LAB.
6/ AC tests are performed with input rise and fall times of 6 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output loads on figure 5.
7/ This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function. When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic. If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay for a dedicated input.
8/ This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9/ This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
10/ This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
11/ This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB.
12/ If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{AS2} for synchronous operation and t_{AS2} for asynchronous operation.
13/ This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous state machine configuration. This delay is for feedback within the same LAB.
14/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local, originating within the same LAB.
15/ This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/_{tCO1}$.
16/ This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
17/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
18/ This parameter indicates the minimum time after a maximum time after synchronous register clock input that the previous register output data is maintained on the output pin.

TABLE I. Electrical performance characteristics – Continued

19/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB.
20/ This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21/ This specification is a measure of the input delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronous clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin.
22/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + 1/t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24/ This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26/ This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

TD7C341B: CY7C341 Replacement System Design Considerations

The TD7C341B was developed as a process miniaturization of the Cypress CY7C341. The differences between die revisions may manifest with differences in performance. The Cypress CY7C341B device is 0.65-micron shrink of the original 0.8-micron CY7C341. This system design consideration guideline is provided so that system design engineers can evaluate their system in replacing the CY7C341 with the TD7C341B given a known performance difference.

During the qualification of the TD7C341B, it was observed that Vcc Power Up delay times between the two devices were different. Further testing indicated that the TD7C341B Vcc Power Up delay has a cold temperature dependence as shown in Table 1. In particular, the Vcc Power Up delay time increased from ~190 µs at room temperature to 115 ms at cold temperature (Tambient = –55 °C). Further testing indicated that the TD7C341B begins exhibiting this longer power up delay time at Tambient = ~ –35 °C. Testing of CY7C341 indicated that there was no cold temperature dependence on the Power Up delay time measurements.

Device Under Test	$T_{ambient}$ = 25 °C	$T_{ambient}$ = –55 °C
CY7C341	95 µs	96 µs
TD7C341B	190 µs	114.6 ms

TABLE 2: Vcc Power Up Delay Time Comparison

The system impact of this longer Vcc Power Up delay time requires system level knowledge as it relates to the Vcc power regulator and overall system power-up sequencing. The system designer should review the power up sequencing between the Vcc power supply enabling and TD7C341B data access. If there is sufficient time between the Vcc power supply enabling and the data access of the TD7C341B, this longer power up delay time will not cause a system disruption. Careful attention should also be given to:

1) Vcc supply regulator current limit and under-voltage control circuitry.
2) TD7C341B Vcc supply decoupling capacitor size and placement.
3) System supervisory circuit (if applicable) implementation of the Vcc supply regulator under-voltage.

For system designers looking to replace the obsolete CY7C341 with TD7C341B, a system review should be conducted to verify that this form-fit-function replacement will suffice in the application given the power up delay time vs temperature variation.

84-CPGA

Device types	All	Device types	All	Device types	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	I/O	C11	I/O	J2	I/O
A2	I/O	D1	I/O	J5	I/O
A3	I/O	D2	I/O	J6	INPUT
A4	I/O	D10	I/O	J7	INPUT
A5	INPUT	D11	I/O	J10	I/O
A6	INPUT / CLK	E1	GND	J11	I/O
A7	GND	E2	GND	K1	I/O
A8	I/O	E3	I/O	K2	I/O
A9	I/O	E9	I/O	K3	I/O
A10	I/O	E10	V_{CC}	K4	I/O
A11	I/O	E11	I/O	K5	GND
B1	I/O	F1	I/O	K6	INPUT
B2	I/O	F2	I/O	K7	V_{CC}
B3	I/O	F3	I/O	K8	I/O
B4	I/O	F9	I/O	K9	I/O
B5	V_{CC}	F10	I/O	K10	I/O
B6	I/O	F11	I/O	K11	I/O
B7	GND	G1	I/O	L1	I/O
B8	I/O	G2	V_{CC}	L2	/O
B9	I/O	G3	I/O	L3	I/O
B10	I/O	G9	I/O	L4	I/O
B11	I/O	G10	GND	L5	GND
C1	I/O	G11	GND	L6	I/O
C2	I/O	H1	I/O	L7	INPUT
C5	I/O	H2	I/O	L8	I/O
C6	INPUT	H10	I/O	L9	I/O
C7	INPUT	H11	I/O	L10	I/O
C10	I/O	J1	I/O	L11	I/O

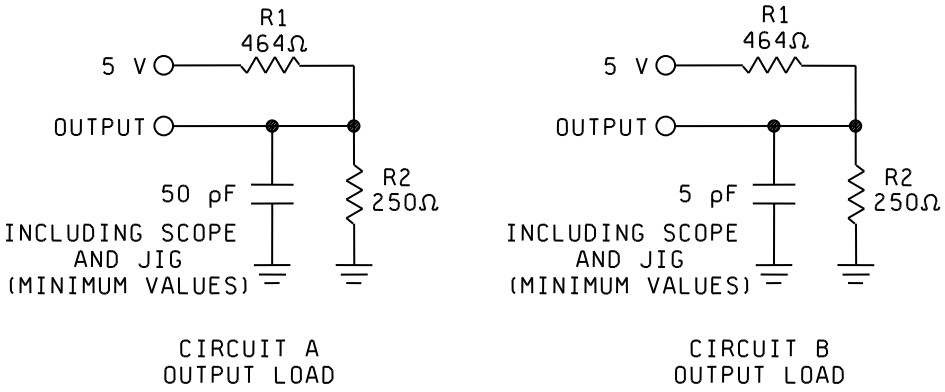
FIGURE 3. Terminal connections

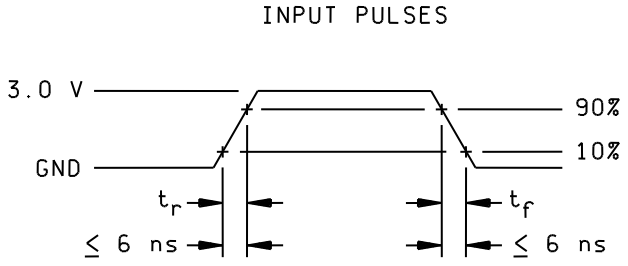
Truth Table		
Input pins		Output pins
I / CLK	I	I/O
X	X	Z

NOTES:
X = Don't care.

1. Z = High impedance.

2. **FIGURE 4. Truth table (unprogrammed)**





AC test conditions

Input pulse level	GND to 3.0 V
Input rise and fall levels	≤ 6 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Output load circuits and test conditions

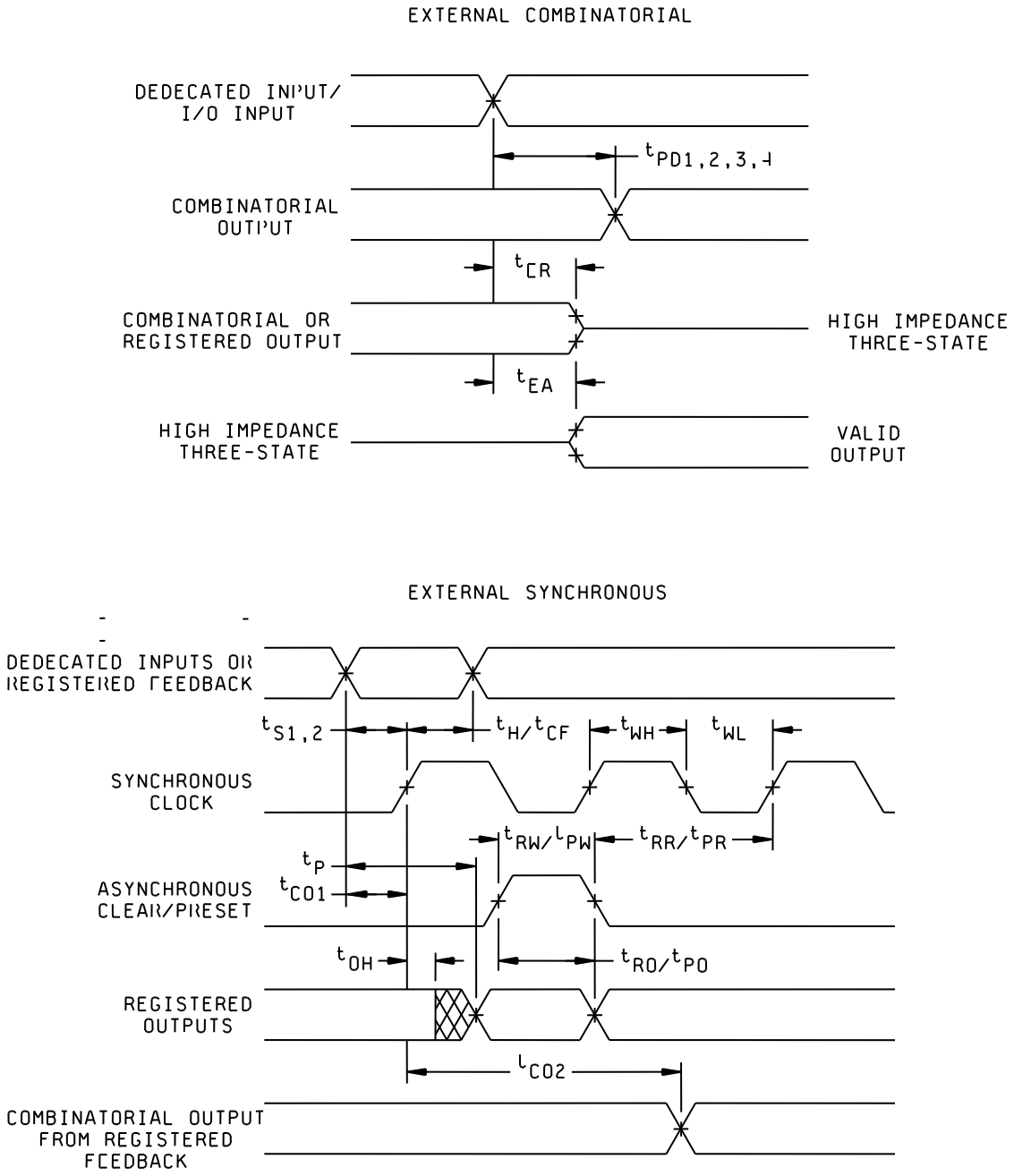


FIGURE 6. Switching waveforms

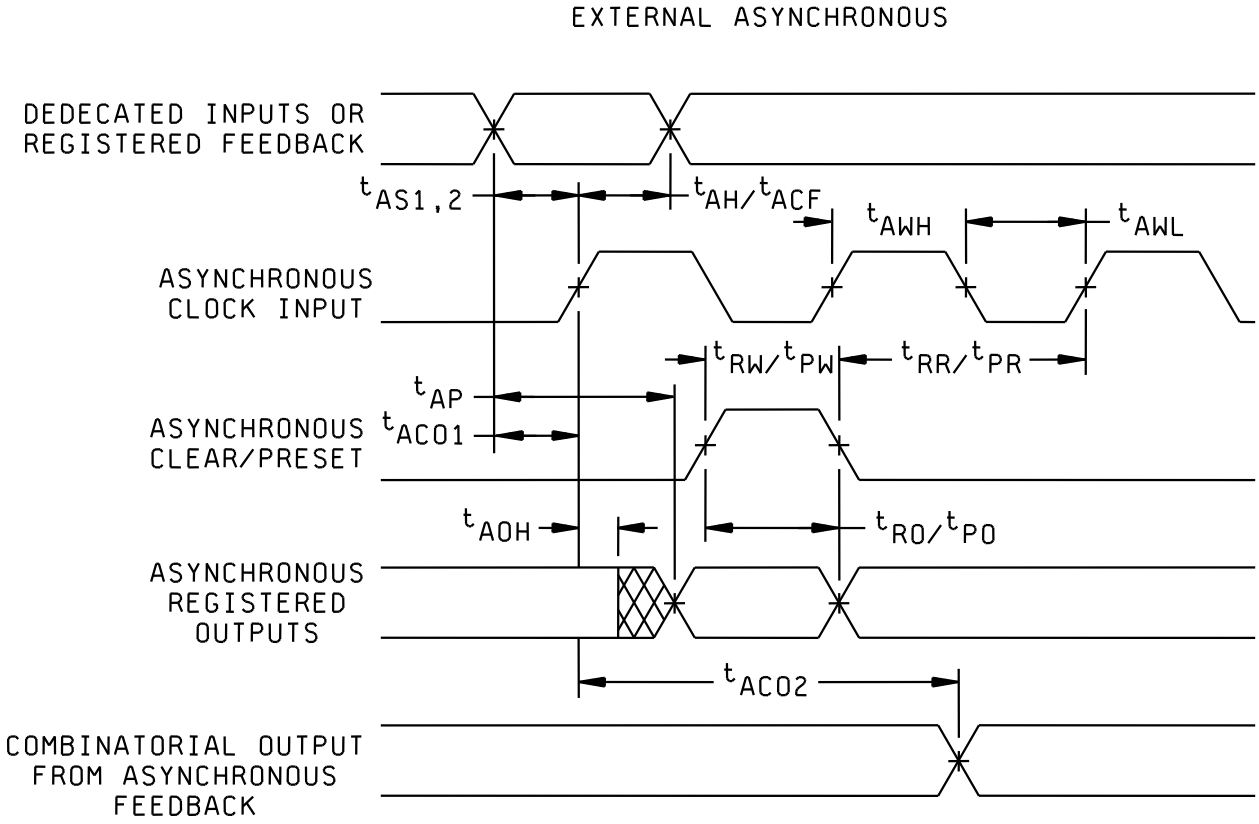


FIGURE 7. Switching waveforms - Continued

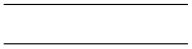
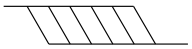
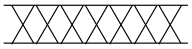
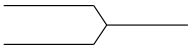
3.0 **Abbreviations, symbols, and definitions.** The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

Product Specification

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IX} ..... Input current.
I_{OZ} ..... Output current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

3.1 **Timing limits.** The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

3.2 **Waveforms.**

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

4.0 Package Diagram

84-Lead Ceramic Windowed Pin Grid Array

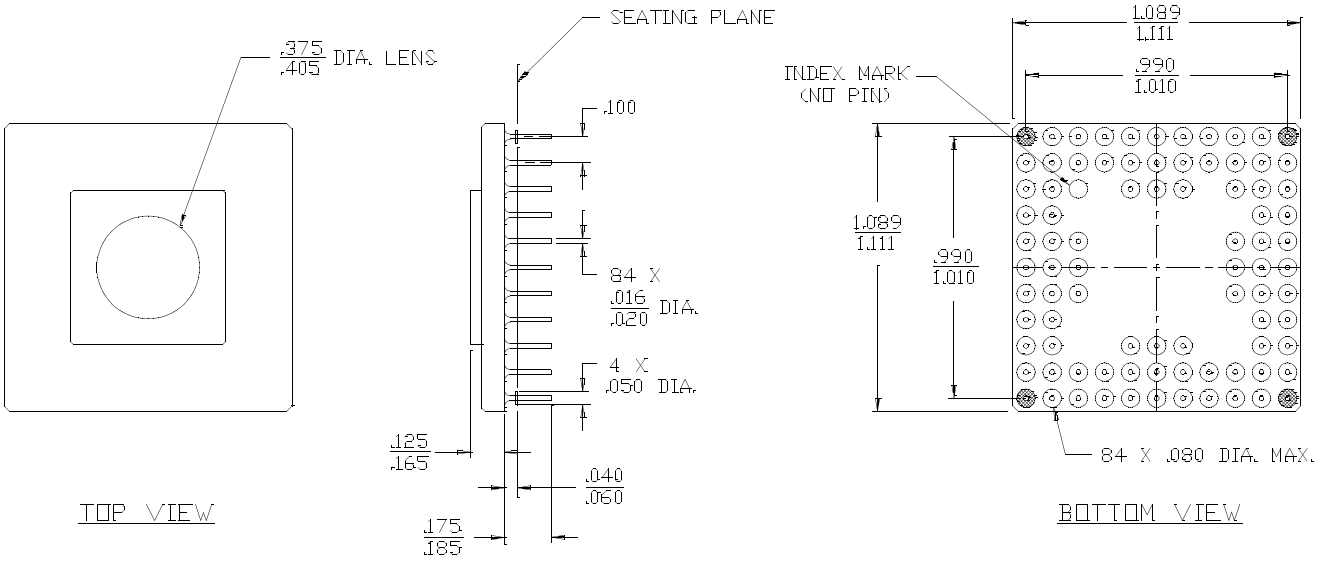


FIGURE 8. Package Diagram

Contact Information:

Teledyne e2v HiRel Electronics at: www.tdehirel.com Contact us via email: tdemarketing@teledyne.com

Preliminary Specification: The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Advanced Information: The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.
Product Specification - The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel will notify customers of the intended changes by issuing a CNF (Customer Notification Form).