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June 2014

FDB024N08BL7

N-Channel PowerTrench[®] MOSFET

80 V, 229 A, 2.4 mΩ

Features

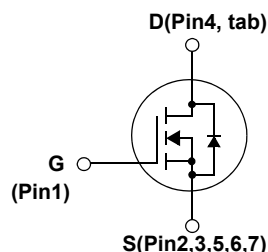
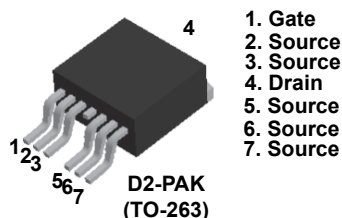
- $R_{DS(on)} = 1.7 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Low FOM $R_{DS(on)} \cdot Q_G$
- Low Reverse Recovery Charge, $Q_{rr} = 112 \text{ nC}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- RoHS Compliant
- Qualified according to JEDEC Standards JESD22-A113F and IPC/JEDEC J-STD-020D.1

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench[®] process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDB024N08BL7	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	A
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		- Derate Above 25°C	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

Thermal Characteristics

Symbol	Parameter	FDB024N08BL7	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.61	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB024N08BL7	FDB024N08B	D2PAK-7L	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.05	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	1	μA
		$V_{DS} = 64\ \text{V}$, $T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 100\ \text{A}$	-	1.7	2.4	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 100\ \text{A}$	-	227	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	-	10170	13530	pF
C_{oss}	Output Capacitance		-	1670	2220	pF
C_{rss}	Reverse Transfer Capacitance		-	35	-	pF
$C_{oss(er)}$	Engry Related Output Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	3025	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 100\ \text{A}$	-	137	178	nC
Q_{gs}	Gate to Source Gate Charge		-	56	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	25	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	28	-	nC
ESR	Equivalent Series Resistance (G-S)	$f = 1\ \text{MHz}$	-	2.4	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\ \text{V}$, $I_D = 100\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_G = 4.7\ \Omega$	-	47	104	ns
t_r	Turn-On Rise Time		-	66	142	ns
$t_{d(off)}$	Turn-Off Delay Time		-	87	184	ns
t_f	Turn-Off Fall Time		-	41	92	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	229*	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	916	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 100 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 40 V, I _{SD} = 100 A,	-	80	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	112	-	nC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $L = 3\ \text{mH}$, $I_{AS} = 24.72\ \text{A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

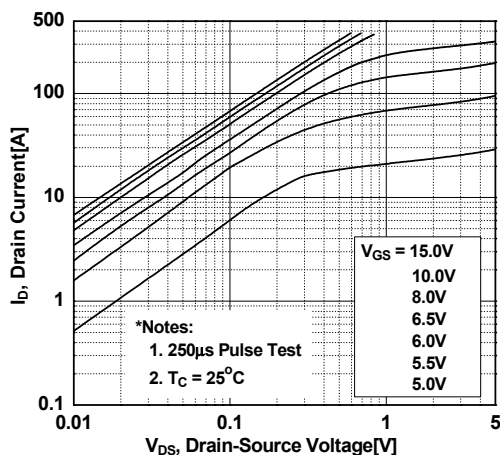


Figure 2. Transfer Characteristics

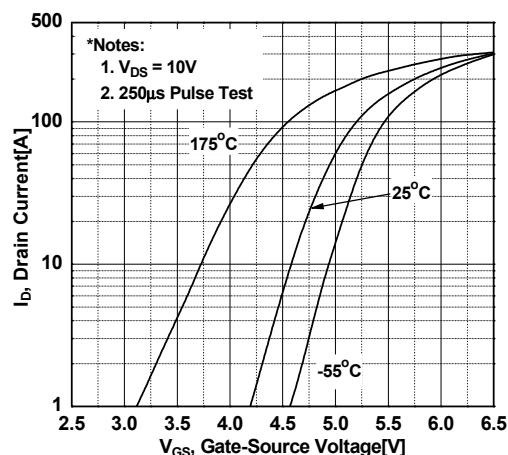


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

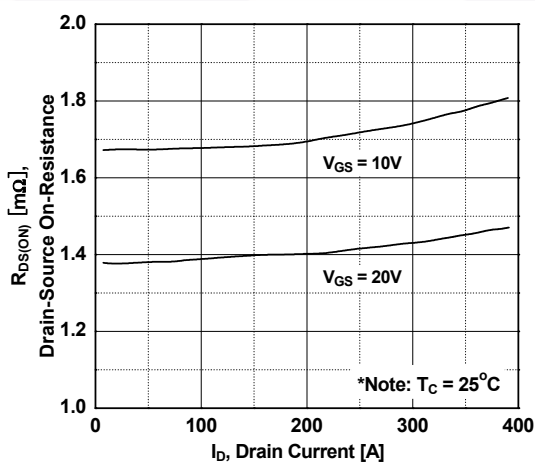


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

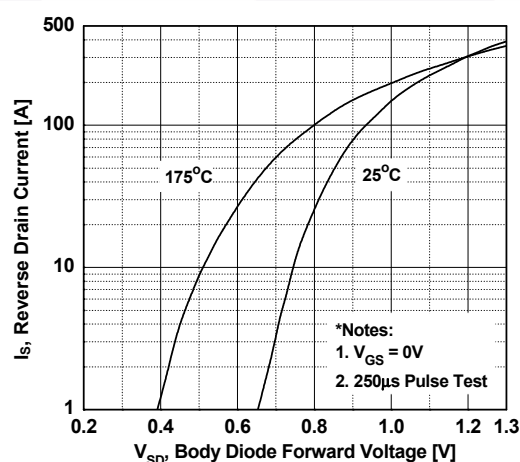


Figure 5. Capacitance Characteristics

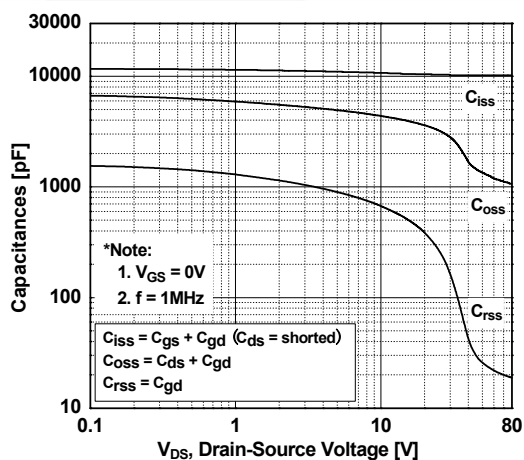
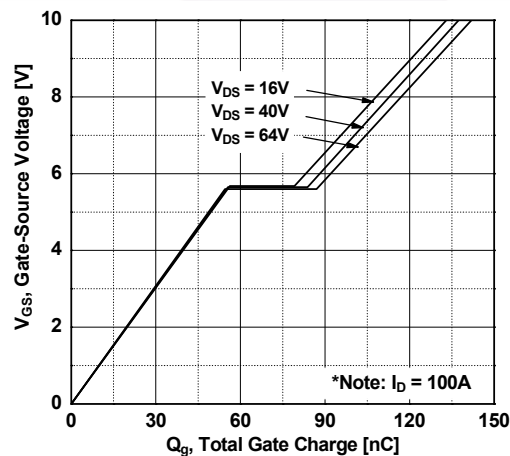


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

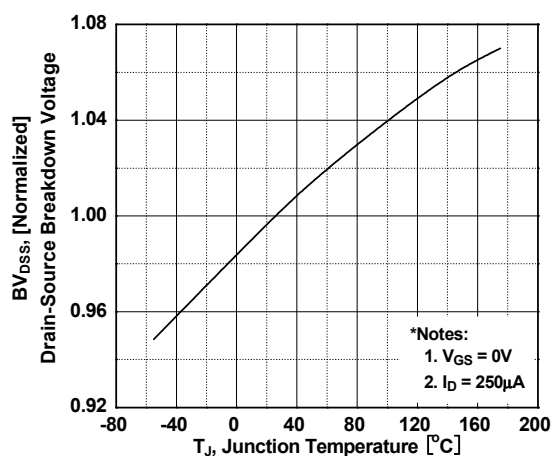


Figure 8. On-Resistance Variation vs. Temperature

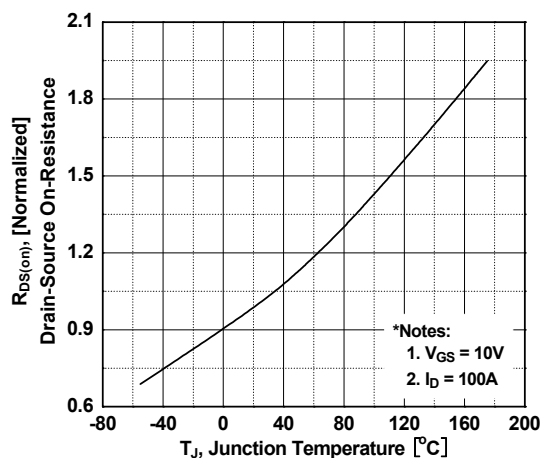


Figure 9. Maximum Safe Operating Area

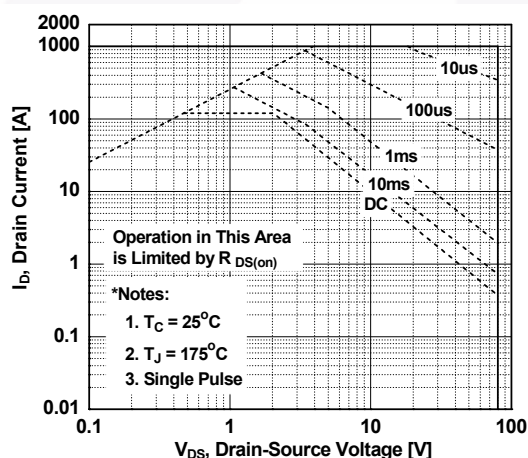


Figure 10. Maximum Drain Current vs. Case Temperature

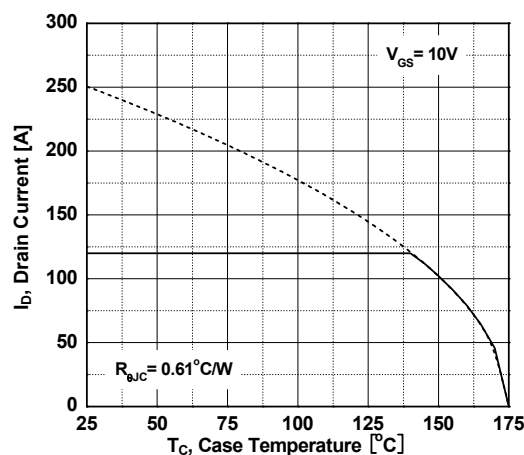


Figure 11. E_oss vs. Drain to Source Voltage

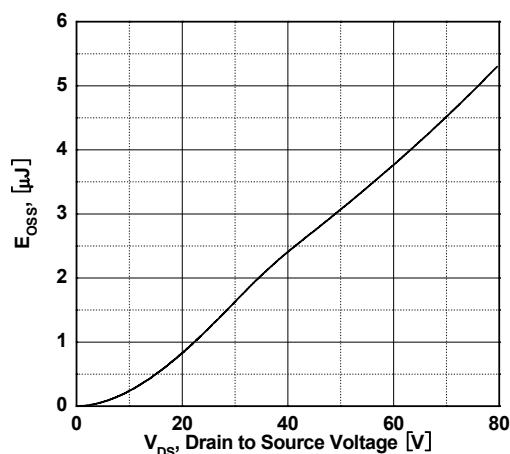
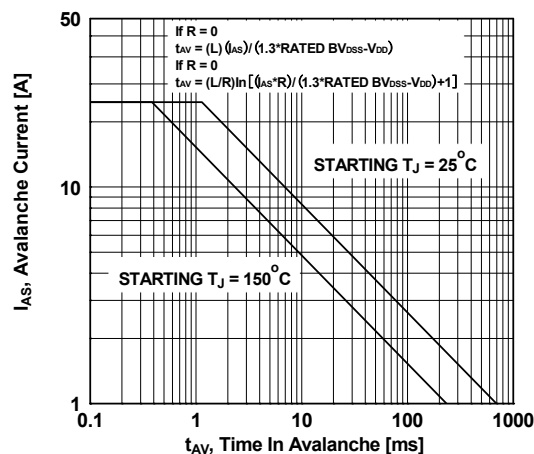


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

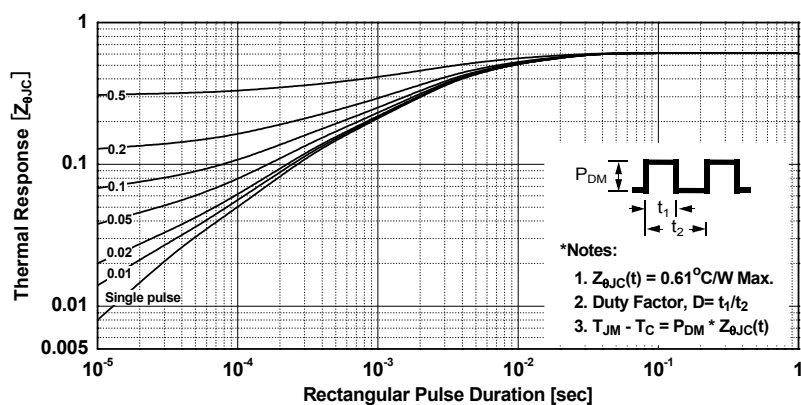


Figure 13. Gate Charge Test Circuit & Waveform

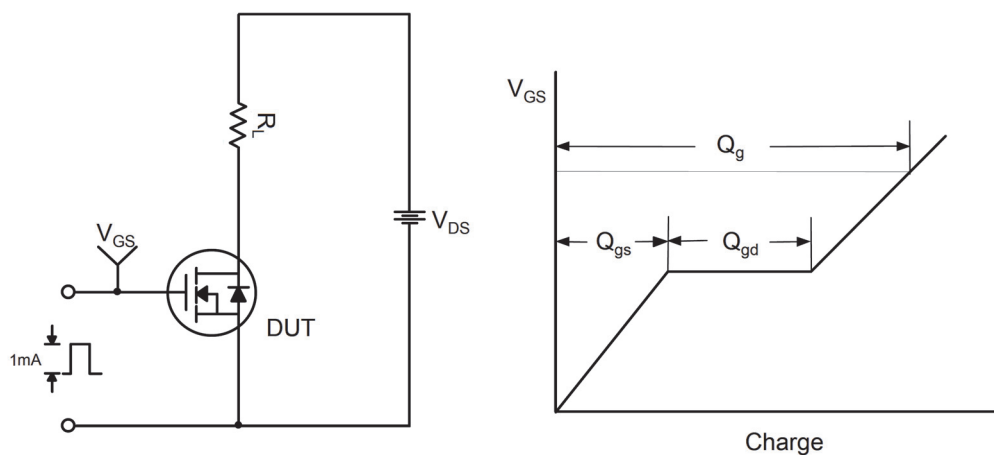


Figure 14. Resistive Switching Test Circuit & Waveforms

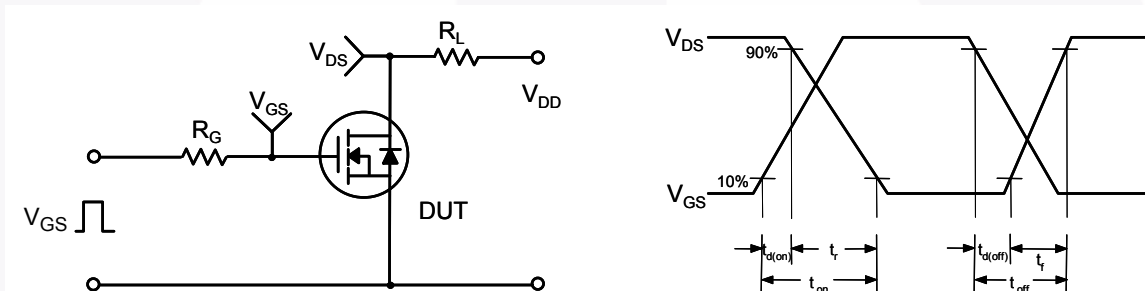


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

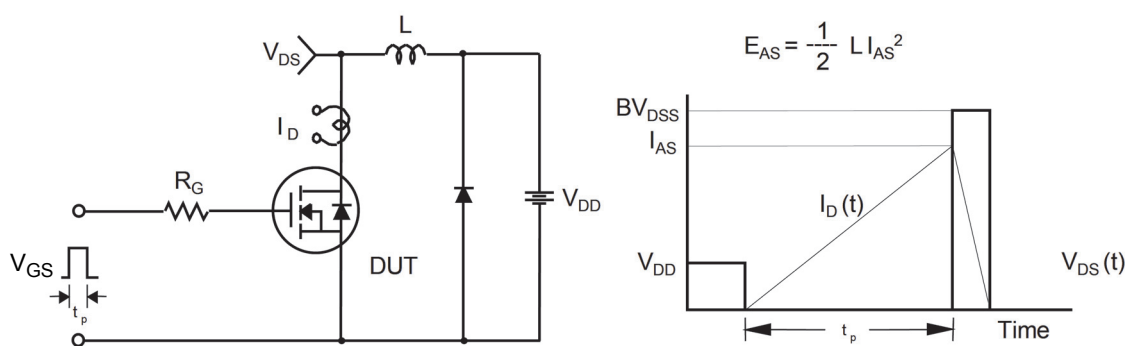
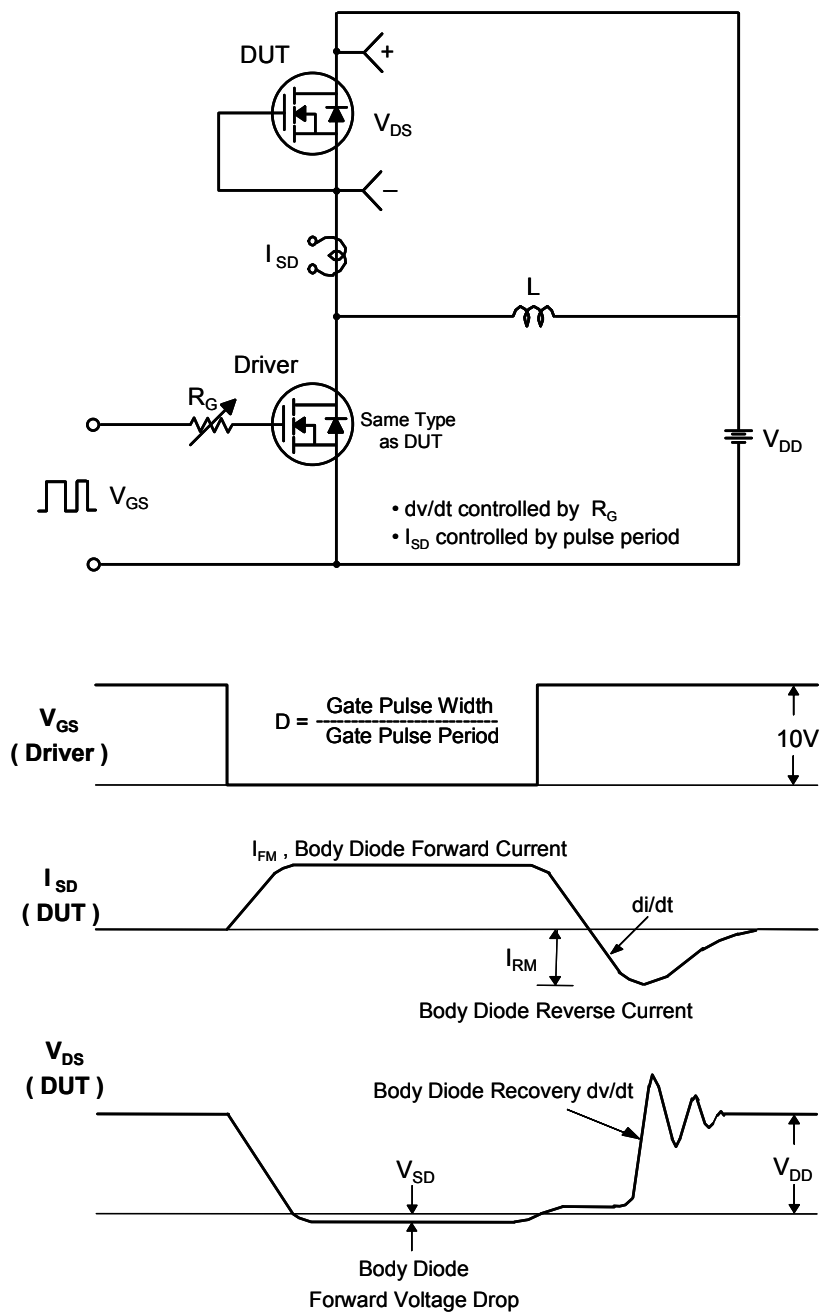
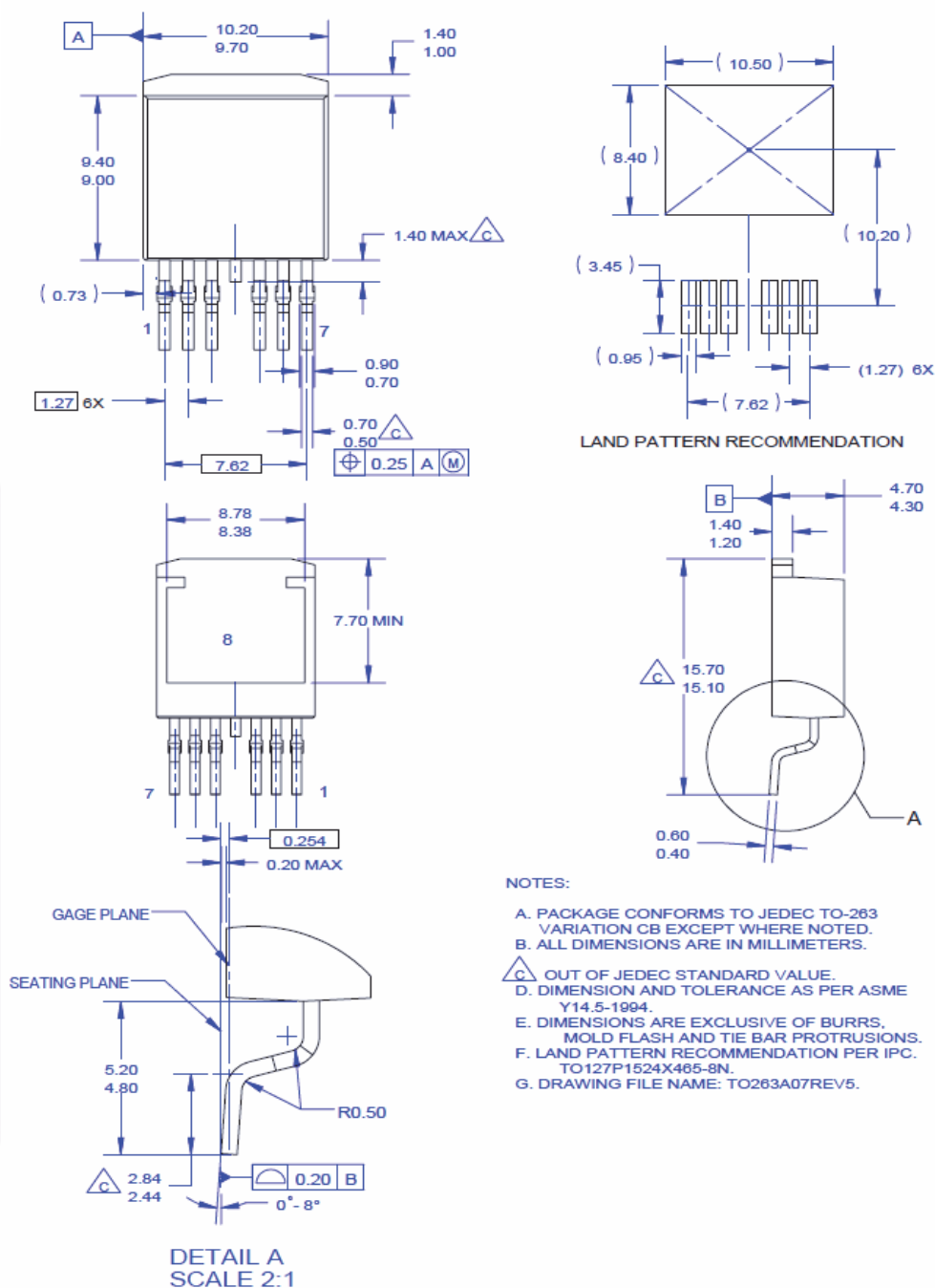


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

Figure 17. TO263 (D²PAK), Molded, 7-Lead, Surface Mount


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