Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology" and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

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FEDL62Q1600-05
Issue Date: May 31, 2018

ML62Q1600 Group

16-bit micro controller

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GENERAL DESCRIPTION

ML62Q1600 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC operator, DMA controller, clock generator, simplified RTC, timer, UART, synchronous serial port, I^2C bus interface unit, buzzer, Voltage Level Supervisor(VSL), successive approximation type A/D converter, D/A converter , analog comparator, LCD driver, safety function and etc.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.
The ML62Q1600 Group has five packages (48pin - 64pin) and five kinds of memory sizes(32Kbyte - 64Kbyte).

Table 1 ML62Q1600 Group Product List

Program memory	Data memory (RAM)	Data Flash	48pin TQFP48	52pin TQFP52	64pin QFP64 TQFP64
64Kbyte	4Kbyte	2Kbyte	ML62Q1602	ML62Q1612	ML62Q1622
48Kbyte	4Kbyte	2Kbyte	ML62Q1601	ML62Q1611	ML62Q1621
32Kbyte	4Kbyte	2Kbyte	ML62Q1600	ML62Q1610	ML62Q1620

FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-chip debug function built-in (supported by LAPIS on-chip debug emulator EASE1000)
  - ISP (In-System Programming) function built-in
  - Minimum instruction execution time
    30.5 µs (at 32.768 KHz system clock)
    62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

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- Operating voltage and temperature
  - Operating voltage: VDD = 1.6 to 5.5 V
  - Operating temperature: -40 to +105 °C

- Internal memory
  - Prrogram Flash memory area
    Rewrite count: 100 cycles
    Rewrite unit: 32bit(4byte)
    Erase unit: 16Kbyte/1Kbyte
    Erase/Rewrite temperature: 0°C to +40°C

  - Data Flash memory area
    Rewrite count 10,000 cycles
    Rewrite unit: 8bit(1byte)
    Erase unit: 2Kbyte/128byte
    Erase/Rewrite temperature: -40°C to +85°C
    Back Ground Operation(CPU can work while erasing and rewriting)

  - Data RAM area
    Rewrite unit: 8bit/16bit(1byte/2byte)
    Parity check function (Parity error reset is generatable)

- Clock
  - Low-speed clock
    Internal low-speed RC oscillation: Approx.32.768 KHz
    External low-speed crystal oscillation: 32.768 KHz crystal resonator is connectable
    4 modes is available for the crystal oscillatiion
    - Tough mode: Largest oscillation allowance to make highest resistance against leakage between the pins
    - Standard mode: Standard oscillation allowance and current consumption
    - Low power current mode: Smaller oscillation allowance than standard mode to make lower current consumption
  - High-speed clock
    PLL oscillation: 32MHz/24MHz/16MHz is selectable by code option
  - WDT(Watch Dog Timer) clock
    Internal low-speed RC oscillation: Aprox. 1kHz
    The WDT independent clock or the divided clock of internal low-speed 32.768kHz RC oscillation clock is selectable by the code option.

- Reset
  - RESET_N pin reset
  - Reset by power-on detection
  - Reset by the 2nd watchdog timer (WDT) overflow
  - Reset by WDT counter clear during the clear invalid period
  - Reset by RAM parity error
  - Reset by unused ROM access
  - Reset by voltage level detection 0 (VLS0)
  - The software reset by BRK instruction (reset CPU only)

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- Power management
  - HALT mode: CPU stops executing instruction, clock oscillations and peripheral circuits remain previous states
  - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits working with low-speed clock remain previous states
  - STOP mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
  - STOP-D mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal regulator's output voltage (V_{DDL}) goes down to reduce the current consumption.
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of the oscillation clock)
  - Block Control Function: Powers down the circuits of unused function blocks (reset the block or stop supplying the clock)

- Interrupt controller
  - Non-maskable interrupt source: 1 (Internal sources: WDT)
  - Maskable interrupt sources: max.37 (Internal sources: max.29, External sources: 8)
  - Four step interrupt levels

- Watchdog timer(WDT)
  - Operation clock: 1kHz WDT independent clock or 32.768kHz RC oscillation clock, selectable by code option
  - Overflow period: 8 types selectable (8ms, 16ms, 32ms, 64ms, 125ms, 500ms, 2000ms and 8000ms @32.768kHz)
  - WDT counter clear enable period : 50%, 75% or 100% of overflow period
    When 100% of overflow period is selected,
    The first overflow generates an interrupt, and the second overflow generates a reset.
    When 50% or 70% of overflow period is selected,
    Clearing the WDT counter out of the enable period generates the WDT invalid clear reset.
  - WDT operation : Enable or disable is selectable by code option
  - Readable WDT counter (WDT counter monitor function)

- DMA(Direct Memory Access) controller
  - Channel : 2ch
  - Operation mode : Wait mode only (cannot be used in No wait mode)
  - Transfer unit: 8bit/16bit
  - Max. transfer count: 1024 time
  - Transfer type: 2 cycle transfer
  - Transfer mode: Single transfer mode
    Fixed address, address increments and address decrements
  - Transfer target: SFR/RAM ←→ SFR/RAM (Transfer from/to Flash is not supported)
  - Transfer request: Serial unit interrupt, A/D interrupt and 16bit timer interrupt

- Time base counter
  - Devide the Low-speed clock(LSCLK) and generate 32.768kHz~1Hz internal pulse signals
  - Priodical interrupt × 3 selectable from 8 frequencies (128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz)
  - The time base clock output (1Hz or 2Hz) from general purpose ports (TBCOUT1).

- Simplified RTC
  - Channel: 1 ch
  - Count by one second from "00 min. 00 sec" to "59 min. 59 sec"
  - One interrupt occurrence is selectable from four periodical interrupt requests (0.5sec, 1sec, 30sec or 60sec)
  - Protect function for incorrect writing the minutes and second.

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- Functional timer(FTM)
  - Channel: 6ch
  - Timer one shot mode and repeat mode, Caputure mode, PWM mode1 and PWM mode 2(complementary output)
  - Same start/stop is avaible with different channels
    (This function is not avaible with 16bit Genral Timer)
  - Event trigger (external interrupts, analog comprator interrupts, 16bit genral timer interrupts and Functional timer interrupts)
  - Delay counter (for generating dead time)
  - Available to specify devision ratio of counter clock channel by channel

- 16bit General timers
  - Channel: 6ch
  - 8 bits timer mode and 16-bit timer mode (1ch 16-bit timer is configurable as 2ch 8-bit timer)
  - Same start/stop is avaible with different channels
    (This function is not avaible with Functional Timer)
  - Timer output (toggled by overflow)
  - Available to specify devision ratio of counter clock channel by channel

- Serial communication unit
  - Channel: Max. 2ch
  - Synchronous Serial Port or UART is seletable in each channel

  < Synchronous Serial Port >
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

  < UART >
  - Full-duplex communication x 2 ch(One Full-duplexUART is configurable as two half-duplex UARTs)
  - 5~8 bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - LSB first/MSB first selectable
  - Internal baud rate generator (1bps ~ 2Mbps)

- I^2C bus interface unit (Master/Slave)
  - Channel: 1ch
  - Master or Slave mode is selectable

  < Master function >
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock syncronization)
  - 7bit address format (10bit address format is supported)

  < Slave function >
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock syncronization)
  - 7bit address format (10bit address format is supported)

- I^2C bus interface (Master only)
  - Channel: 2ch
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock syncronization)
  - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
  - I/O port: Max. 53 (Including one pin for on-chip debug and pins for other shared functions)
  - Input port: Max. 2(Including a shared function)
  - External interrput function × 8
  - LED driver port : Max. 52 (Including LCD drive pins)
  - Carrier frequency output function (used for IR communication)

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- Successive approximation type A/D converter
  - Channel: Max.8ch (20pinTSSOP, 24pinWQFN and 32pinTQFP)
  - Resolution: 10bit
  - Conversion time: Selectable 2.25μs (min) /channel (When the conversion clock is 8MHz)
  - Referece voltages are selectable
    (VDD pin input voltage / Internal reference voltage(Approx. 1.55V) / Extenal reference voltage (V_{REF} pin)
  - Scan function (repeat conversion)
  - One result register for each channel
  - Interrupt by threshold of conversion result
  - Temprature sensor for low-speed RC oscillation adjustment

- Voltage level superviosr (VSL)
  - Accuracy: ±4°C
  - Threshold voltage: 12 values selectable (1.85V ~ 4.00V)
  - Voltage level detection reset (VLS reset)
  - Voltage level detection interrupt (VLS0 interrupt)

- Analog comparator
  - Channel: 2ch
  - Interrupts allow edge selection and sampling selection
  - An external or an internal reference voltage is selectable

- D/A converter
  - Channel: 1ch
  - Resolution: 8bit
  - Output impedance: 6k ohm(Typ.)
  - R-2R radder method

- Buzzer
  - 4 buzzer mode (Repeat sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
  - 8frequencies (4.096kHz to 293Hz)
  - 15 step duty (1/16 to 15/16)
  - Slectable the logic of buzzer output pin (Possitive or Negative logic)

- CRC(Cycle Redundancy Check) operation function
  - Generation eqution: $X^{16}+X^{12}+X^{5}+1$
  - LSB first
  - Automatic CRC mode: Automatic CRC calculation with data of program memory in HALT mode

- LCD driver
  - Max. 280 dots (35seg x 8 com)
    ML62Q1600/ML62Q1601/ML62Q1602[*1]: 24seg×8com (com Max), 29seg×3com (seg Max.)
    ML62Q1610/ML62Q1611/ML62Q1612[*1]: 27seg×8com (com Max.), 32seg×3com (seg Max.)
    ML62Q1620/ML62Q1621/ML62Q1622[*1]: 35seg×8com (com Max.), 40seg×3com (seg Max.)
    [*1] : Five pins are shared for common or segment, selectable by setting a SFR
  - 1/3 bias (built-in bias generation circuit)
  - Frame frequency (Approx. 32Hz, 38Hz, 64Hz, 75Hz, 128Hz and 150Hz)
  - Four bias generation modes (Internal voltage boost, Internal capacitive voltage divde, External supply voltage/capacitive divde, and External suppy voltages)
  - Contrast adjustment (32 steps) is available in the Internal voltage boost mode.

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- Safety Function
  - RAM/SFR guard
  - Automatic CRC calculation with data of program memory
  - RAM parity error detection
  - ROM unused area access reset
  - Clock mutual check
  - WDT counter check
  - Successive approximation type A/D converter test
  - UART test
  - Synchronous serial test
  - I^2C test
  - GPIO test

- Shipping pacakge

  - 48-pin plastic TQFP
    ML62Q1600/1601/1602-xxxTB (Blank part: ML62Q1600/1601/1602-NNNTB)

  - 52-pin plastic TQFP
    ML62Q1610/1611/1612-xxxTB (Blank part: ML62Q1610/1611/1612-NNNTB)

  - 64-pin plastic TQFP
    ML62Q1620/1621/1622-xxxTB (Blank part: ML62Q1620/1621/1622-NNNTB)

  - 64-pin plastic QFP
    ML62Q1620/1621/1622-xxxGA (Blank part: ML62Q1620/1621/1622-NNNGA)

    xxx: ROM code number

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ML62Q1600 Group how to read the part number

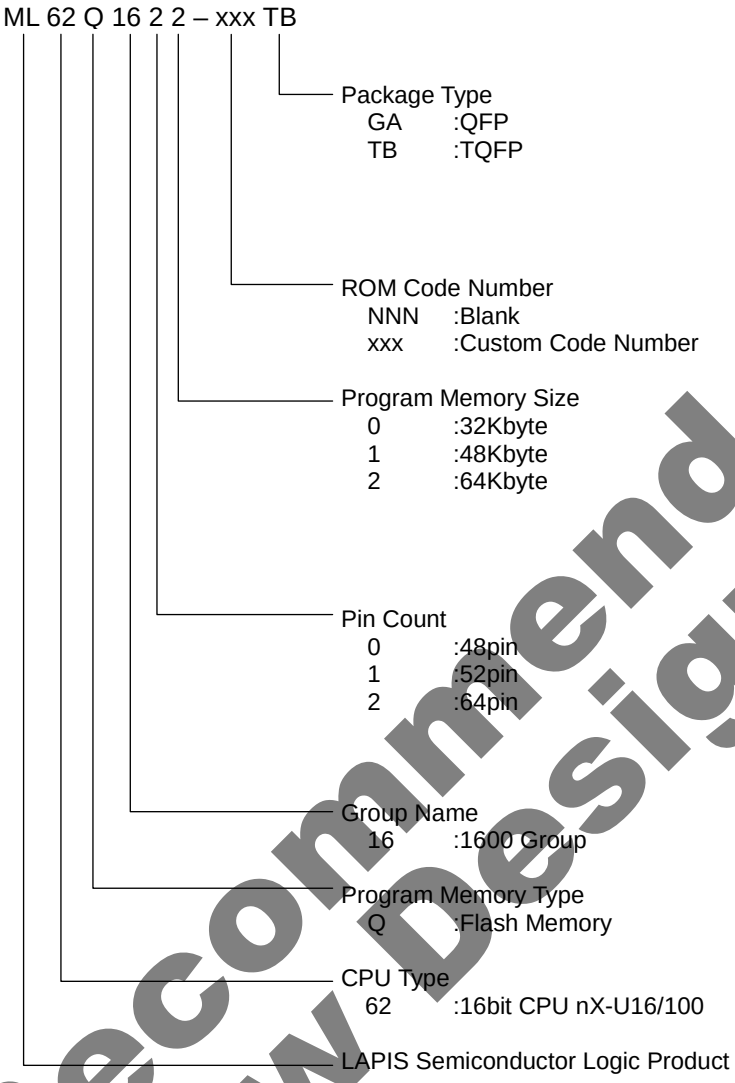


Figure 1 ML62Q1600 Group Part Number

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ML62Q1600 Group Main Function List

Table 2 ML62Q1600 Group Main Function List

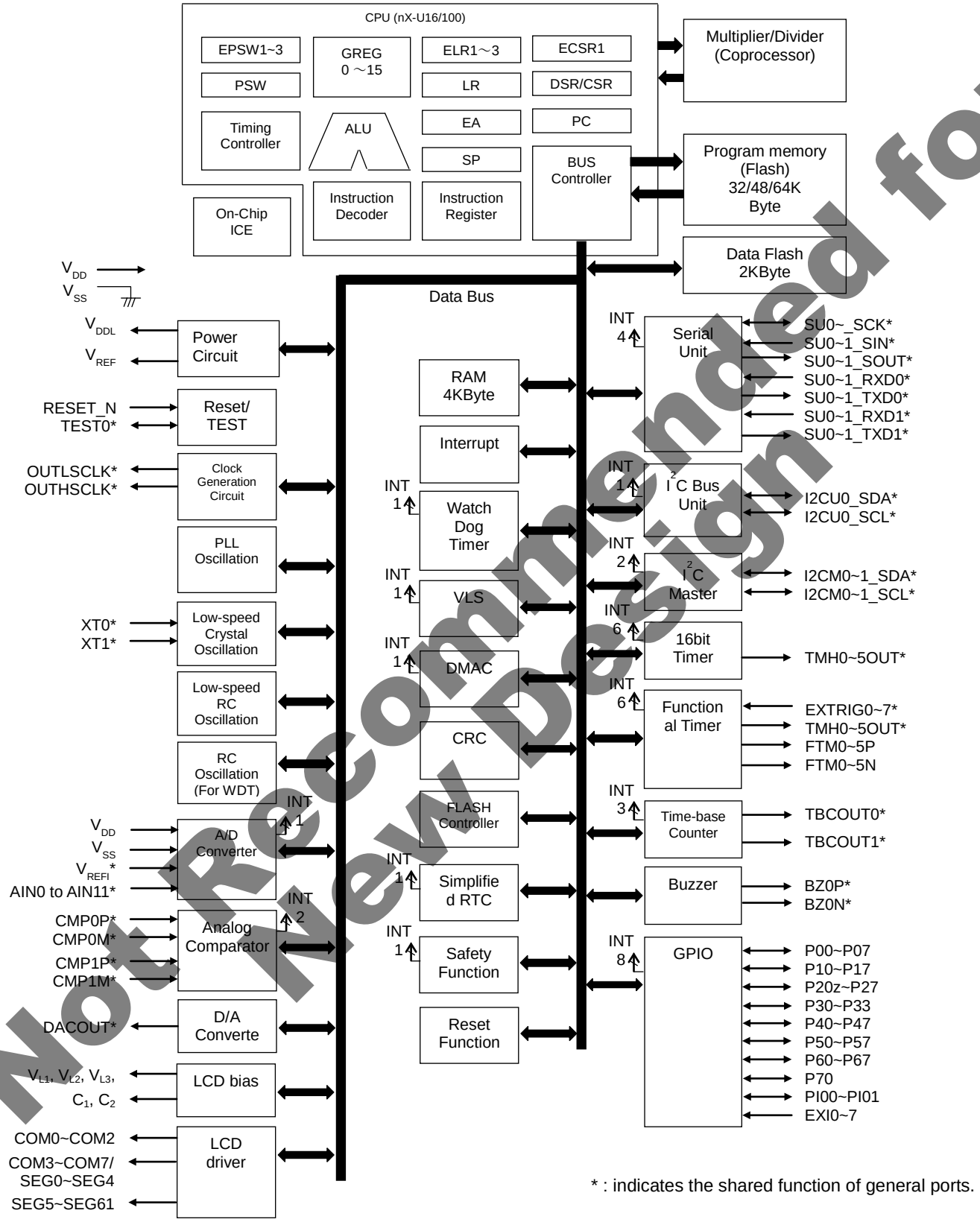
Part number	Pin						LCD drive pin				Interrupt		Timer			Serial			Analog			
	Total pin-counts	Power pin counts	Input reset pin	Input port *3	I/O port	LED drive port	LCD common/segment shared pin [number of pin] *4 *5	LCD common pin [number of pin] *5	LCD segment pin [number of pin] *5	LCD bias pin [number of pin]	Interna interrupt	External interrupt	Functional Timer [channel]	16bit General I Timer [channel] *1	Simplified RTC [channel]	Full-duplex UART or Synchronous serial [channel] *2	I2C bus unit (Master/Slave) [channel]	I2C bus interface (Master only) [channel]	10bit Sussesive type A/D converter [channel]	Analog comparator [channel]	Analog comparator [input pin]	8bit D/A converter [channel]
ML62Q1600																						
ML62Q1601	48				37	36			24													
ML62Q1602																						
ML62Q1610																						
ML62Q1611	52	3	1	2	41	40	5	3	27	5	30	8	6	6	1	2	1	2	12	2	4	1
ML62Q1612																						
ML62Q1620																						
ML62Q1621	64				53	52			35													
ML62Q1622																						

*1 : One 16bit timer is configurable as two 8bit timers
*2 : Full-duplex UART and Synchronous Serial Port can not be used simultaneously in the same channel.
One Full-duplexUART is configurable as two half-duplex UARTs.
*3 : Shared with pins for crystal oscillation
*4 : The LCD common/segment shared pins are shared for common or segment, selectable by setting a SFR
*5 : All LCD drive pins are shared with general purpose I/O ports.

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BLOCK DIAGRAM



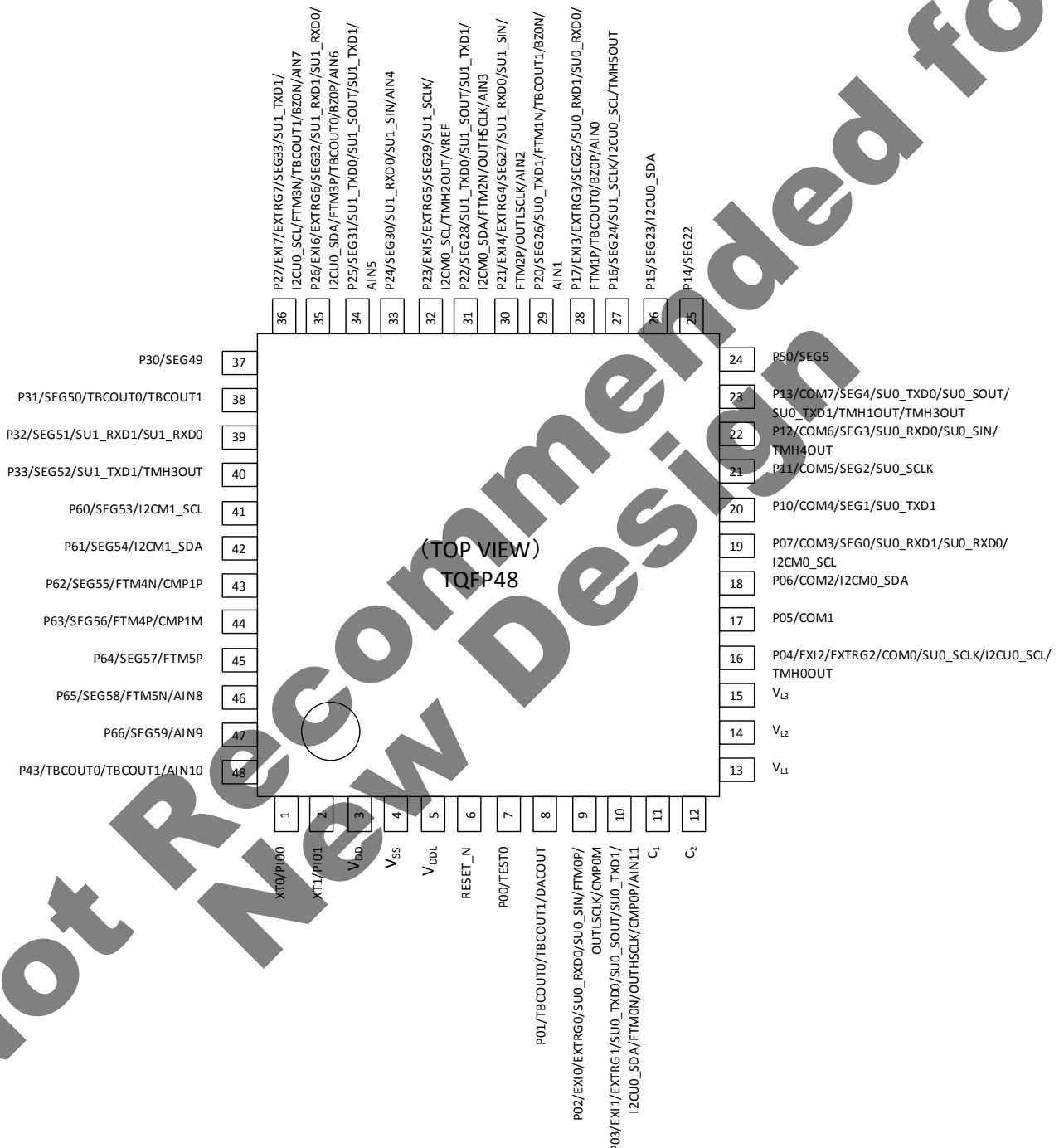
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Figure 2 ML62Q1600 Group Block Diagram

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PIN CONFIGURATION

Pin Layout of ML62Q1600/1601/1602 48pin TQFP Package

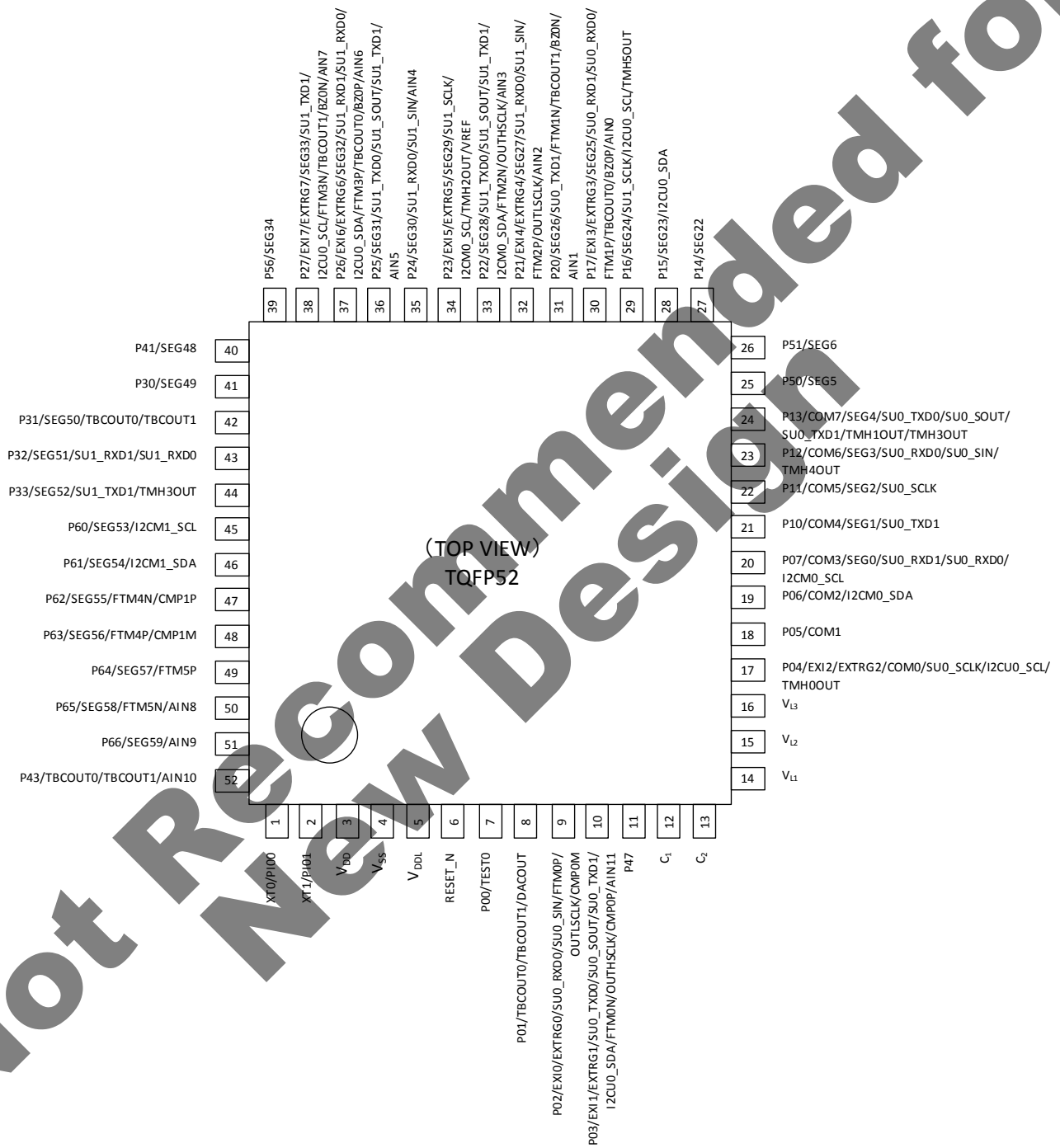


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Figure 3 Pin Layout of ML62Q1600/1601/1602 48pin TQFP Package

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Pin Layout of ML62Q1610/1611/1622 52pin TQFP Package



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Figure 4 Pin Layout of ML62Q1610/1611/1612 52pin TQFP52 Package

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Pin Layout of ML62Q1620/1621/1622 64pin TQFP/QFP Package

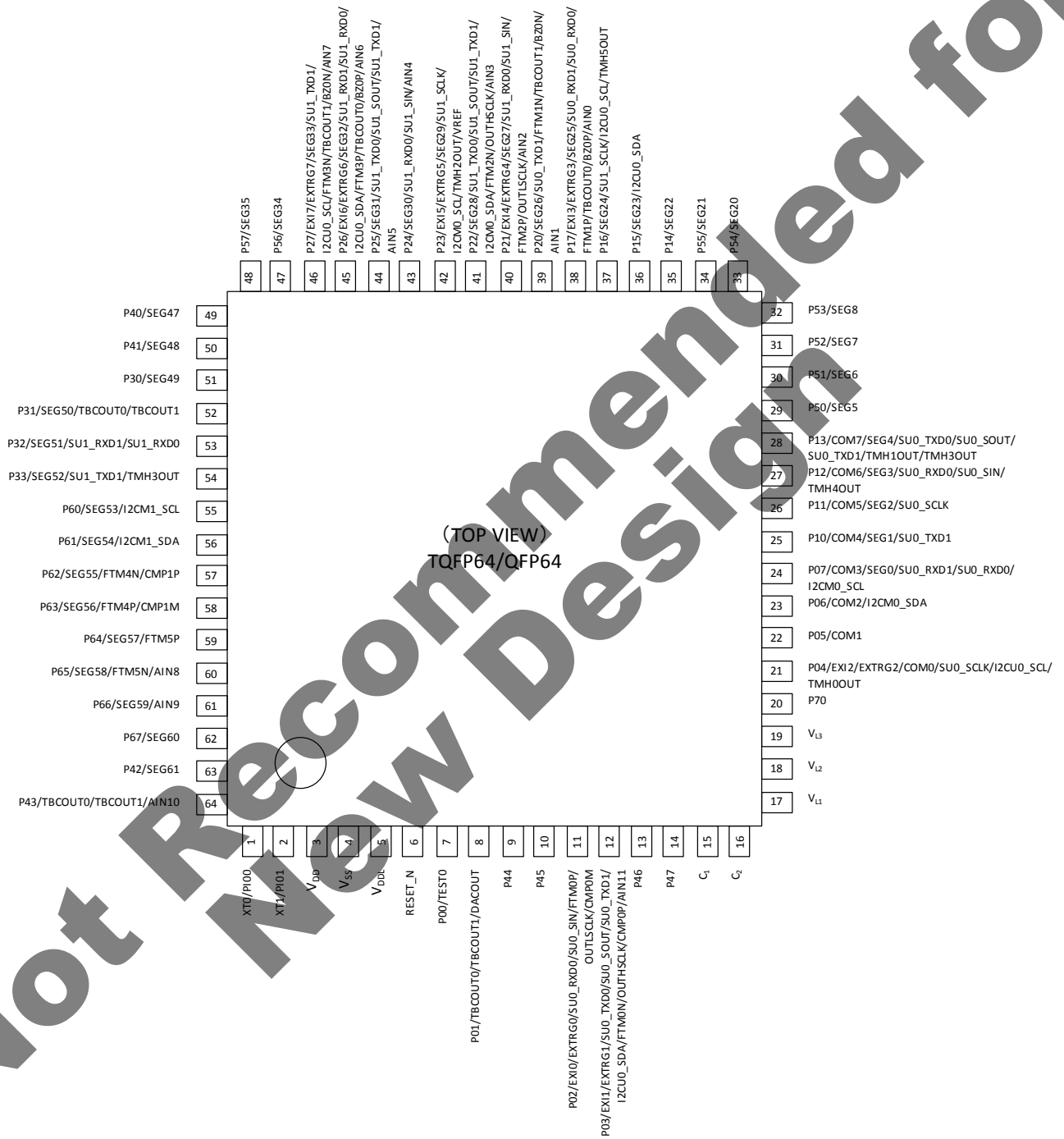


Figure 5 Pin Layout of ML62Q1620/1621/1622 64pin TQFP/QFP Package

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PIN LIST

Table 3 Pin List (1/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP)	Pn name	Primary function	Shared function	
3	3	3	3	V_{DD}	Positive power pin	−	
4	4	4	4	V_{SS}	Negative power pin	−	
5	5	5	5	V_{DDL}	Internal regulator output	−	
6	6	6	6	RESET_N (I)	Reset input Used for on-chip debug interface	−	
1	1	1	1	XT0 / PI00 (I)	General Input pin	Low speed crystal resonator connection pin	
2	2	2	2	XT1 / PI01 (I)	General Input pin	Low speed crystal resonator connection pin	
7	7	7	7	P00/ TEST0 （I/O）	General I/O pin Used for on-chip debug interface (Not available to use as I/O pin when connecting to the on-chip emulator)	−	
8	8	8	8	P01/ DACOUT (I/O)	General I/O pin D/A converter output pin	2nd function	−
						3rd function	−
						4th functiion	−
						5th function	−
						6th function	TBCOUT0
						7th function	TBCOUT1
						8th function	−
9	9	11	11	P02/ EXI0/ EXTRG0 (I/O)	General I/O pin External interrupt Functional timer external trigger	2nd function	SU0_RXD0/SU0_SIN
						3rd function	−
						4th functiion	−
						5th function	FTM0P
						6th function	OUTLSCLK
						7th function	CMP0M
						8th function	−
10	10	12	12	P03/ EXI1/ EXTRG1 (I/O)	General I/O pin External interrupt Functional timer external trigger	2nd function	SU0_TXD0/SU0_SOUT
						3rd function	SU0_TXD1
						4th functiion	I2CU0_SDA
						5th function	FTM0N
						6th function	OUTHSCLK
						7th function	CMP0P
						8th function	AIN11
16	17	21	21	P04/ EXI2/ EXTRG2/ COM0 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Common output pin	2nd function	SU0_SCLK
						3rd function	−
						4th functiion	I2CU0_SCL
						5th function	TMH0OUT
						6th function	−
						7th function	−
						8th function	−
17	18	22	22	P05/ COM1 (I/O)	General I/O pin LCD Common output pin	2nd function	−
						3rd function	−
						4th functiion	−
						5th function	−
						6th function	−
						7th function	−
						8th function	−

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Table 3 Pin List (2/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP)	Pn name	Primary function	Shared function	
18	19	23	23	P06 / COM2 (I/O)	General I/O pin LCD Common output pin	2nd function	—
						3rd function	—
						4th functiion	I2CM0_SDA
						5th function	—
						6th function	—
						7th function	—
						8th function	—
19	20	24	24	P07 / COM3 / SEG0 (I/O)	General I/O pin LCD Common output pin LCD Segment output pin	2nd function	SU0_RXD1
						3rd function	SU0_RXD0
						4th functiion	I2CM0_SCL
						5th function	—
						6th function	—
						7th function	—
						8th function	—
20	21	25	25	P10 / COM4 / SEG1 (I/O)	General I/O pin LCD Common output pin LCD Segment output pin	2nd function	SU0_TXD1
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—
21	22	26	26	P11 / COM5 / SEG2 (I/O)	General I/O pin LCD Common output pin LCD Segment output pin	2nd function	SU0_SCLK
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—
22	23	27	27	P12 COM6 / SEG3 (I/O)	General I/O pin LCD Common output pin LCD Segment output pin	2nd function	SU0_RXD0/SU0_SIN
						3rd function	—
						4th functiion	—
						5th function	TMH4OUT
						6th function	—
						7th function	—
						8th function	—
23	24	28	28	P13 COM7 / SEG4 (I/O)	General I/O pin LCD Common output pin LCD Segment output pin	2nd function	SU0_TXD0/SU0_SOUT
						3rd function	SU0_TXD1
						4th functiion	—
						5th function	TMH1OUT
						6th function	—
						7th function	TMH3OUT
						8th function	—
25	27	35	35	P14 / SEG22 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—

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Table 3 Pin List (3/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP).	Pn name	Primary function	Shared function	
26	28	36	36	P15 / SEG23 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	I2CU0_SDA
						5th function	—
						6th function	—
						7th function	—
						8th function	—
27	29	37	37	P16 / SEG24 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_SCLK
						3rd function	—
						4th functiion	I2CU0_SCL
						5th function	TMH5OUT
						6th function	—
						7th function	—
						8th function	—
28	30	38	38	P17 / EXI3/ EXTRG3 / SEG25 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Segment output pin	2nd function	SU0_RXD1
						3rd function	SU0_RXD0
						4th functiion	—
						5th function	FTM1P
						6th function	TBCOUT0
						7th function	BZ0P
						8th function	AIN0
29	31	39	39	P20 / SEG26 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU0_TXD1
						3rd function	—
						4th functiion	—
						5th function	FTM1N
						6th function	TBCOUT1
						7th function	BZ0N
						8th function	AIN1
30	32	40	40	P21 / EXI4 / EXTRG4 / SEG27 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Segment output pin	2nd function	SU1_RXD0/SU1_SIN
						3rd function	—
						4th functiion	—
						5th function	FTM2P
						6th function	OUTLSCLK
						7th function	—
						8th function	AIN2
31	33	41	41	P22 / SEG28 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_TXD0/SU1_SOUT
						3rd function	SU1_TXD1
						4th functiion	I2CM0_SDA
						5th function	FTM2N
						6th function	OUTHSCLK
						7th function	—
						8th function	AIN3
32	34	42	42	P23 / EXI5 / EXTRG5 / SEG29 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Segment output pin	2nd function	SU1_SCLK
						3rd function	—
						4th functiion	I2CM0_SCL
						5th function	TMH2OUT
						6th function	—
						7th function	—
						8th function	V_{REF}

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Table 3 Pin List (4/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP).	Pn name	Primary function	Shared function	
33	35	43	43	P24 / SEG30 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_RXD0/SU1_SIN
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	AIN4
34	36	44	44	P25 / SEG31 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_TXD0/SU1_SOUT
						3rd function	SU1_TXD1
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	AIN5
35	37	45	45	P26 / EXI6 / EXTRG6 / SEG32 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Segment output pin	2nd function	SU1_RXD1
						3rd function	SU1_RXD0
						4th functiion	I2CU0_SDA
						5th function	FTM3P
						6th function	TBCOUT0
						7th function	BZ0P
						8th function	AIN6
36	38	46	46	P27 / EXI7 / EXTRG7 / SEG33 (I/O)	General I/O pin External interrupt Functional timer external trigger LCD Segment output pin	2nd function	SU1_TXD1
						3rd function	—
						4th functiion	I2CU0_SCL
						5th function	FTM3N
						6th function	TBCOUT1
						7th function	BZ0N
						8th function	AIN7
37	41	51	51	P30 / SEG49 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—
38	42	52	52	P31 / SEG50 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	TBCOUT0
						7th function	TBCOUT1
						8th function	—

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Table 3 Pin List (5/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP)	Pn name	Primary function	Shared function	
39	43	53	53	P32 / SEG51 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_RXD1
						3rd function	SU1_RXD0
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
40	44	54	54	P33 / SEG52 (I/O)	General I/O pin LCD Segment output pin	2nd function	SU1_TXD1
						3rd function	
						4th functiion	–
						5th function	TMH3OUT
						6th function	–
						7th function	–
						8th function	–
–	–	49	49	P40 / SEG47 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	40	50	50	P41 / SEG48 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	63	63	P42 / SEG61 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
48	52	63	63	P43 (I/O)	General I/O pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	TBCOUT0
						7th function	TBCOUT1
						8th function	AIN10

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Table 3 Pin List (6/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP).	Pn name	Primary function	Shared function	
–	–	9	9	P44 (I/O)	General I/O pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	10	10	P45 (I/O)	General I/O pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	13	13	P46 (I/O)	General I/O pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	11	14	14	P47 (I/O)	General I/O pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
24	25	29	29	P50 / SEG5 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	26	30	30	P51 / SEG6 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–

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Table 3 Pin List (7/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP)	Pn name	Primary function	Shared function	
–	–	31	31	P52 / SEG7 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	32	32	P53 / SEG8 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	33	33	P54 / SEG20 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	34	34	P55 / SEG21 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	39	47	47	P56 / SEG34 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–
–	–	48	48	P57 / SEG35 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	–
						6th function	–
						7th function	–
						8th function	–

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Table 3 Pin List (8/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP)	Pn name	Primary function	Shared function	
41	45	55	55	P60 / SEG53 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	I2CM1_SCL
						5th function	–
						6th function	–
						7th function	–
						8th function	–
42	46	56	56	P61 / SEG54 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	I2CM1_SDA
						5th function	–
						6th function	–
						7th function	–
						8th function	–
43	47	57	57	P62 / SEG55 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	FTM4N
						6th function	–
						7th function	CMP1P
						8th function	–
44	48	58	58	P63 / SEG56 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	FTM4P
						6th function	–
						7th function	CMP1M
						8th function	–
45	49	59	59	P64 / SEG57 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	FTM5P
						6th function	–
						7th function	–
						8th function	–
46	50	60	60	P65 / SEG58 (I/O)	General I/O pin LCD Segment output pin	2nd function	–
						3rd function	–
						4th functiion	–
						5th function	FTM5N
						6th function	–
						7th function	–
						8th function	AIN8

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Table 3 Pin List (9/9)

48Pin No.	52Pin No.	64Pin No. (QFP)	64Pin No. (TQFP).	Pn name	Primary function	Shared function	
47	51	61	61	P66 / SEG59 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	AIN9
—	—	62	62	P67 / SEG60 (I/O)	General I/O pin LCD Segment output pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—
—	—	20	20	P70 (I/O)	General I/O pin	2nd function	—
						3rd function	—
						4th functiion	—
						5th function	—
						6th function	—
						7th function	—
						8th function	—
15	16	19	19	V_{L3}	LCD bias power source 3	—	
14	15	18	18	V_{L2}	LCD bias power source 2	—	
13	14	17	17	V_{L1}	LCD bias power source 1	—	
12	13	16	16	C_2	LCD bias power source generation capacitor connection pin 2	—	
11	12	15	15	C_1	LCD bias power source generation capacitor connection pin 1	—	

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PIN DESCRIPTION

Table 4 Pin Description (1/5)

Function	Signal name	Pin name	I/O	Description	Logic
Power	–	V_{SS}	–	Negative power supply pin (-)	–
	–	V_{DD}	–	Positive power supply pin (+). Connect a capacitor C_V (1µF) between this pin and V_{SS}.	–
	–	V_{DDL}	–	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C_V(1µF) between this pin and V_{SS}.	–
Test	TEST0	P00	I/O	Input pin for testing. Also, used for on-chip debug interface or ISP function. P00 is initialized as pull-up input mode by the system reset (not high-impedance mode).	Positive
System	V_{REF}	P23	–	Reference voltage output. An internal reference voltage in the SA type A/D converter block can be externally used for a reference. The pin is shared with the SA type A/D converter external reference voltage input.	–
	RESET_N	RESET_N	I	Input for reset. Asserting "L" level to this pin enters the MCU into system reset mode and internal circuits are initialized, then releasing it to "H" level make CPU start running the program. Used for on-chip debug interface or ISP function. Internal pull-up resistor is not installed.	Negative
	XT0	XT0	I	Low speed crystal oscillation pins Conenct 32.768kHz crystal resonator and have capacitors between the pin and V_{SS}.	–
	XT1	XT1	O		–
	OUTLSCLK	P02 P21	O	Low-speed clock output.	–
	OUTHSCLK	P03 P22	O	Low-speed clock output.	–
General input port (GPI)	PI00, PI01	XT0, XT1	I	General Input port Not available to use as general inputs when using the crystal resonator.	Positive
General port (GPIO)	P00	P00	I/O	General I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output P00 is only initialized as pulled-up input and other ports are initialized as high-impedence Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
	P01 - P07	P01 - P07	I/O	General I/O port - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 - P17	P10 - P17			
	P20 - P27	P20 - P27			
	P30 - P33	P30 - P33			
	P40 – P47	P40 – P47			
	P50 – P57	P50 – P57			
	P60 – P67	P60 – P67			
	P70	P70			

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Table 4 Pin Description (2/5)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03	O	Serial communication unit0/UART0 data output pin.	Positive
		P13			
	SU0_RXD0	P02	I	Serial communication unit0/UART0 data input pin.	Positive
		P07			
		P12			
		P17			
	SU0_TXD1	P03	O	Serial communication unit0/UART1 data output pin.	Positive
		P10			
		P13			
		P20			
	SU0_RXD1	P07	I	Serial communication unit0/UART1 data input pin.	Positive
		P17			
	SU1_TXD0	P22	O	Serial communication unit1/UART0 data output pin	Positive
		P25			
	SU1_RXD0	P21	I	Serial communication unit1/UART0 data input pin.	Positive
		P24			
		P26			
		P32			
	SU1_TXD1	P22	O	Serial communication unit1/UART1 data output pin.	Positive
		P25			
		P27			
		P33			
	SU1_RXD1	P26	I	Serial communication unit1/UART1 data input pin.	Positive
		P32			
Syncronous Serial Port	SU0_SIN	P02	I	Serial communication unit0/Synchronous serial data input pin.	Positive
		P12			
	SU0_SCK	P04	I/O	Serial communication unit0/Synchronous serial clock I/O pin.	Positive
		P11			
	SU0_SOUT	P03	O	Serial communication unit0/Synchronous serial data output pin.	Positive
		P13			
	SU1_SIN	P21	I	Serial communication unit1/Synchronous serial data input pin.	Positive
		P24			
	SU1_SCK	P16	I/O	Serial communication unit1/Synchronous serial clock I/O pin.	Positive
		P23			
	SU1_SOUT	P22	O	Serial communication unit1/Synchronous serial data output pin.	Positive
		P25			
I^2C Bus	I2CU0_SDA	P03	I/O	I^2C Unit0 (Master and Salve) Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P15			
		P26			
	I2CU0_SCL	P04	I/O	I^2C Unit0 (Master and Salve) Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P16			
		P27			
	I2CM0_SDA	P06	I/O	I^2C Master0 Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P22			
	I2CM0_SCL	P07	I/O	I^2C Master0 Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P23			
	I2CM1_SDA	P61	I/O	I^2C Master1 Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
	I2CM1_SCL	P60	I/O	I^2C Master1 Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive

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Table 4 Pin Description (3/5)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 output.	Positive
	FTM0N	P03	O	Functional Timer0 output.	Negative
	FTM1P	P17	O	Functional Timer1 output.	Positive
	FTM1N	P20	O	Functional Timer1 output.	Negative
	FTM2P	P21	O	Functional Timer2 output.	Positive
	FTM2N	P22	O	Functional Timer2 output.	Negative
	FTM3P	P26	O	Functional Timer3 output.	Positive
	FTM3N	P27	O	Functional Timer3 output.	Negative
	FTM4P	P63	O	Functional Timer4 output.	Positive
	FTM4N	P62	O	Functional Timer4 output.	Negative
	FTM5P	P64	O	Functional Timer5 output.	Positive
	FTM5N	P65	O	Functional Timer5 output.	Negative
	EXTRG0	P02	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG1	P03	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG2	P04	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG3	P17	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG4	P21	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG5	P23	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG6	P26	I	Functional Timer0-5 event trigger input pin.	—
	EXTRG7	P27	I	Functional Timer0-5 event trigger input pin.	—
16bit General Timer	TMH0OUT	P04	O	16bit General Timer 0 output pin	Positive
	TMH1OUT	P13	O	16bit General Timer 1 output pin	Positive
	TMH2OUT	P23	O	16bit General Timer 2 output pin	Positive
	TMH3OUT	P13 P33	O	16bit General Timer 3 output pin	Positive
	TMH4OUT	P12	O	16bit General Timer 4 output pin	Positive
	TMH5OUT	P16	O	16bit General Timer 5 output pin	Positive
Time Base Counter (TBC)	TBCOUT0	P01 P17 P26 P31 P43	O	Frequency adjustment clock output pin	Positive
	TBCOUT1	P01 P20 P27 P31 P43	O	Time Base Counter 1Hz/2Hz output pin	Positive
Buzzer	BZ0P	P17 P26	O	Buzzer output (positive phase)	Positive
	BZ0N	P20 P27	O	Buzzer output (negative phase)	Negative

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Table 4 Pin Description (4/5)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	GPIO maskable external interrupt pin	—
	EXI1	P03	I	GPIO maskable external interrupt pin	—
	EXI2	P04	I	GPIO maskable external interrupt pin	—
	EXI3	P17	I	GPIO maskable external interrupt pin	—
	EXI4	P21	I	GPIO maskable external interrupt pin	—
	EXI5	P23	I	GPIO maskable external interrupt pin	—
	EXI6	P26	I	GPIO maskable external interrupt pin	—
	EXI7	P27	I	GPIO maskable external interrupt pin	—
Successive approximation type A/D converter	V_{REFI}	P23	—	SA type A/D converter external reference voltage input. The voltage provided to the pin is used as the reference voltage for the A/D conversion.	—
	AIN0	P17	I	SA type A/D converter channel 0 input pin	—
	AIN1	P20	I	SA type A/D converter channel 1 input pin	—
	AIN2	P21	I	SA type A/D converter channel 2 input pin	—
	AIN3	P22	I	SA type A/D converter channel 3 input pin	—
	AIN4	P24	I	SA type A/D converter channel 4 input pin	—
	AIN5	P25	I	SA type A/D converter channel 5 input pin	—
	AIN6	P26	I	SA type A/D converter channel 6 input pin	—
	AIN7	P27	I	SA type A/D converter channel 7 input pin	—
	AIN8	P65	I	SA type A/D converter channel 8 input pin	—
	AIN9	P66	I	SA type A/D converter channel 9 input pin	—
	AIN10	P43	I	SA type A/D converter channel 10 input pin	—
	AIN11	P03	I	SA type A/D converter channel 11 input pin	—
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	—
	CMP0M	P02	I	Comparator input 0 (inverting input)	—
	CMP1P	P62	I	Comparator input 1 (noninverting input)	—
	CMP1M	P63	I	Comparator input 1 (inverting input)	—
D/A converter	DACOUT	P01	O	D/A converter output pin	—

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Table 4 Pin Description (5/5)

Function	Signal name	Pin name	I/O	Description	Logic
LCD driver	COM0	P04	—	Common output pin	—
	COM1	P05	—	Common output pin	—
	COM2	P06	—	Common output pin	—
	COM3/SEG0	P07	—	Common/Segment output shared pin	—
	COM4/SEG1	P10	—	Common/Segment output shared pin	—
	COM5/SEG2	P11	—	Common/Segment output shared pin	—
	COM6/SEG3	P12	—	Common/Segment output shared pin	—
	COM7/SEG4	P13	—	Common/Segment output shared pin	—
	SEG5	P50	—	Segment output pin	—
	SEG6	P51	—	Segment output pin	—
	SEG7	P52	—	Segment output pin	—
	SEG8	P53	—	Segment output pin	—
	SEG20	P54	—	Segment output pin	—
	SEG21	P55	—	Segment output pin	—
	SEG22	P14	—	Segment output pin	—
	SEG23	P15	—	Segment output pin	—
	SEG24	P16	—	Segment output pin	—
	SEG25	P17	—	Segment output pin	—
	SEG26	P20	—	Segment output pin	—
	SEG27	P21	—	Segment output pin	—
	SEG28	P22	—	Segment output pin	—
	SEG29	P23	—	Segment output pin	—
	SEG30	P24	—	Segment output pin	—
	SEG31	P25	—	Segment output pin	—
	SEG32	P26	—	Segment output pin	—
	SEG33	P27	—	Segment output pin	—
	SEG34	P56	—	Segment output pin	—
	SEG35	P57	—	Segment output pin	—
	SEG47	P40	—	Segment output pin	—
	SEG48	P41	—	Segment output pin	—
	SEG49	P30	—	Segment output pin	—
	SEG50	P31	—	Segment output pin	—
	SEG51	P32	—	Segment output pin	—
	SEG52	P33	—	Segment output pin	—
	SEG53	P60	—	Segment output pin	—
	SEG54	P61	—	Segment output pin	—
	SEG55	P62	—	Segment output pin	—
	SEG56	P63	—	Segment output pin	—
	SEG57	P64	—	Segment output pin	—
	SEG58	P65	—	Segment output pin	—
	SEG59	P66	—	Segment output pin	—
	SEG60	P67	—	Segment output pin	—
	SEG61	P42	—	Segment output pin	—
	C_1,C_2	C_1,C_2	—	LCD bias power source generation capacitor connection pin	—
	V_{L1}~V_{L3}	V_{L1}~V_{L3}	—	LCD bias power source pin. Connect the capacitors (C_{L1},C_{L2},C_{L3}) between the pin and Vss.	—

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TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	Recommended pin termination
RESET_N	Connect to V_{DD} through a resistor
P00/TEST0	Open the pin with the internal initial condition of pulled-up input mode.
XT0/PI00, XT1/PI01	Open the pins with the internal initial condition of Hi-impedance mode.
P01 to P07	
P10 to P17	
P20 to P27	
P30 to P33	
P40 to P47	
P50 to P57	
P60 to P67	
P70	
C_1, C_2	Open
V_{L1}	Open
V_{L2}	Open
V_{L3}	Connect to V_{DD} through a resistor

Note:
For unused input ports or unused input/output ports, if an unstable middle level voltage is supplied to the corresponding pins which are configured as inputs without pull-up register or input/output mode, supply current may become excessively large. Therefore, it is recommended to configure those pins as either input mode with a pull-up resistor or output mode.

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = +25°C		-0.3 to +2.0	V
Power supply voltage 3	V_{L3}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 4	V_{L1} ,V_{L2}	Ta = +25°C		-0.3 to V_{L3}+0.3*1	V
Input voltage	V_{IN}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
Output voltage1	V_{OUT1}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
Output voltage2	V_{OUT2}	Ta = +25°C		-0.3 to +6.5	V
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-150*2	
"L" level output current	I_{OUTL}	Ta = +25°C	1pin	+40	mA
			Total	+150	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	—		-55 to +150	°C

*1 6.5V or lower
*2 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
[Note] Use the product within absolute maximum ratings. The absolute maximum ratings are conditions which may physically deteriorate the quality of product.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	-40 to +105	°C
Operating voltage 1	V_{DD}	—	1.6 to 5.5	V
Operating voltage 2	V_{L3}	External supply method	2.7 to 5.5	V
Operating voltage 3	V_{L2}	External supply method	2/3 x V_{L3}	V
Operating voltage 4	V_{L1}	External supply method	1/3 x V_{L3}	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V_{DD} = 1.8 to 5.5V	30k to 25M	
V_{DDL} pin external capacitance	C_L	—	1.0 ±30%	µF
V_{L1},V_{L2},V_{L3} pin external capacitance	C_{L1},C_{L2}, C_{L3}	—	0.47±30% or 1.0±30%	µF
C_1 and C_2 pin external capacitance	C_{12}	—	0.47±30% or 1.0±30%	µF

Maker	Part number	Frequency (kHz)	Load capacitance CL(pf)	Oscillation mode	Oscillation circuit parameter C_{DL} (pf) *2*3	Oscillation circuit parameter C_{GL} (pf) *2*3
Kyocera	ST3215SB*1	32.768	7	Standard	13	13
				Low power	12	12
				Touch	13	13
			9		18	18
SII	VT-200F*1		12.5	Standard	22	22
			9	Low power	16	16
Daishinku	DST1610A*1		12.5	Touch	22	22

*1 These crystal resonator support the operating temperature up to +85°C. Ask the crystal resonator makers for the product supports +105°C.
*2 These includes wiring and parasitic capacitance.
*3 These are reference data. Please optimize them on user system.

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Current Consumption

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.5	20	µA	
			Ta = -40 to +105 °C	—	0.5	55		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.65	22	µA	
			Ta = -40 to +105 °C	—	0.65	60		
Supply current 2-1	IDD2-1	Internal RC Oscillating. CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped. LCD operation is stopped.	Ta = -40 to +85 °C	—	3.4	27	µA	
			Ta = -40 to +105 °C	—	3.4	67		
Supply current 2-2	IDD2-2	Low speed Crystal Oscillating. CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped. LCD operation is stopped.	Ta = -40 to +85 °C	—	2.2	27	µA	1
			Ta = -40 to +105 °C	—	2.2	67		
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock*1*2 PLL oscillation is stopped. LCD operation is stopped.	Ta = -40 to +105 °C	—	14	76	µA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*2 PLL 32MHz is oscillating. LCD operation is stopped. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	5.0	6.2	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*2 PLL 24MHz is oscillating. LCD operation is stopped. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	7.3	8.5		

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all "1"
*2 CPU running in wait mode

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Low speed Crystal Oscillation

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

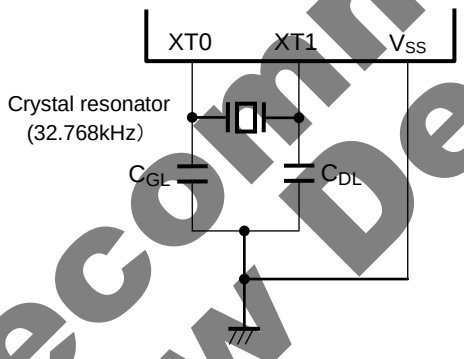
Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequeny *1 *2	f_{XTL}	—	—	32.768	—	kHz
Crystal oscillation start time	T_{XTL}	—	—	—	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, it requires evaluation on the actual PCB circuit for matching. Ask crystal resonator makers for matching and confirm the oscillation characteristics.

*2: The quality of oscillation characteristics might be lost, depending on material of PCB, condition of wiring capacitance or parasitic capacitance on the external circuits. Note for designing the external circuit.

- Make the wires on the external circuit as short as possible.
- Place the crystal resonator and oscillation circuit as close to the MCU as possible and make the wires between the external capacitance and crystal resonator as short as possible.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground VSS pin and connect them to the ground that has low variation of current and voltage.
  variation.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Low speed Crystal Oscillation external circuit example



External Clock Input

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	—	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	tEXCKW	—	1/fEXCK x 0.4		1/fEXCK x 0.6	s

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On-chip Oscillator

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1	f_{RCL1}	Ta= +25°C V_{DD} = 1.8 to 5.5V Without software adjustment *1	Typ -1.0%	32.768	Typ +1.0%	kHz	1
		Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V Without software adjustment *1	Typ -2.5%	32.768	Typ +2.5%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V Without software adjustment *1	Typ -3.0%	32.768	Typ +3.0%		
		V_{DD} = 1.6 to 1.8V Without software adjustment *1	Typ -3.5%	32.768	Typ +3.5%		
Low-speed RC oscillator frequency accuracy 2	f_{RCL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V With software adjustment *1	Typ -1.0%	32.768	Typ +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V With software adjustment *1	Typ -1.5%	32.768	Typ +1.5%		
PLL oscillation frequency accuracy 1	f_{PLL1}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V Without software adjustment *1	Typ -2.5%	16/24/32	Typ +2.5%	MHz	
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V Without software adjustment *1	Typ -3.0%	16/24/32	Typ +3.0%		
		V_{DD} = 1.6 to 1.8V Without software adjustment *1	Typ -3.5%	16/24/32	Typ +3.5%		
PLL oscillation frequency accuracy 2	f_{PLL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V With software adjustment *1	Typ -1.0%	16/24/32	Typ +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V With software adjustment *1	Typ -1.5%	16/24/32	Typ +1.5%		
PLL oscillation start time	T_{PLL}	V_{DD} = 1.6 to 5.5V	—	—	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f_{RC1K}	Ta= -40 to +105°C V_{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

*1 Adjust the frequency by using temperature sensor in ADC and a Specific Function Register (LRCADJ register)

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Input / Output pin 1

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage1 “H”/”L” level (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70)	VOH1	IOH1=-10mA V_{DD}≧4.5V		V_{DD} -1.5	—	—	V	2
		IOH1=-1mA V_{DD}≧1.6V		V_{DD} -0.5	—	—		
	VOL1	IOL1=+10mA V_{DD}≧4.5V		—	—	1.5		
		IOL1=+1mA V_{DD}≧1.6V		—	—	0.5		
Output voltage2 “L” level (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70)	VOL2	When Nch open drain output mode is selected	IOL2=+15mA V_{DD}≧4.5V	—	—	0.7		
			IOL2=+8mA V_{DD}≧3.0V	—	—	0.5		
			IOL2=+3mA V_{DD}≧2.0V	—	—	0.4		
			IOL2=+2mA 2.0V＞V_{DD}≧1.6V	—	—	0.4		
Output voltage 3 LCD COM/SEG (COM0~COM7) (SEG0~SEG61)	VOH3M	V_{L3} = 3V, V_{L2} = 2V, V_{L1} = 1V	IOH3M=-0.03mA V_{L3} output	V_{L3} -0.2	—	—	V	2
	VOH3P		IOMH3P=+0.03mA V_{L2} output	—	—	V_{L2} +0.2		
	VOMH3M		IOMH3M=-0.03mA V_{L2} output	V_{L2} -0.2	—	—		
	VOML3P		IOML3P=+0.03mA V_{L1} output	—	—	V_{L1} +0.2		
	VOML3M		IOML3M=-0.03mA V_{L1} output	V_{L1} -0.2	—	—		
	VOL3P		IOL3P=+0.03mA V_{SS} output	—	—	0.2		

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Input / Output pin 2

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
"H" level output current1 *1*4	IOH1	1pin	V_{DD}≧4.5V	-10*3*5	—	—	mA	3
			V_{DD}≧1.6V	-1*3*5	—	—		
		Total of P00~P07, P10~P13, P44~P47, P50~P53 and P70 (duty≦50%)	V_{DD}≧4.5V	-90*5	—	—		
			V_{DD}≧1.6V	-20*5	—	—		
		Total of P14~P17, P20~P27, P30~P33, P40~P43, P54~P57 and P60~P67 (duty≦50%)	V_{DD}≧4.5V	-90*5	—	—		
			V_{DD}≧1.6V	-20*5	—	—		
		All pin total (duty≦50%)	V_{DD}≧4.5V	-180*5	—	—		
			V_{DD}≧1.6V	-40*5	—	—		
"L" level output current1 *2	IOL1	1pin (CMOS outpu mode)	V_{DD}≧4.5V	—	—	10*3		
			V_{DD}≧1.6V	—	—	1*3		
"L" level output current2 *2	IOL2	1pin (Nch open drain output mode)	V_{DD}≧4.5V	—	—	15*3		
			V_{DD}≧3.0V	—	—	8*3		
			V_{DD}≧2.0V	—	—	3*3		
			V_{DD}≧1.6V	—	—	2*3		
"L" level output current Total *2*4	IOL3	Total of P00~P07, P10~P13, P44~P47, P50~P53 and P70 (duty≦50% *6)	V_{DD}≧4.5V	—	—	90		
			V_{DD}≧3.0V	—	—	40		
			V_{DD}≧2.0V	—	—	15		
			2.0V＞V_{DD}≧1.6V	—	—	10		
		Total of P14~P17, P20~P27, P30~P33, P40~P43, P54~P57 and P60~P67 (duty≦50% *6)	V_{DD}≧4.5V	—	—	90		
			V_{DD}≧3.0V	—	—	40		
			V_{DD}≧2.0V	—	—	15		
			2.0V＞V_{DD}≧1.6V	—	—	10		
		All pin total (duty≦50% *6)	V_{DD}≧4.5V	—	—	180		
			2.0V＞V_{DD}≧1.6V	—	—	20		
Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67), (P70)	IOOH	VOH=V_{DD} (High impedance mode)		—	—	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	—	—		

*1 Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.
*2 Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.
*3 Do not beyond total current.
*4 The total current is on the condition of Duty≦50%(same applies to IOH1).
When the duty ＞50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6 Nch open drain output mode

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(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-1*1	—	—		
Input current2 (P00/TEST0)	IIL2	VIL2=V_{SS} (pull-up mode)	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2=V_{SS} (pull-up mode)	3.7	10	80	kΩ	
	IIH2Z	VIH2=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL2Z	VIL2=V_{SS} (High impedance mode)	-1*1	—	—		
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70)	IIL3	VIL3=V_{SS}(pull-up mode)	-250*1	-30*1	-2*1		
	V/IIL3	VIL3=V_{SS} (pull-up mode)	22	100	800	kΩ	
	IIH3Z	VIH3=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL3Z	VIL3=V_{SS} (High impedance mode)	-1*1	—	—		
Input current4 (PI00-PI01)	IIH4	VIH4=V_{DD}	—	—	1		
	IIL4	VIL4=V_{SS}	-1*1	—	—		
Input voltage1 (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70) (PI00~PI01)	VIH1	—	0.7 x V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3 x V_{DD}		
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70) (PI00~PI01)	CPIN	f = 10kHz Ta = +25°C	—	—	10	pF	—

*1 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

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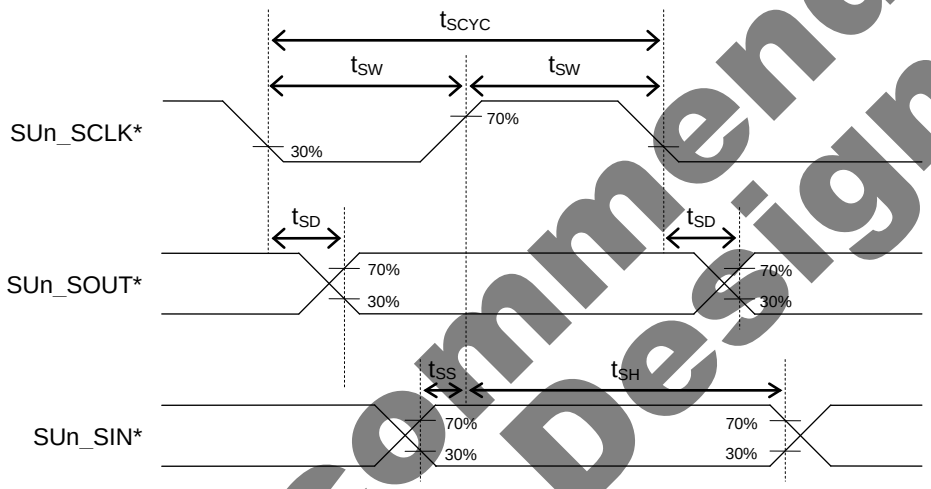
Synchronous Serial Port

Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t_{SCYC}	—	1 *2	—	—	µs
SCK input pulse width	t_{SW}	—	0.5 *3	—	—	µs
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100+ HSCLK*1×3	ns
		V_{DD}=1.8 to 5.5V	—	—	200+ HSCLK*1×3	ns
SIN input setup time	t_{SS}	—	HSCLK*1 x1	—	—	ns
SIN input hold time	t_{SH}	—	80+ HSCLK*1×3	—	—	ns

*1 Cycle of high speed clock
*2 Need input cycles of HSLCK x8 or longer
*3 Need input cycles of HSLCK x4 or longer



* 2nd to 8th function of port, n=0~1

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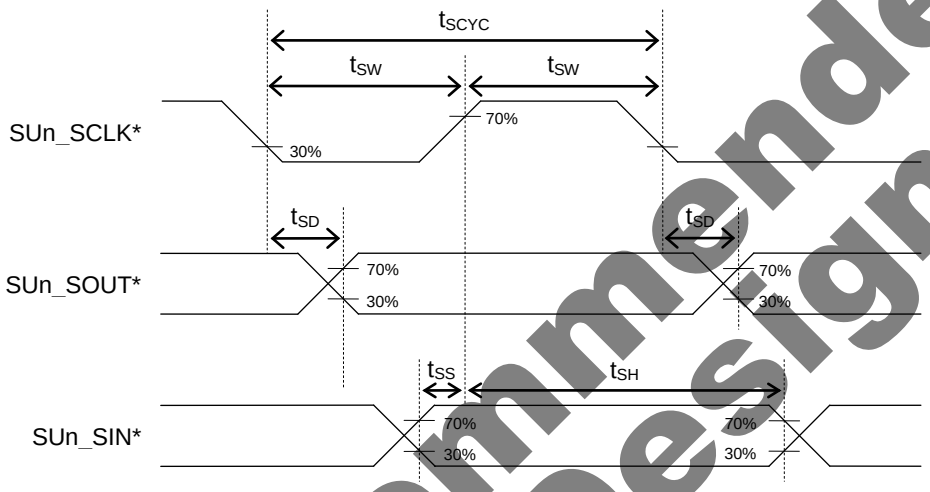
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Master mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t_{SCYC}	—	—	SCLK*[1]	—	ns
SCK output pulse width	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	ns
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100	ns
		V_{DD}=1.8 to 5.5V	—	—	160	ns
SIN input setup time	t_{SS}	V_{DD}=2.4 to 5.5V	120	—	—	ns
		V_{DD}=1.8 to 5.5V	180	—	—	ns
SIN input hold time	t_{SH}	V_{DD}=2.4 to 5.5V	80	—	—	ns
		V_{DD}=1.8 to 5.5V	100	—	—	

*[1] Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIOnMOD)
VDD≧2.4V: min250ns , VDD≧1.8V: min500ns



* 2nd to 8th function of port, n=0~1

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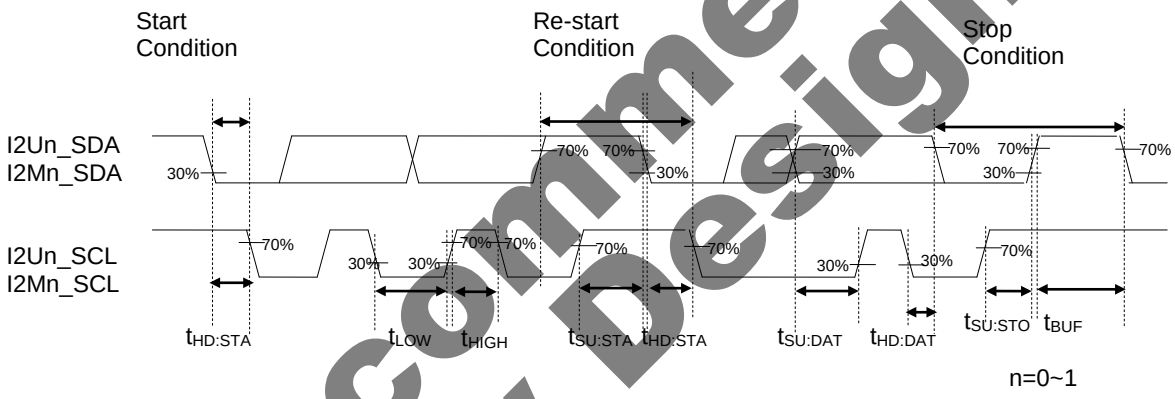
I²C Bus Interface

Standard Mode 100kHz

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



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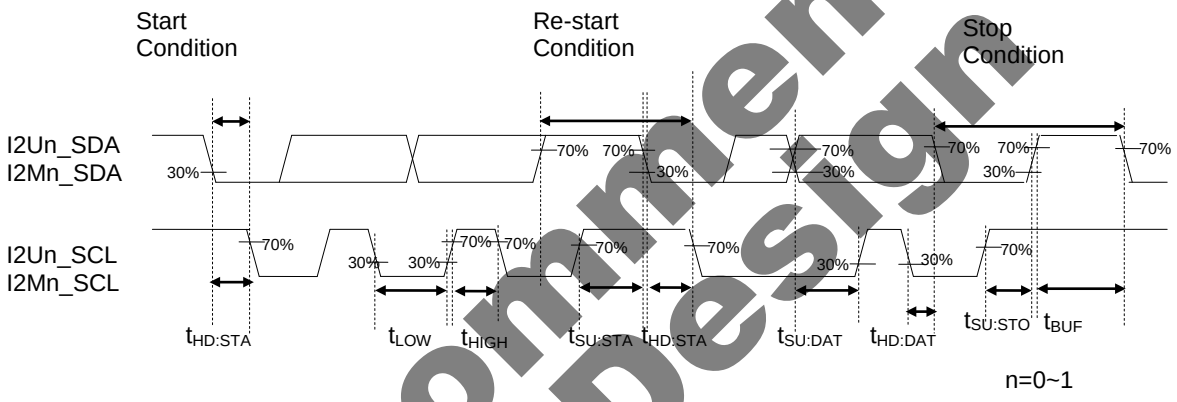
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Fast Mode 400kHz

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



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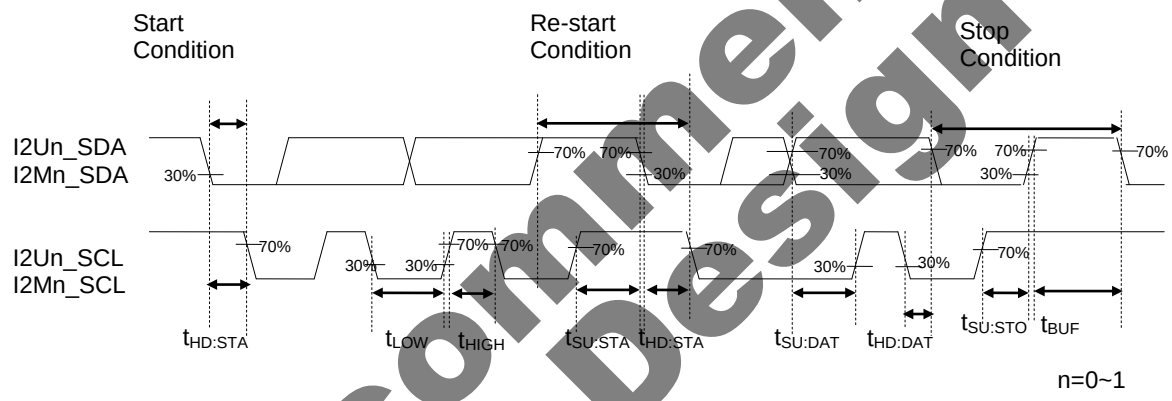
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1Mbps Mode

(V_{DD}=2.7 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.26	—	—	µs
SCL "L" level time	t_{LOW}	—	0.5	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.26	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.26	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.26	—	—	µs
Bus-free time	t_{BUF}	—	0.5	—	—	µs

When using the I^2C as the master, configure the I^2C master n mode register(I2MnMOD) and I^2C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



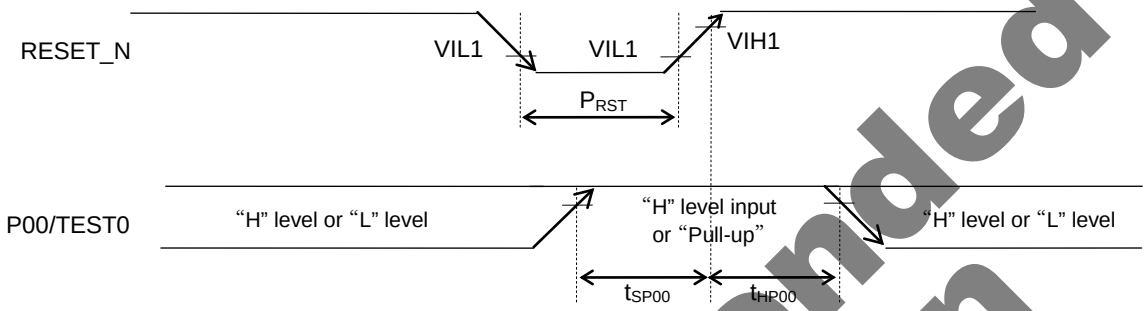
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Reset

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width	P_{RST}	—	2	—	—	ms	1
P00 "H" level setup time	t_{SP00}	—	1	—	—	ms	
P00 "L" level hold time	t_{HP00}	—	1	—	—	ms	

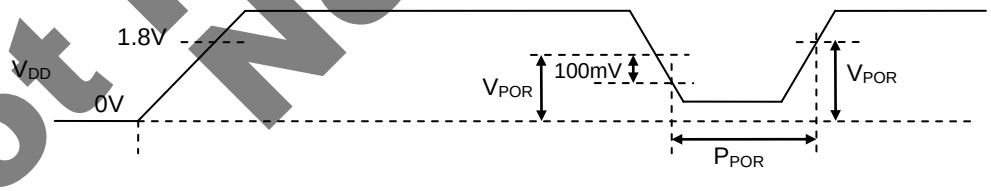


Power On Reset

(V_{SS} =0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
POR detect voltage	V_{POR}	Power down(falling)	1.44	1.5	1.58	V	1
		Power up(rising)	1.45	1.53	1.8	V	
Power on rising slope	R_{POR}*1	—	0.009	—	60	V/ms	
POR response time	P_{POR}	*2	200	—	—	µs	

*1: Rise the V_{DD} to 1.8V or higher when powering on.
*2: This is the time from the V_{DD} gets 100mV lower than V_{POR} to the Power-On-Reset internlly genertes.
Make the power down falling slope 2V/ms or lower(i.e. slower).



[Note for in case of instantaneous power failure]
In case of instantaneous power failure and a pulse shorter than the response time of VLS or POR is asserted to V_{DD}, it is possible to make the MCU cannot get the reset and make erroneous operation. In that case, please have countermeasures such as preventing the voltage down using bypass capacitor or making reset pin reset.

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VLS

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition VLS0LV *1		Min.	Typ.	Max.	Unit	Measuring circuit
VLS threshold voltage *2	V_{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V_{VLSF}		Falling	3.84	4.00	4.16		
	V_{VLSR}	01H	Rising	3.57	3.76	3.95		
	V_{VLSF}		Falling	3.55	3.70	3.85		
	V_{VLSR}	02H	Rising	2.94	3.11	3.28		
	V_{VLSF}		Falling	2.92	3.05	3.18		
	V_{VLSR}	03H	Rising	2.85	3.01	3.17		
	V_{VLSF}		Falling	2.83	2.95	3.07		
	V_{VLSR}	04H	Rising	2.75	2.91	3.07		
	V_{VLSF}		Falling	2.73	2.85	2.97		
	V_{VLSR}	05H	Rising	2.66	2.81	2.96		
	V_{VLSF}		Falling	2.64	2.75	2.86		
	V_{VLSR}	06H	Rising	2.56	2.71	2.86		
	V_{VLSF}		Falling	2.54	2.65	2.76		
	V_{VLSR}	07H	Rising	2.46	2.61	2.76		
	V_{VLSF}		Falling	2.44	2.55	2.66		
	V_{VLSR}	08H	Rising	2.37	2.51	2.65		
	V_{VLSF}		Falling	2.35	2.45	2.55		
	V_{VLSR}	09H	Rising	1.98	2.11	2.24		
	V_{VLSF}		Falling	1.96	2.05	2.14		
	V_{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V_{VLSF}		Falling	1.87	1.95	2.03		
	V_{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V_{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I_{VLS}	—		—	50	—	nA	

*1 Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

*2 The Data VSL0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V_{CMR}	—	0.1	—	V_{DD} -1.5	V	1
Comparator0 input offset	V_{CMOF}	Ta=+25 °C、V_{DD}=5.0V	—	5	—	mV	
Comparator Reference Voltage	V_{CMREF}	—	0.75	0.8	0.85	V	

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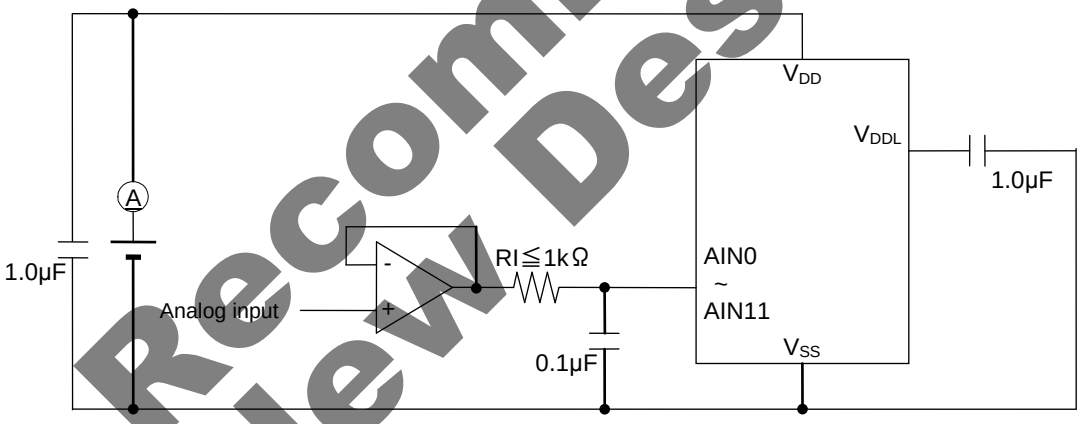
Successive Approximation Type A/D Converter

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bit
Integral non-linearity error	AINL	2.7V≦V_{REFP} *1≦5.5V	-4	—	4	LSB
		2.2V≦V_{REFP} *1＜2.7V	-6	—	6	
		1.8V≦V_{REFP} *1＜2.2V	-10	—	10	
		V_{REFP}=Internal reference voltage	-15	—	15	
Differential non-linearity error	ADNL	2.7V≦V_{REFP} *1≦5.5V	-3	—	3	
		2.2V≦V_{REFP} *1＜2.7V	-5	—	5	
		1.8V≦V_{REFP} *1＜2.2V	-9	—	9	
		V_{REFP}=Internal reference voltage	-14	—	14	
Zero-scale error	ZSE	RI≦1kΩ	-6	—	6	
Full-scale error	FSE	RI≦1kΩ	-6	—	6	
A/D reference voltage	V_{REFx}	—	1.8	—	V_{DD}	V
Internal reference voltage	V_{REFI}	—	1.5	1.55	1.6	
Conversion time	t_{CONV}	4.5V≦V_{DD} ≦5.5V	2.25	—	427	μs
		2.2V≦V_{DD}≦5.5V	4.5	—	427	
		1.8V≦V_{DD}≦5.5V	18	—	427	

*1 : VDD or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter by setting bit5(VREFP1) and bit4(VREFP0) of SA-ADC TEMP/VREF control register(VREFCON).

The current flows during the ADC sampling as it takes charging. Make the output impedance of the anlog signal source 1k Ω or smaller. Also, putting 0.1uF capacitor on the ADC input pin is recommended to reduce the noise.



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D/A Converter

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	Dn	—	—	—	8	bit
Conversion cycle	tc	—	10	—	—	µs
Integral non-linearity error	DINL	RL=4MΩ	-2	—	2	LSB
Differential non-linearity error	DDNL	RL=4MΩ	-1	—	1	
Output impedance	Ro	DACEN bit of D/A converter enable register =1	3	6	9	kΩ

Reference Voltage Output

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REFOUT}	—	—	1.55	—	V
Output impedance	$R_{VREFOUT}$	—	—	—	500	kΩ

Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash (1024Byte x2)		10000	times
	CEPP	Program Flash		100	
Erase unit	—	Block erase	Program Flash	16K	B
			Data Flash	2K	
	—	Sector erase	Program Flash	1K	B
			Data Flash	128	
Erase time (Max.)	—	Block erase / Sector erase		85	ms
Write unit	—	Program Flash		4	B
		Data Flash		1	
Write time (Max.)	—	Program Flash		80	µs
		Data Flash		40	
Data retention period	YDR	—		15	years

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LCD Driver

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

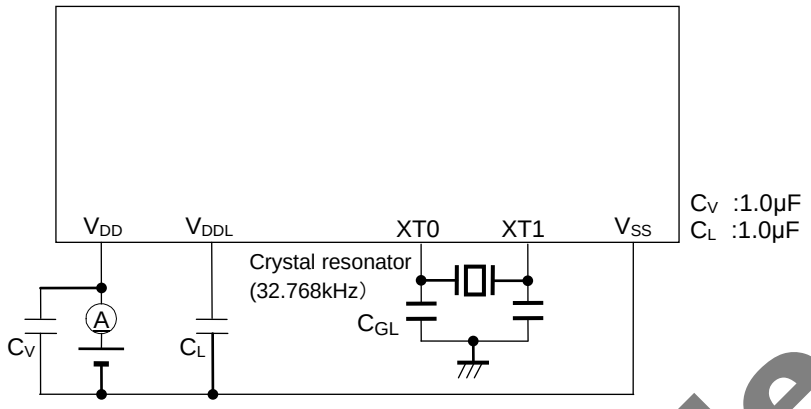
Parameter	Symbol	Condition		Range			Unit
			LCN*1	Min.	Typ.	Max.	
V_{L1} Voltage	V_{L1}	Ta=+25 °C $C_{L1,L2,L3}$=0.47µF	00H	Typ -0.05	0.950	Typ +0.05	V
			01H		0.975		
			02H		1.000		
			03H		1.025		
			04H		1.050		
			05H		1.075		
			06H		1.100		
			07H		1.125		
			08H		1.150		
			09H		1.175		
			0AH		1.200		
			0BH		1.225		
			0CH		1.250		
			0DH		1.275		
			0EH		1.300		
			0FH		1.325		
			10H		1.350		
			11H		1.375		
			12H		1.400		
			13H		1.425		
			14H		1.450		
			15H		1.475		
			16H		1.500		
			17H		1.525		
			18H		1.550		
			19H		1.575		
			1AH		1.600		
			1BH		1.625		
			1CH		1.650		
			1DH		1.675		
			1EH		1.700		
			1FH		1.725		
V_{L2} Voltage	V_{L2}	Ta=+25 °C C_{L1},C_{L2},C_{L3}=0.47µF C_{12}=0.47µF		V_{L1} x 1.8	V_{L1} x 2	—	V
V_{L3} Voltage	V_{L3}			V_{L1} x 2.7	V_{L1} x 3	—	
Bias generation circuit start-up time	t_{BIAS}			—	—	200	ms

*1 : Value in LCN4~LCN0 bits of bias control register (BIASCON)

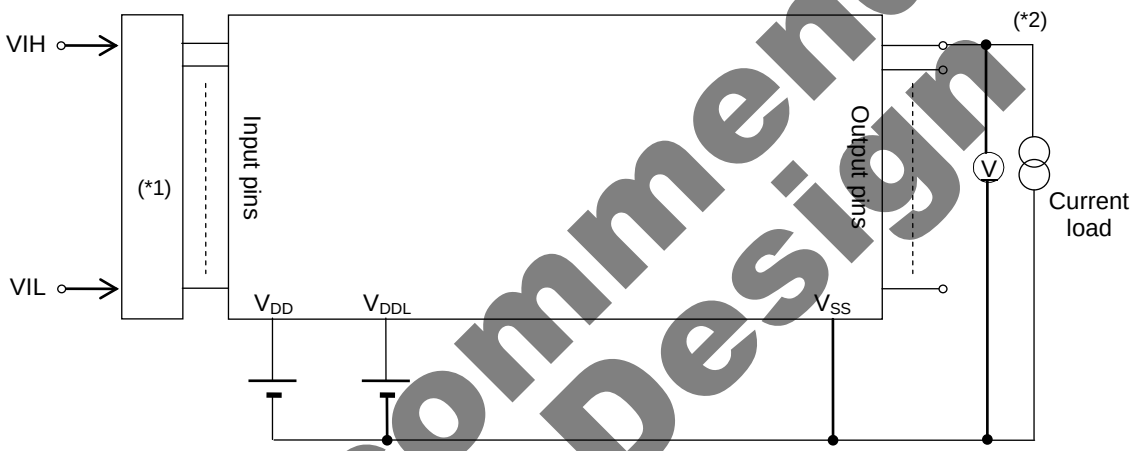
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Measuring circuit 1

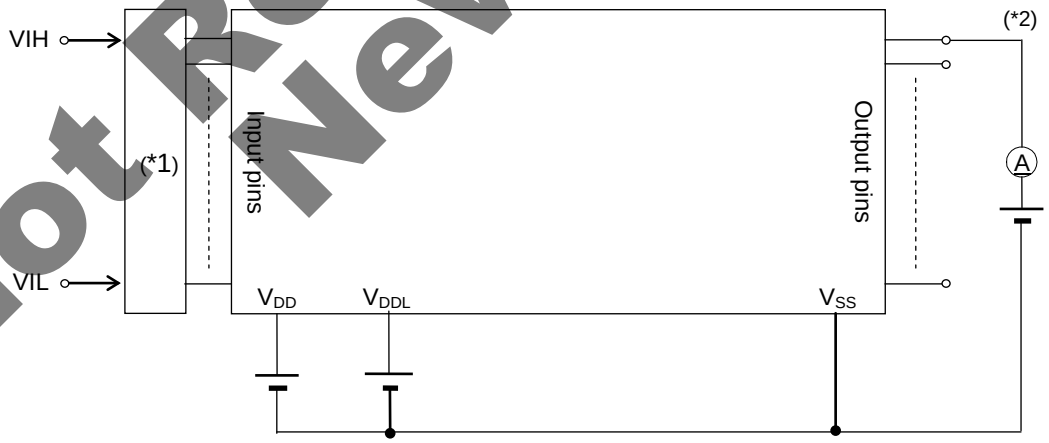


Measuring circuit 2



(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 3

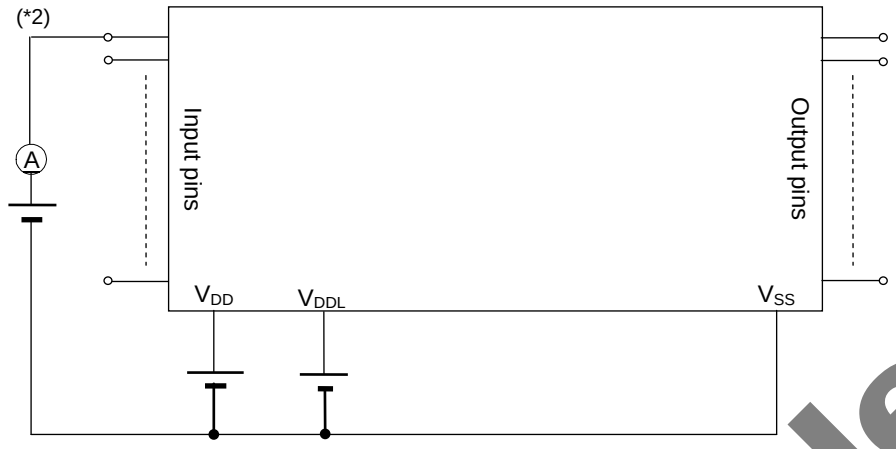


(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

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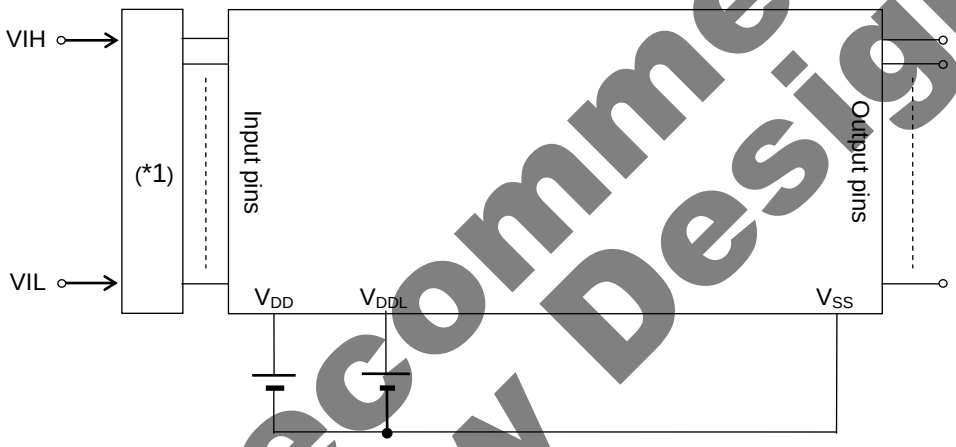
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Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5



(*1) Input logic circuit to determine the specified measuring conditions

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Characteristics graphs

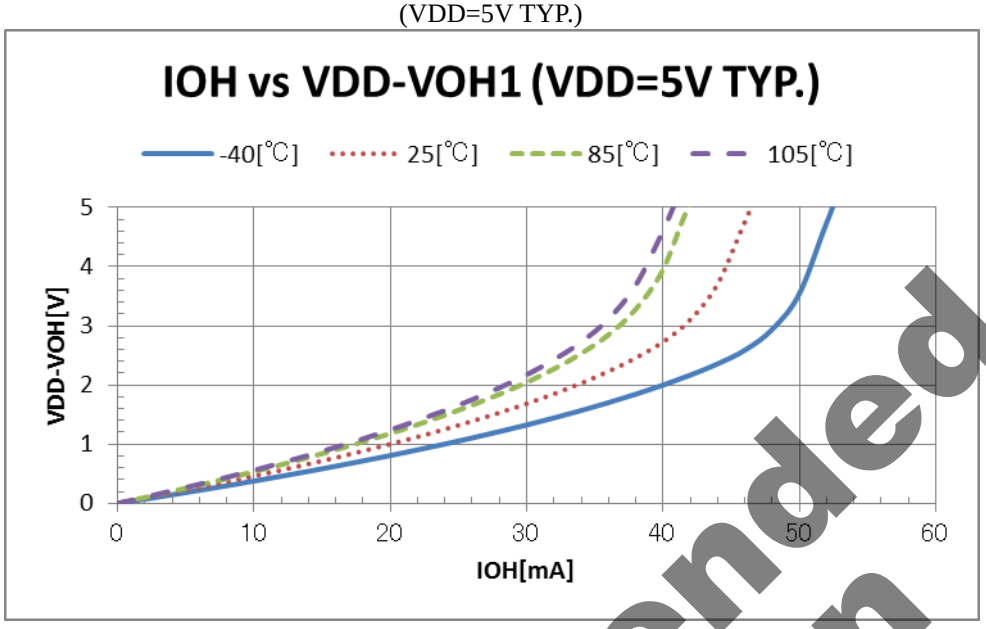
These Graphs on the following pages are references for designing an application.

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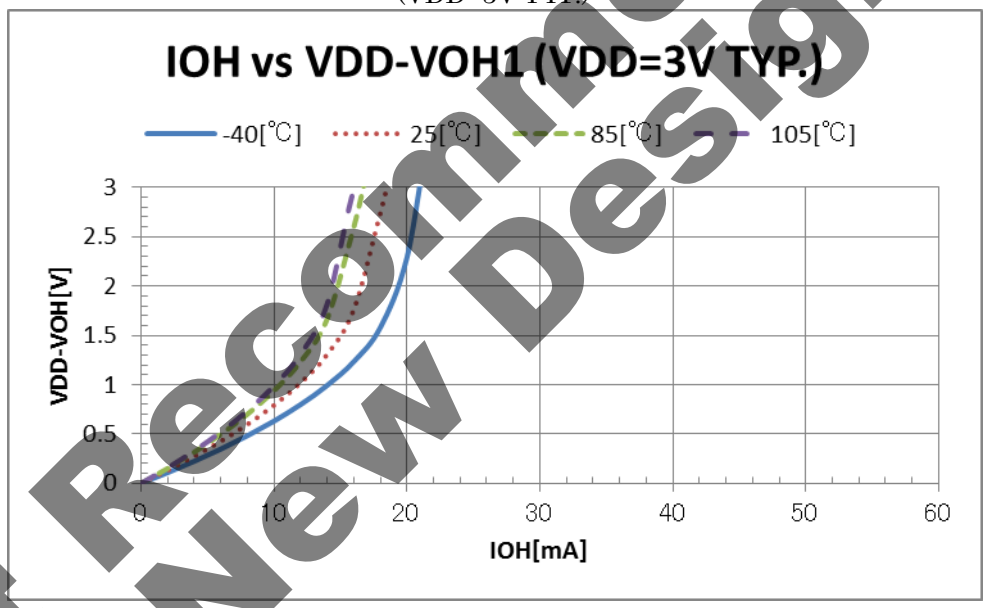
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IOH VS VDD-VOH1

(VDD=5V TYP.)



(VDD=3V TYP.)

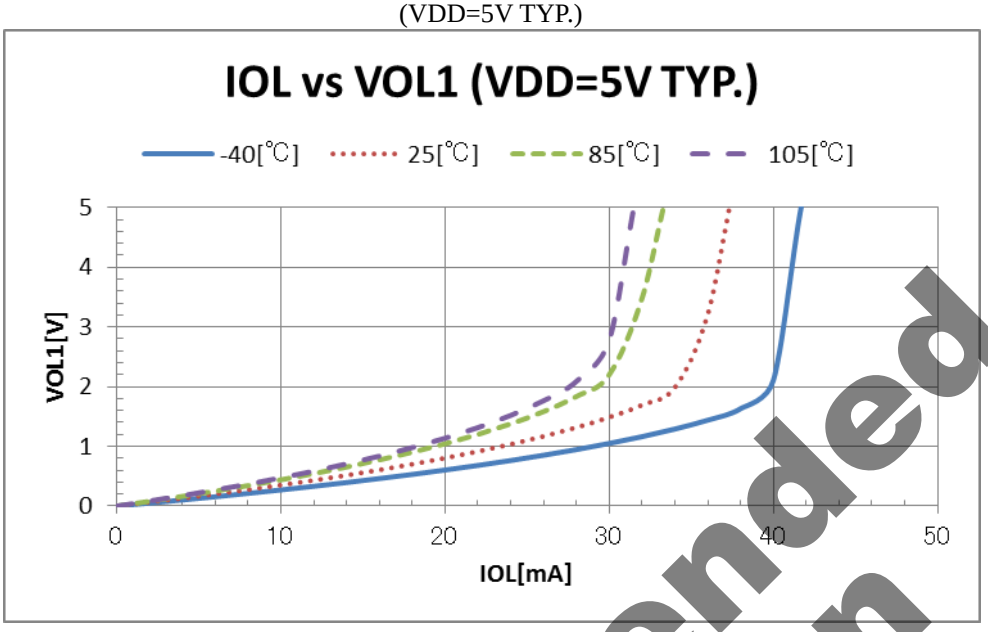


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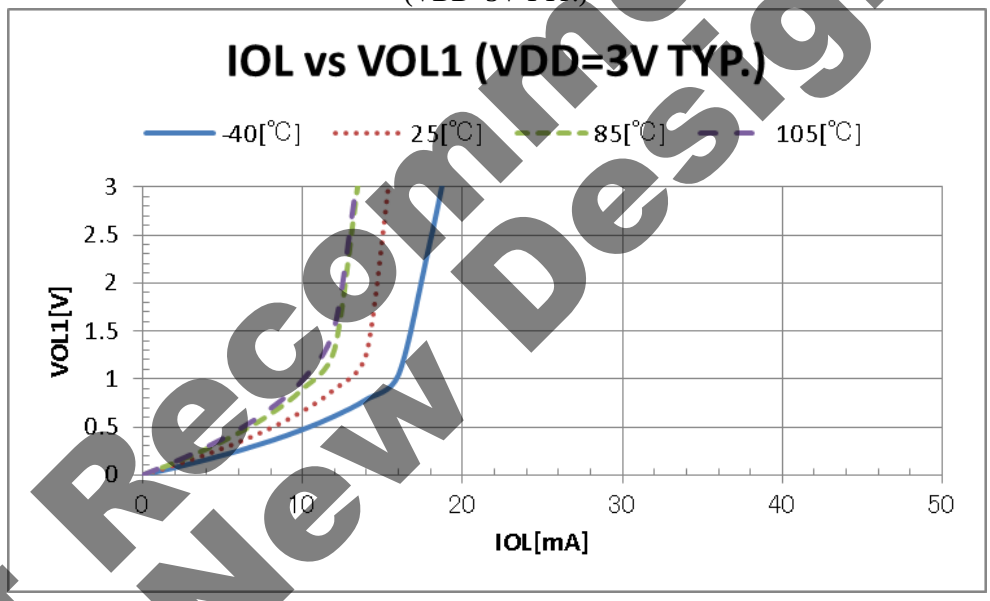
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IOL VS VOL1

(VDD=5V TYP.)



(VDD=3V TYP.)

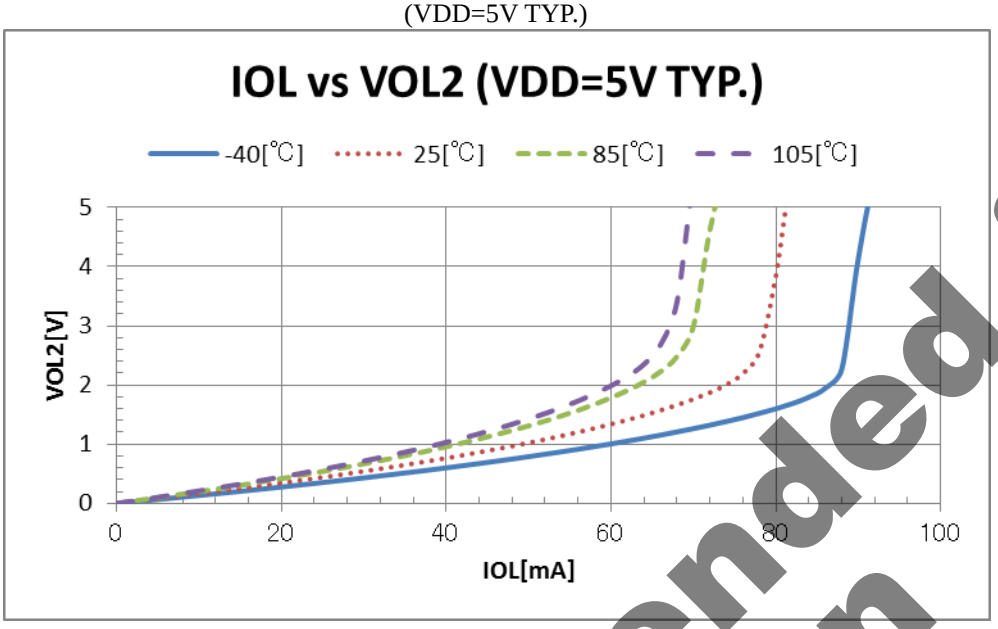


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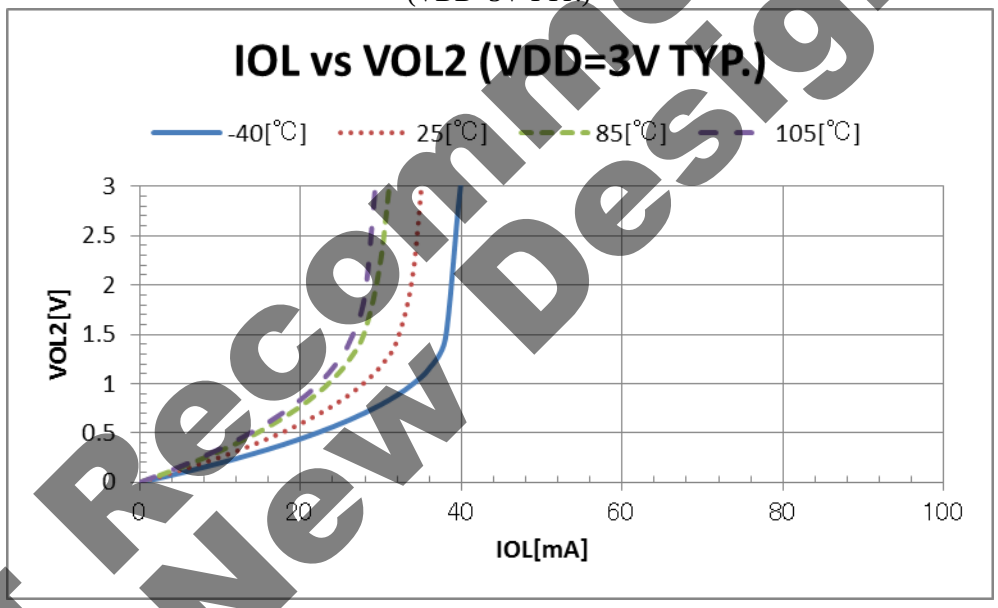
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IOL VS VOL2

(VDD=5V TYP.)



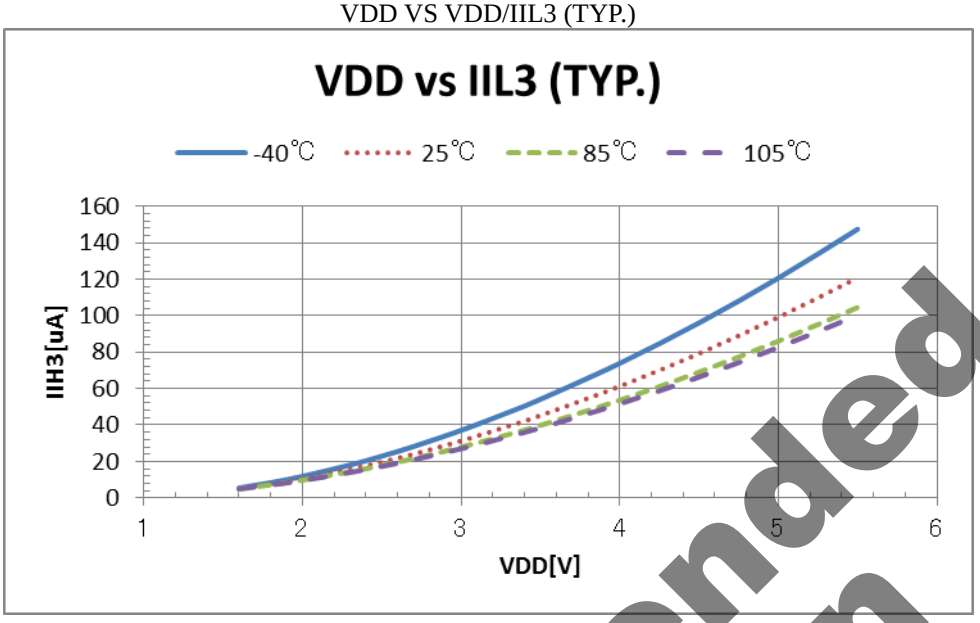
(VDD=3V TYP.)



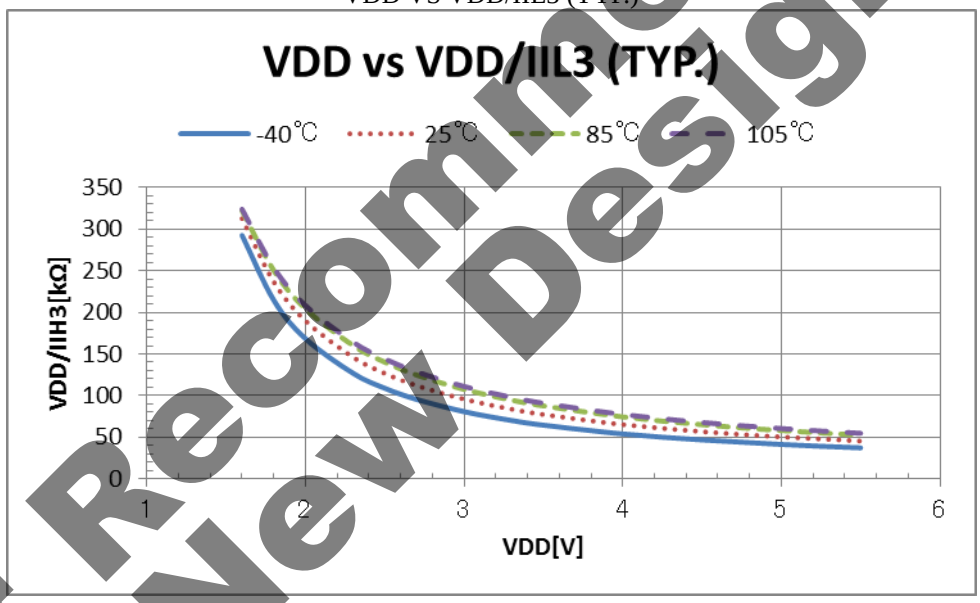
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VDD VS VDD/IIL3 (TYP.)



VDD VS VDD/IIL3 (TYP.)

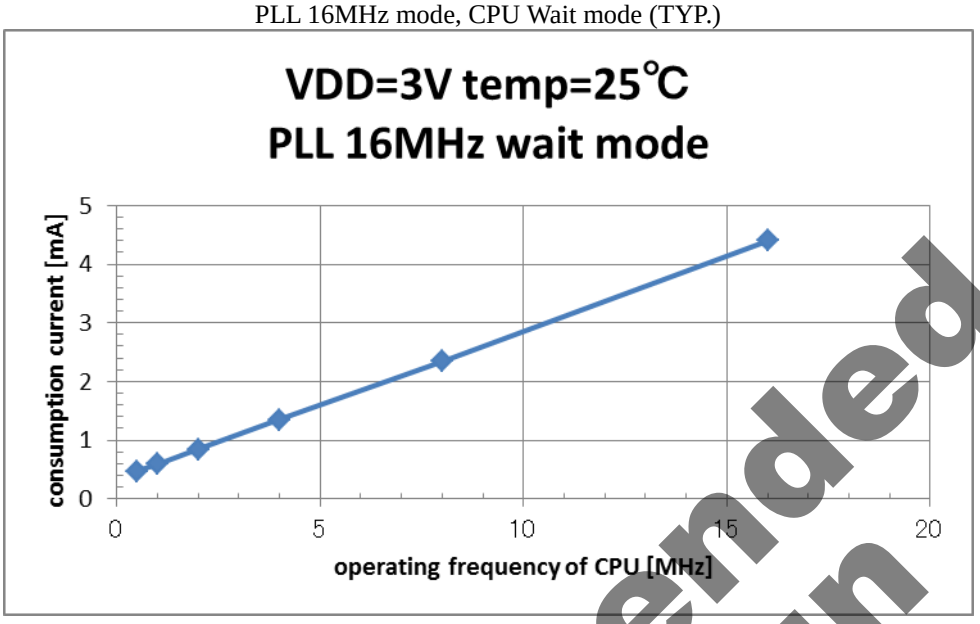


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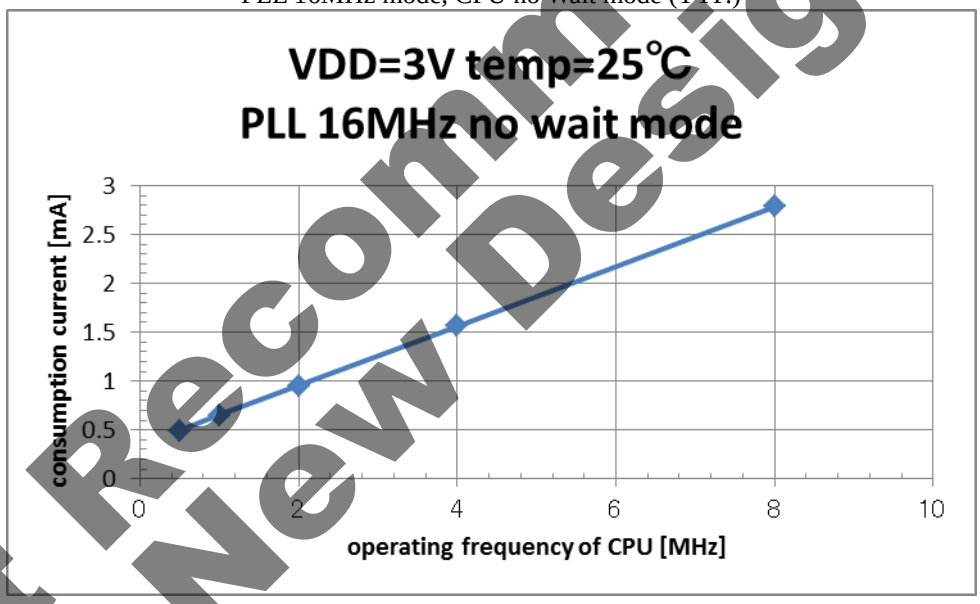
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Current consumption VS operating frequency of CPU

VDD=3V, temp=+25°C, stop the clock supply to peripherals.
PLL 16MHz mode, CPU Wait mode (TYP.)



PLL 16MHz mode, CPU no Wait mode (TYP.)

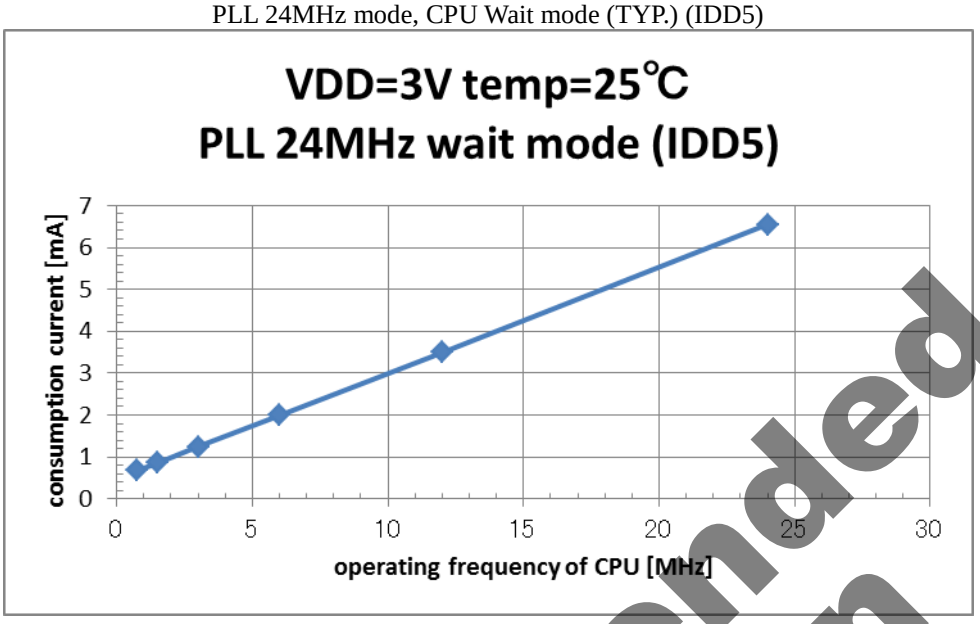


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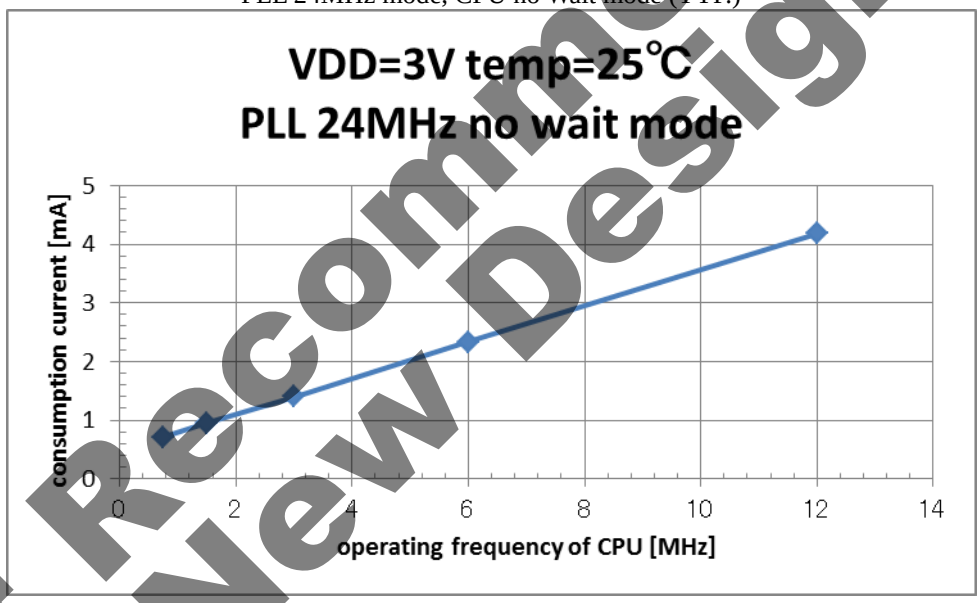
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VDD=3V, temp=+25°C, stop the clock supply to peripherals.

PLL 24MHz mode, CPU Wait mode (TYP.) (IDD5)



PLL 24MHz mode, CPU no Wait mode (TYP.)

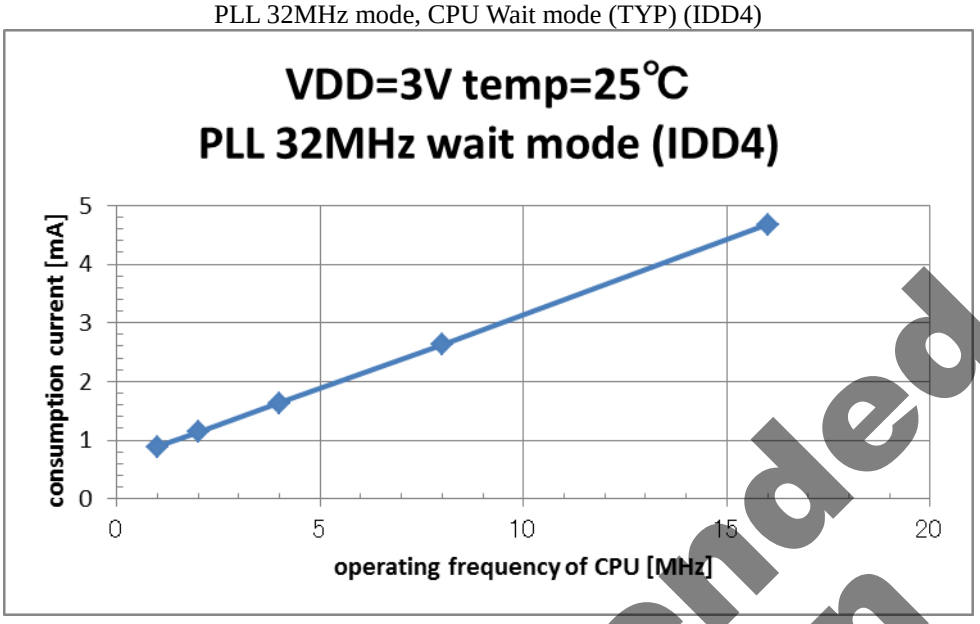


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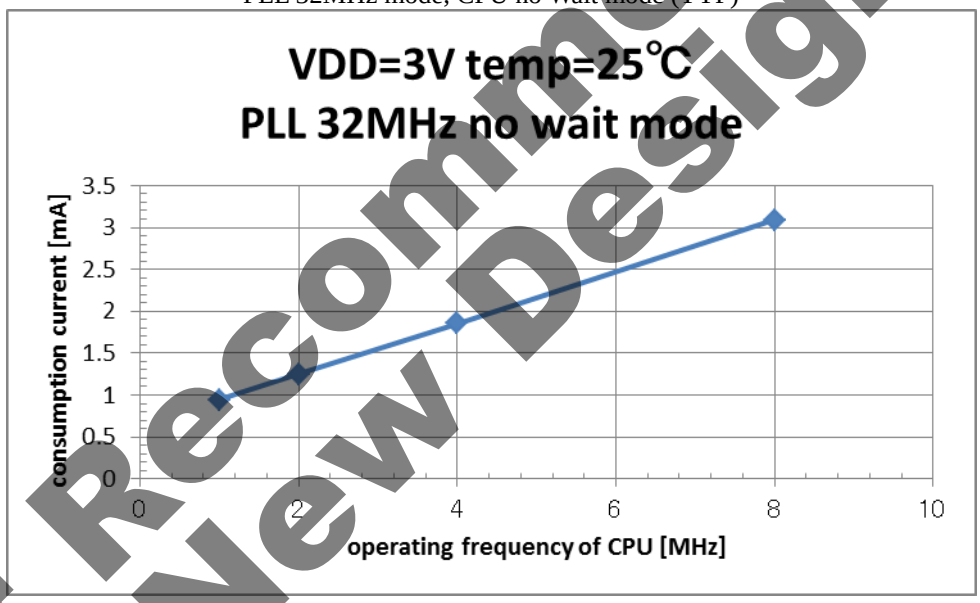
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VDD=3V, temp=+25°C, stop the clock supply to peripherals.

PLL 32MHz mode, CPU Wait mode (TYP) (IDD4)



PLL 32MHz mode, CPU no Wait mode (TYP)

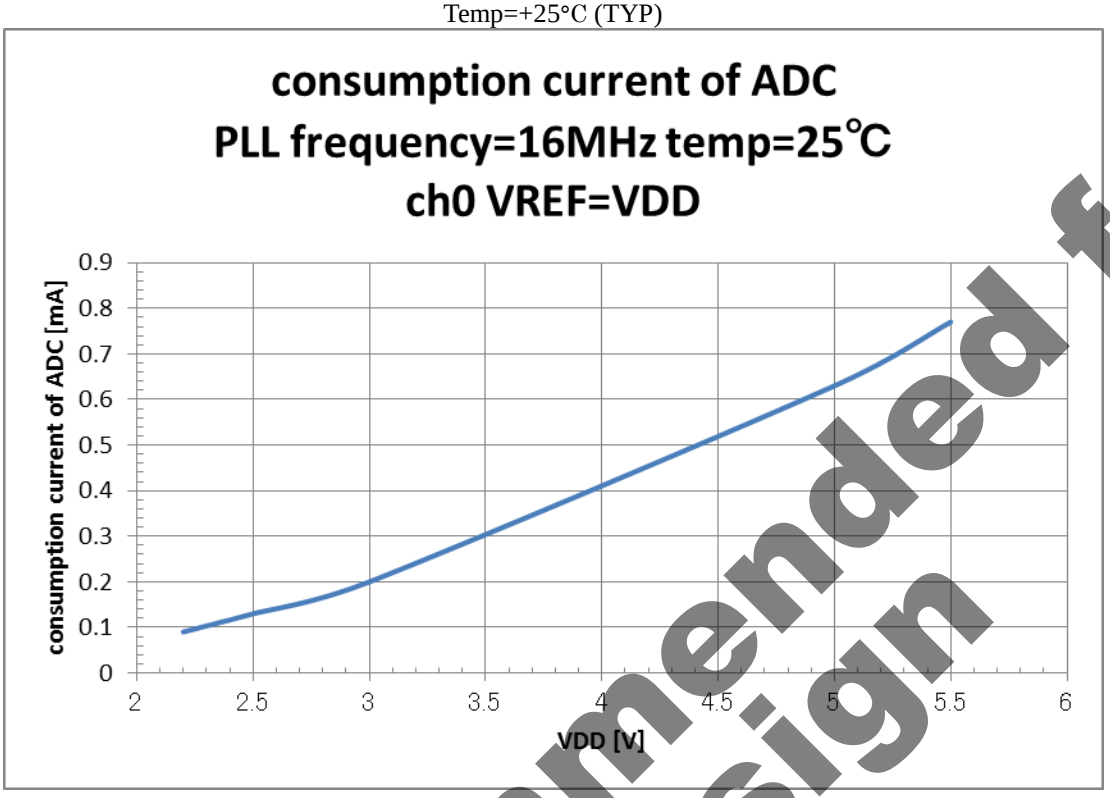


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Consumption current of ADC VS operating voltage

Temp=+25°C (TYP)

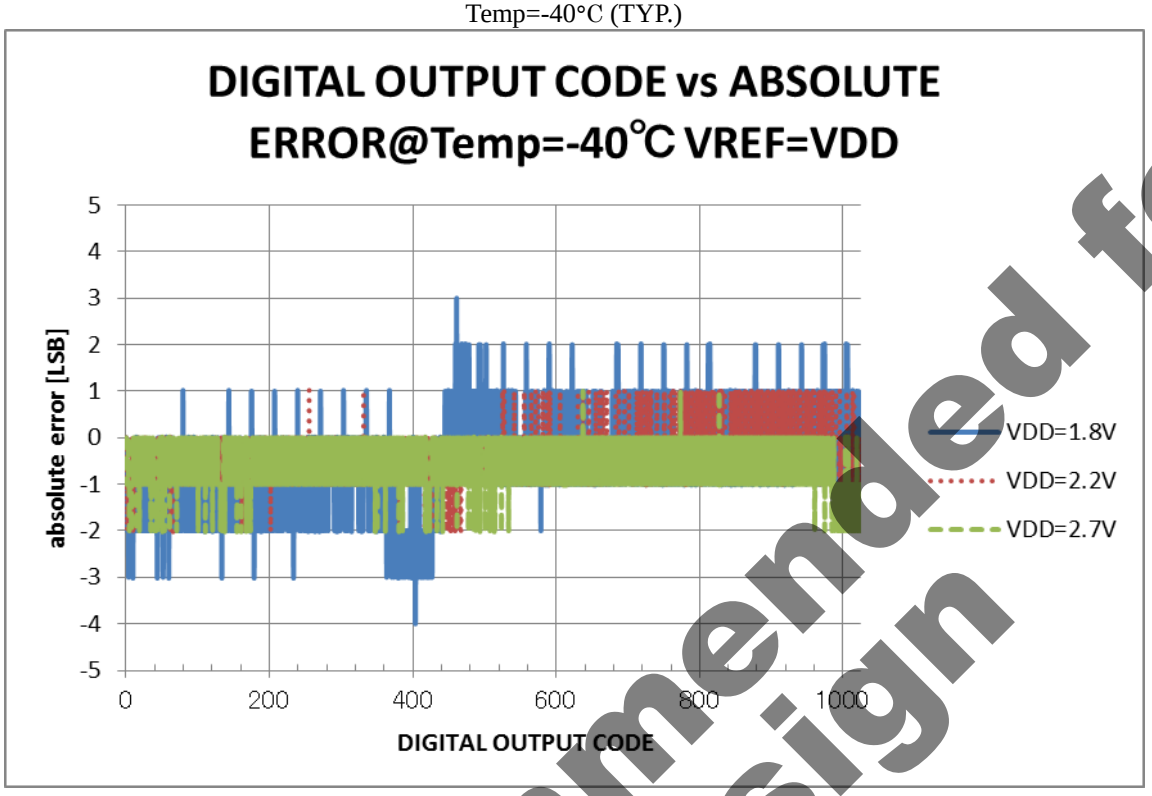


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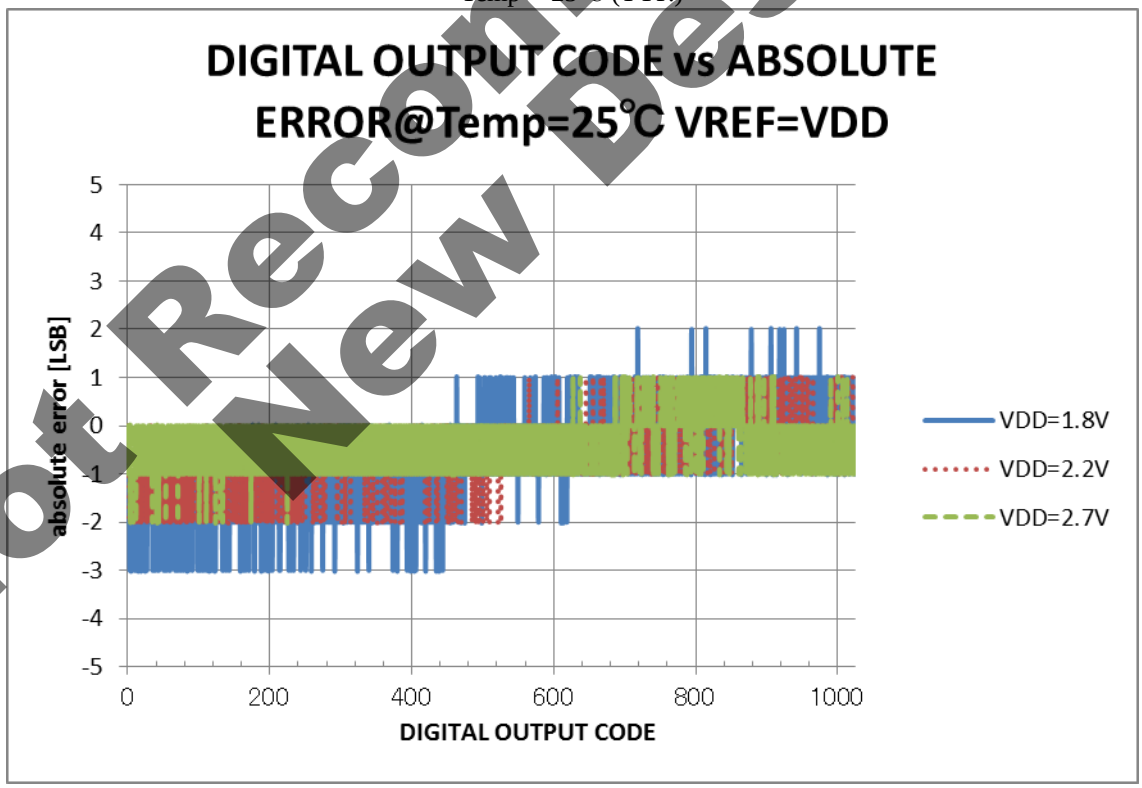
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DIGITAL OUTPUT CODE vs absolute error of ADC

Temp=-40°C (TYP.)



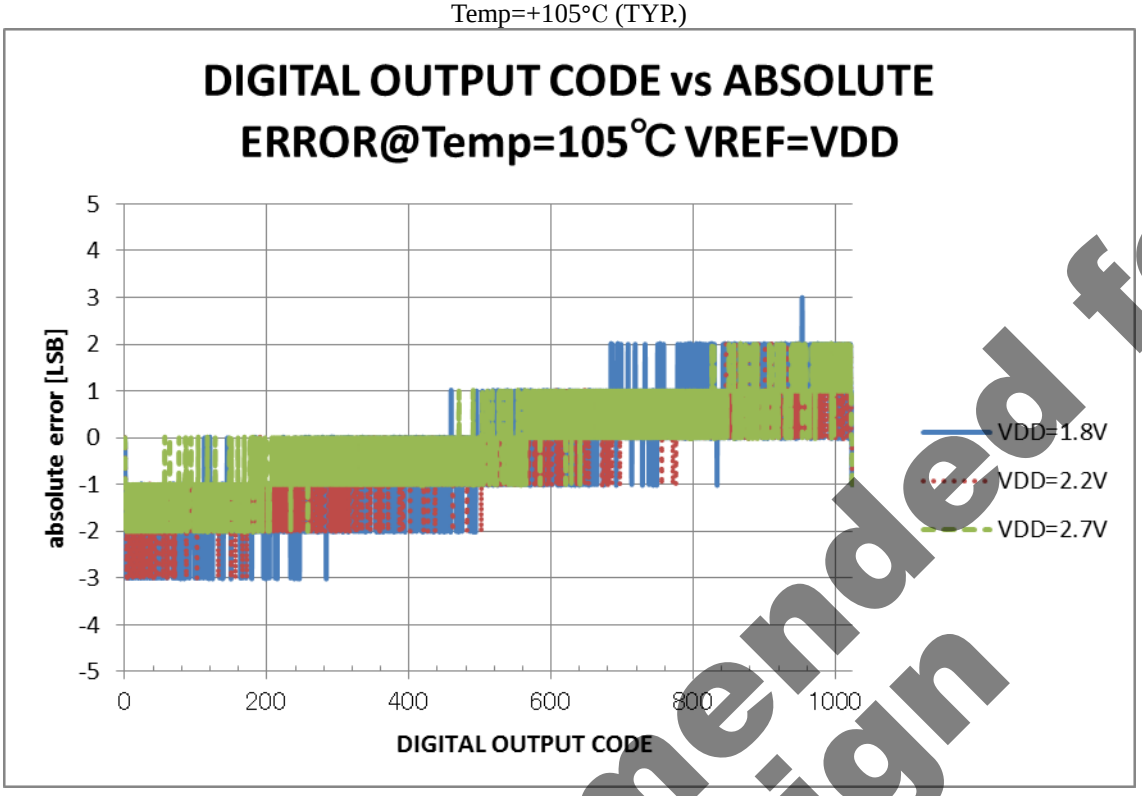
Temp=+25°C (TYP.)



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Temp=+105°C (TYP.)

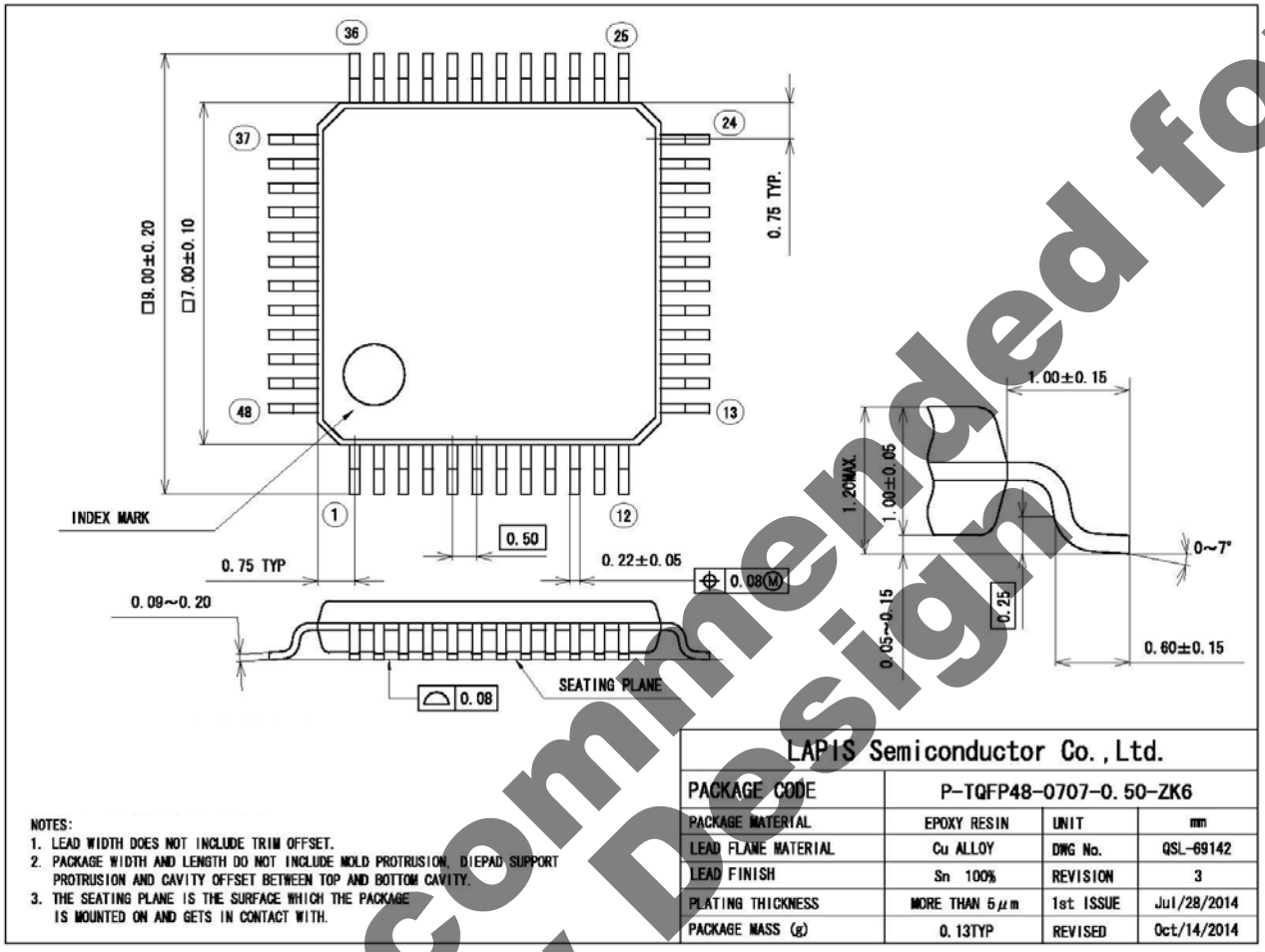


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PACKAGE DIMENSIONS

ML62Q1600/1601/1602 48pin TQFP Package



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	3
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/14/2014

(Unit: mm)

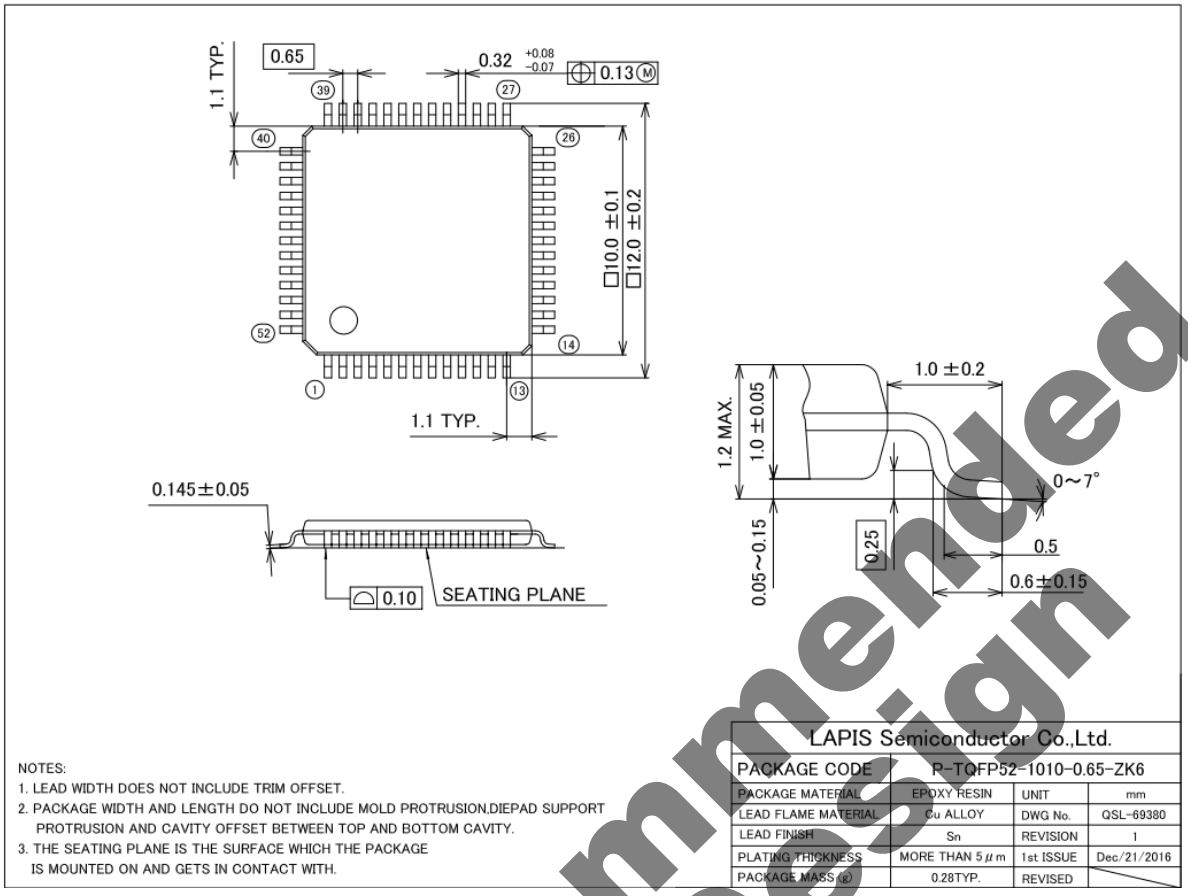
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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ML62Q1610/1611/1622 52pin TQFP Package



(Unit: mm)

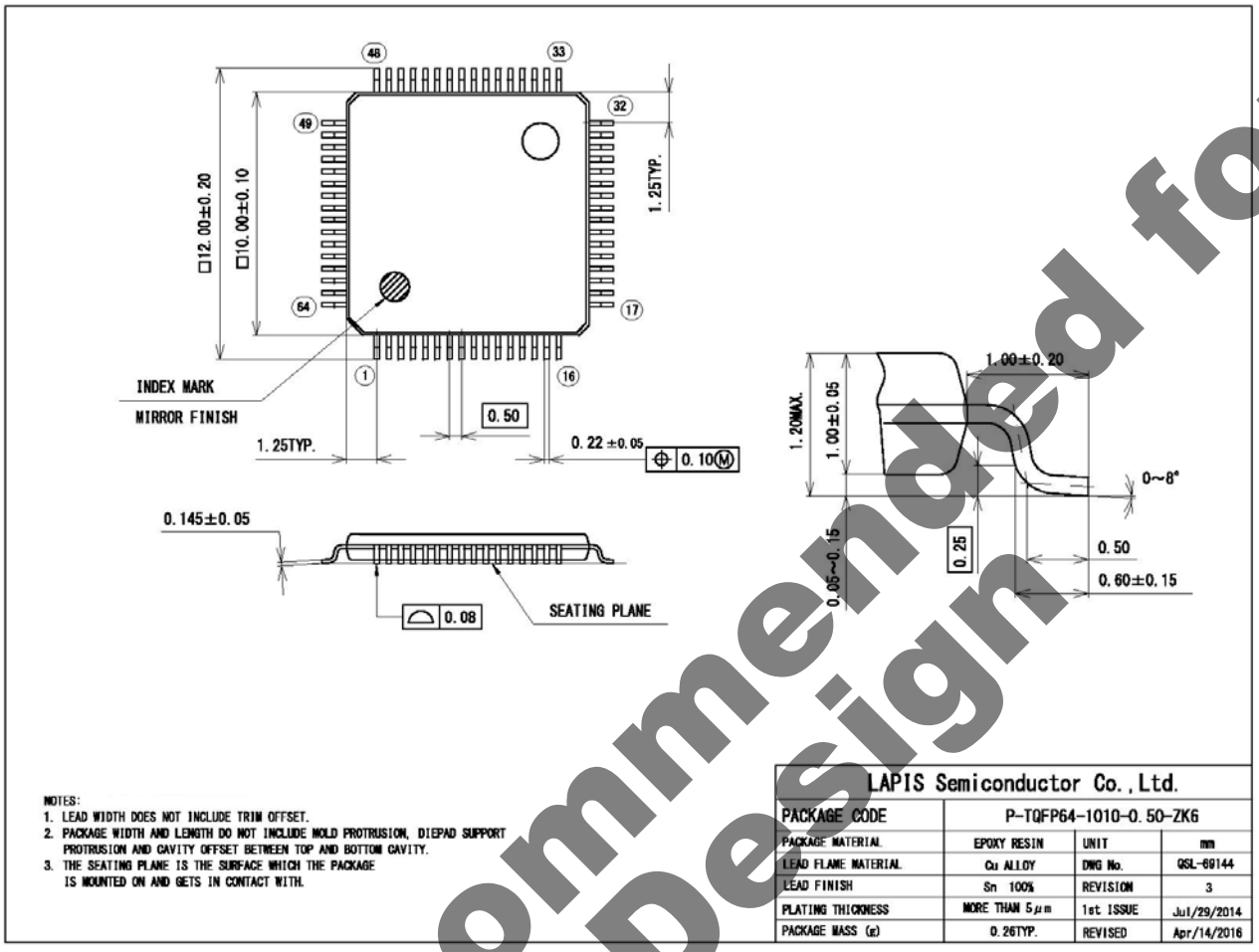
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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ML62Q1620/1621/1622 64pin TQFP Package



(Unit: mm)

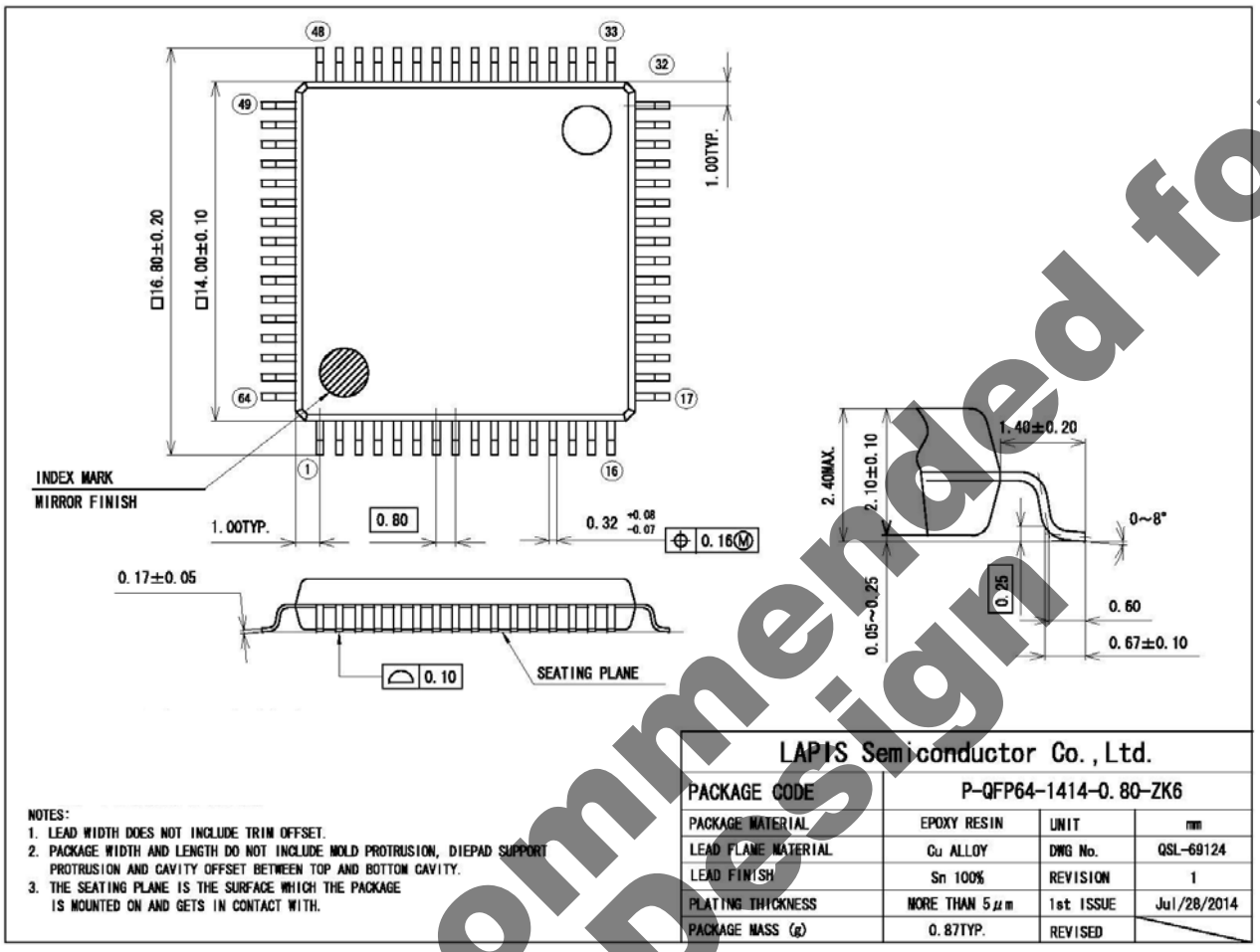
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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ML62Q1620/1621/1622 64pin QFP Package



(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q1600-01	Oct 19, 2017	-	-	Formal 1st Revision.
FEDL62Q1600-02	Nov 1, 2017	3	3	Added description about Simplified RTC.
		28,33,34	28,33,34	Added description about the current.
		33	33	Added IOH1 condition. "VOH≧VDD-0.5"
FEDL62Q1600-04	May 11, 2018	-	-	The 3rd Revision (-03) is skipped to match the revision number to Japanese User's Manual.
		3	3	Added a description about DMA operation mode
		5	5	Corrected the kind of reference voltage for ADC.
		29	29	Added the condition of V_{DD} for IDD4/IDD5.
		30	30	Added the spec of input pulse width (tEXCKW).
		28,32,33	28,32,33	Changed the word "High"/ "Low" level to "H"/"L" level.
		32,33	32,33	Added P00 for IOH1 and IOL3. Changed overall specifications of IOH/IOL and VOH/VOL.
		34	35	Added the pull-up resistance value in the spec of Input current 2 and Input current 3.
		35~39	35~39	Added "n=0~1" in the figures.
		39	40	Changed the spec of $t_{SU:DAT}$ (0.05us → 0.1us) in the 1Mpbs Mode.
		35~39	36~40	Changed the channel number of serial ports : "0" or "1" to "n"
		40	41	• Added minimum value of R_{POR}. • Added the sped of P00 setup/hold time.
		42	43	• Corrected the conditions of Conversion time "2.2V≦V_{DD}≦5.5V" → "2.7V≦V_{DD}≦5.5V" "V_{DD} = 5.0V" → "4.5V≦V_{DD}≦5.0V" • Added a note for the external component of the ADC input.
		42,43	43,44	Seperate the symbol of INL and DNL between ADC and DAC.
		45	46	Added the crystal oscillation circuit to the measuring circuit 1.
		-	48~57	Added the characteristic graghs.
		47	58	Changed the figure for 48pin TQFP package dimension.
		Over all	Over all	Added "+" to the positive temperatures (25 °C , 85 °C , 105 °C → +25 °C , +85 °C , +105 °C).
FEDL62Q1600-05	May 31, 2018	33	33	Added the note "*6 :Nch open drain output mode" for IOL3 and IOL2.

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