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FDPC8014S

April 2014

PowerTrench® Power Clip 25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 3.8 m Ω at V_{GS} = 10 V, I_D = 20 A
- Max $r_{DS(on)} = 4.7 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 18 \text{ A}$

Q2: N-Channel

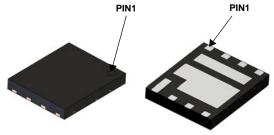
- Max $r_{DS(on)} = 1.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 41 \text{ A}$
- \blacksquare Max $\rm r_{DS(on)}$ = 1.4 m Ω at $\rm V_{GS}$ = 4.5 V, $\rm I_D$ = 37 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

General Description

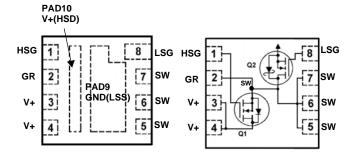
This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFETTM (Q2) have been designed to provide optimal power

Applications

- Computing
- Communications
- General Purpose Point of Load







Pin	Name	ame Description Pin Name Description		Pin	Name	Description		
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		25 ^{Note5}	25	V
V_{GS}	Gate to Source Voltage		±12	±12	V
I _D	Drain Current -Continuous	T _C = 25 °C		110	
I_D	-Continuous	T _A = 25 °C	20 ^{Note1a}	41 ^{Note1b}	Α
	-Pulsed	T _A = 25 °C (Note 4)	75	160	
E _{AS}	Single Pulse Avalanche Energy	(Note 3)	73	253	mJ
D	Power Dissipation for Single Operation	$T_C = 25 ^{\circ}C$		42	W
P_{D}	Power Dissipation for Single Operation	T _A = 25 °C	2.1 ^{Note1a}	2.3 Note1b	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to	+150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.0	3.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD/16OD	FDPC8014S	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Chara	octeristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	Q1	25			V
D V DSS	Diaili to Source Breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	Q2	25			V
ΔBV_{DSS}	Breakdown Voltage Temperature	$I_D = 250 \mu A$, referenced to 25 °C	Q1		24		mV/°C
ΔT_{J}	Coefficient	I_D = 10 mA, referenced to 25 °C	Q2		24		IIIV/ C
	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V	Q1			1	μΑ
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	Q2			500	μА
	Gate to Source Leakage Current,	V _{GS} = 12 V/-8 V, V _{DS} = 0 V	Q1			±100	nA
IGSS	Forward	$V_{GS} = 12 \text{ V/-8 V}, V_{DS} = 0 \text{ V}$	Q2			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$ $V_{GS} = V_{DS}, I_D = 1 mA$	Q1 Q2	0.8 1.1	1.3 1.4	2.5 2.5	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-4 -3		mV/°C	
	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 20 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 18 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125 \text{ °C}$	Q1		2.8 3.4 3.9	3.8 4.7 5.3		
r _{DS(on)}	Diam to Source On Resistance	$V_{GS} = 10V$, $I_D = 41$ A $V_{GS} = 4.5$ V, $I_D = 37$ A $V_{GS} = 10$ V, $I_D = 41$ A , $I_J = 125$ °C	Q2		0.9 1.0 1.1	1.2 1.4 1.5	mΩ	
9 _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 20 \text{ A}$ $V_{DS} = 5 \text{ V}, I_{D} = 41 \text{ A}$	Q1 Q2		182 315		S	

Dynamic Characteristics

•							
C	Input Capacitance		Q1		1695	2375	pF
C _{iss}	при Сараспансе	Q1:	Q2		6580	9870	ρı
C	Output Capacitance	$V_{DS} = 13 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1		495	710	pF
C _{oss}	Output Capacitance	Q2:	Q2		1720	2580	ρı
C	Reverse Transfer Capacitance	$V_{DS} = 13 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1		54	100	nΕ
C _{rss}	Reverse Transfer Capacitance	105 10 1, 165 0 1, 1 11111	Q2		204	370	pF
D	Gate Resistance		Q1	0.1	0.4	1.2	Ω
R_g	Gale Resistance		Q2	0.1	0.4	1.2	5.2

Switching Characteristics

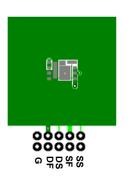
t _{d(on)}	Turn-On Delay Time			Q1 Q2	8 16	16 28	ns
t _r	Rise Time		Q1: $V_{DD} = 13 \text{ V}, I_{D} = 20 \text{ A}, R_{GEN} = 6 \Omega$ Q2: $V_{DD} = 13 \text{ V}, I_{D} = 41 \text{ A}, R_{GEN} = 6 \Omega$		2 6	10 11	ns
t _{d(off)}	Turn-Off Delay Time	Q2:			24 47	38 75	ns
t _f	Fall Time				2 4	10 10	ns
Qg	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1	Q1 Q2	25 93	35 130	nC
Qg	Total Gate Charge	V _{GS} = 0 V to 4.5 V		Q1 Q2	11 43	16 60	nC
Q _{gs}	Gate to Source Gate Charge		$Q2 V_{DD} = 13 \text{ V, I}_{D}$	Q1 Q2	3.4 13		nC
Q _{gd}	Gate to Drain "Miller" Charge		= 41 A	Q1 Q2	2.2 8.5		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

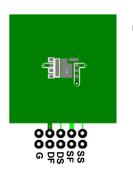
Symbol Parameter		Test Conditions	Type	Min	Тур	Max	Units			
Drain-Source Diode Characteristics										
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 20 \text{ A}$ (Note 2) $V_{GS} = 0 \text{ V}, I_S = 41 \text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V			
I _S	Diode continuous forward current	T _C = 25 °C	Q1 Q2		60 110		Α			
I _{S,Pulse}	Diode pulse current	1 _C = 23 C	Q1 Q2		75 160		Α			
t _{rr}	Reverse Recovery Time	Q1 I _F = 20 A, di/dt = 100 A/μs	Q1 Q2		25 36	40 58	ns			
Q _{rr}	Reverse Recovery Charge	Q2 $I_F = 41 \text{ A, di/dt} = 300 \text{ A/}\mu\text{s}$	Q1 Q2		10 47	20 75	nC			

Notes

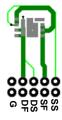
 $1.R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



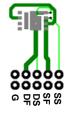
a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 130 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

- 2 Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0%.
- 3. Q1 : E_{AS} of 73 mJ is based on starting T_J = 25 $^{\rm o}$ C; N-ch: L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 24 A. Q2: E_{AS} of 253 mJ is based on starting T_J = 25 $^{\rm o}$ C; N-ch: L = 3 mH, I_{AS} = 13 A, V_{DD} = 25 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 43 A.
- 4. Pulsed Id limited by junction temperature,td<=10 us. Please refer to SOA curve for more details.
- 5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

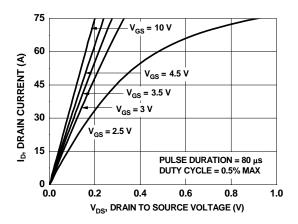


Figure 1. On Region Characteristics

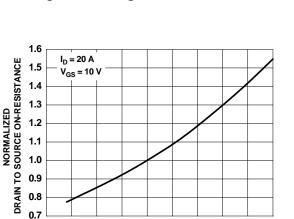


Figure 3. Normalized On Resistance vs. Junction Temperature

75

100 125 150

-50

-25 0 25 50 T_J, JUNCTION TEMPERATURE (°C)

-75

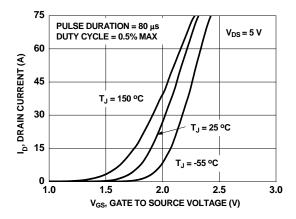


Figure 5. Transfer Characteristics

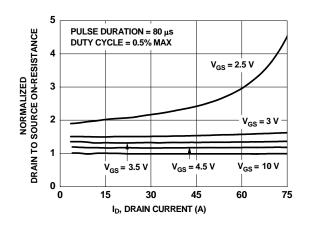


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

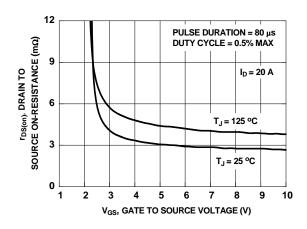


Figure 4. On-Resistance vs. Gate to Source Voltage

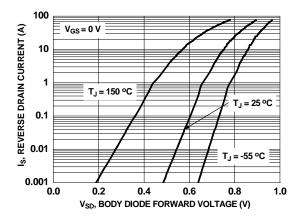


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

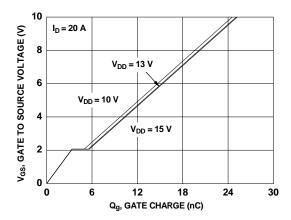


Figure 7. Gate Charge Characteristics

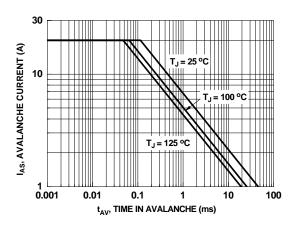


Figure 9. Unclamped Inductive Switching Capability

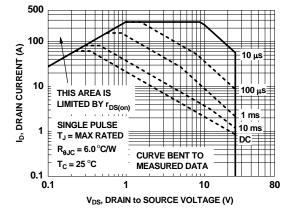


Figure 11. Forward Bias Safe Operating Area

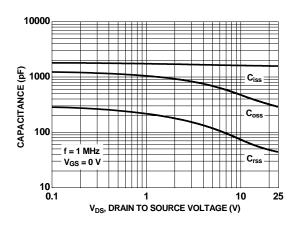


Figure 8. Capacitance vs. Drain to Source Voltage

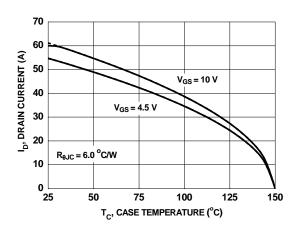


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

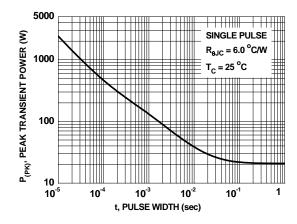


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25$ °C unless otherwise noted

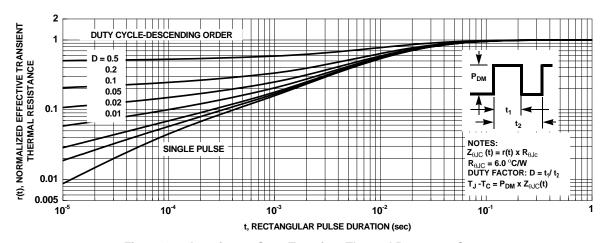


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

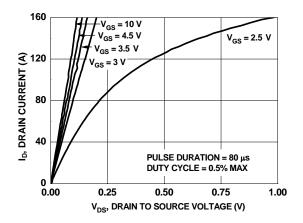


Figure 14. On- Region Characteristics

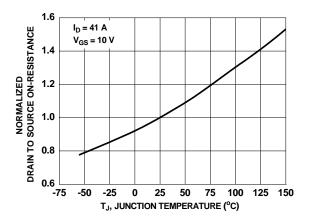


Figure 16. Normalized On-Resistance vs. Junction Temperature

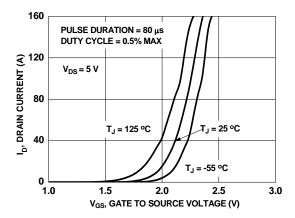


Figure 18. Transfer Characteristics

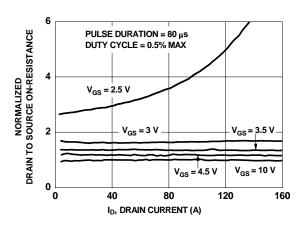


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

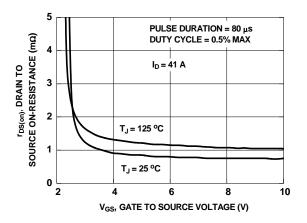


Figure 17. On-Resistance vs. Gate to Source Voltage

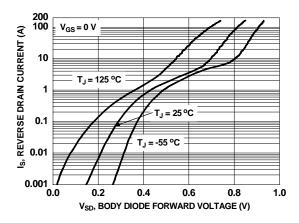


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

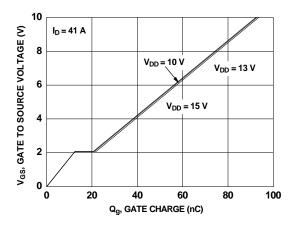


Figure 20. Gate Charge Characteristics

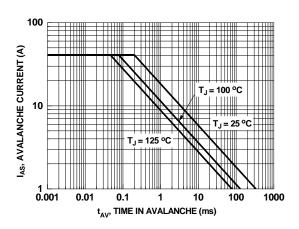


Figure 22. Unclamped Inductive Switching Capability

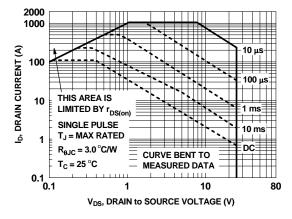


Figure 24. Forward Bias Safe Operating Area

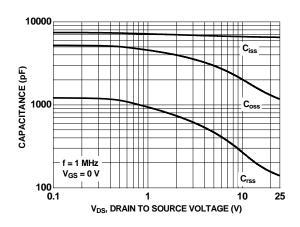


Figure 21. Capacitance vs. Drain to Source Voltage

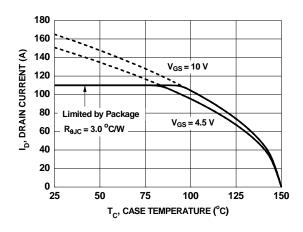


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

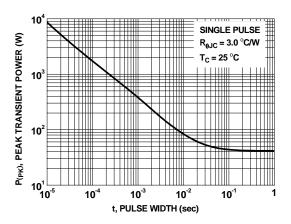


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25$ °C unless otherwise noted

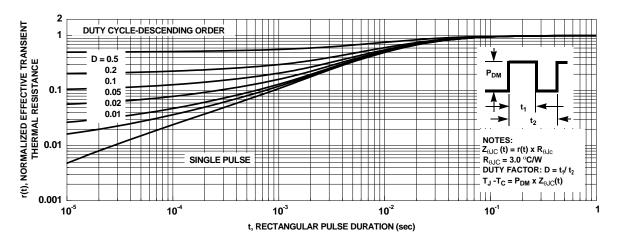


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFETTM Schottky body diode Characteristics

Fairchild's SyncFETTM process embeds a Schottky diode in parallel with PowerTrench[®] MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverses recovery characteristic of the FDPC8014S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

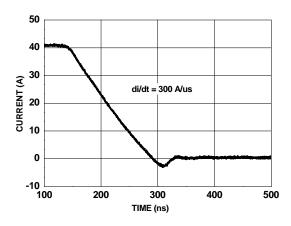


Figure 27. FDPC8014S SyncFETTM Body Diode Reverse Recovery Characteristic

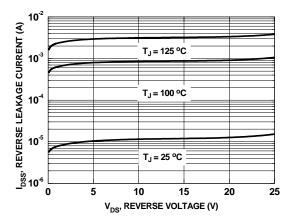
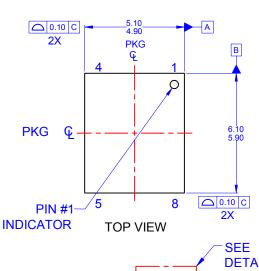
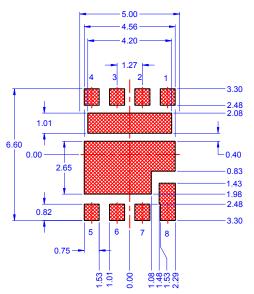
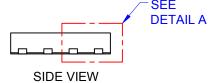


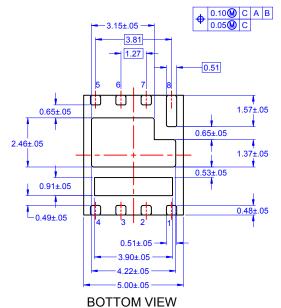
Figure 28. SyncFETTM Body Diode Reverse Leakage vs. Drain-source Voltage





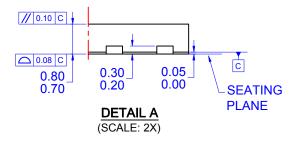


RECOMMENDED LAND PATTERN



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08KREV2



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