

Quad Precision Operational Amplifier

DESCRIPTION

The **RH1014M** is the first precision quad operational amplifier which directly upgrades designs in the industry standard 8-pin DIP LM124/LM148/OP-11/5156 pin configuration. Low offset voltage (300 μ V max), low drift ($\leq 2.5\mu$ V/ $^{\circ}$ C), low offset current (≤ 1.5 nA), and high gain (1.2 million min) combine to make the RH1014M four truly precision amplifiers in one package.

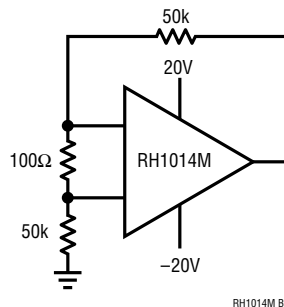
The wafer lots are processed to Analog Devices' in-house Class S flow to yield circuits usable in stringent military applications.

ABSOLUTE MAXIMUM RATINGS

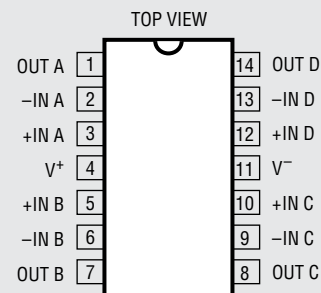
Supply Voltage	± 22 V
Differential Input Voltage	± 30 V
Input Voltage	Equal to Positive Supply Voltage
.....	5V Below Negative Supply Voltage
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	-55° C to 125° C
Storage Temperature Range	-65° C to 150° C
Lead Temperature (Soldering, 10 sec).....	300° C

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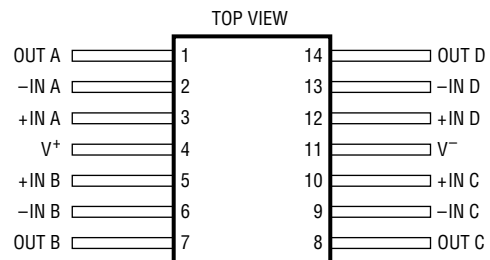
BURN-IN CIRCUIT



PACKAGE INFORMATION



J PACKAGE
14-LEAD CERAMIC DIP
OBSOLETE PACKAGE
For Reference Only



W PACKAGE
14-LEAD FLATPAK GLASS SEALED

TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ C$			SUB-GROUP	$-55^\circ C \leq T_A \leq 125^\circ C$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage					300	1			550	2,3	μV
			2			450	1			750	3	μV
		$V_{CM} = 0.1V$	2							750	2	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage		1							2.5		$\mu V/^\circ C$
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability					0.5						$\mu V/Mo$
I_{OS}	Input Offset Current					10	1			20	2,3	nA
			2			10	1			20	2,3	nA
I_B	Input Bias Current					30	1			45	2,3	nA
			2			50	1			120	2,3	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz				0.55						μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10Hz$				24						$nV/\sqrt{Hz}$
		$f_0 = 1000Hz$				22						$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz$				0.07						$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential	1			70						$M\Omega$
		Common Mode				4						$G\Omega$
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2k$				1.2	4	0.25			5,6	$V/\mu V$
		$V_O = \pm 10V$, $R_L \geq 600\Omega$				0.5	4					$V/\mu V$
		$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	2			1						$V/\mu V$
	Input Voltage Range		1			13.5						V
			1			-15.0						V
			1,2			3.5						V
			1,2			0						V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13.5V$, $-15V$				97	1					dB
		$V_{CM} = 13V$, $-14.9V$						94			2,3	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$				100	1	97			2,3	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$				120	1					dB
V_{OUT}	Output Voltage Swing	$R_L \geq 2k$				± 12.5	4	± 11.5			5,6	V
		Output Low, No Load	2			25	4					mV
		Output Low, 600Ω to GND	2			10	4			18	5,6	mV
		Output Low, $I_{SINK} = 1mA$	2			350	4					mV
		Output High, No Load	2			4.0	4					V
		Output High, 600Ω to GND	2			3.4	4	3.1			5,6	V
SR	Slew Rate					0.2	4					$V/\mu s$
I_S	Supply Current	Per Amplifier				0.55	1			0.70	2,3	mA
			2			0.50	1			0.65	2,3	mA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 3) $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si) MIN	10KRAD (Si) MAX	20KRAD (Si) MIN	20KRAD (Si) MAX	50KRAD (Si) MIN	50KRAD (Si) MAX	100KRAD (Si) MIN	100KRAD (Si) MAX	200KRAD (Si) MIN	200KRAD (Si) MAX	UNITS
V_{OS}	Input Offset Voltage				450		450		600		750		900	μV
			2		600		600		750		900			μV
I_{OS}	Input Offset Current				10		10		15		20		25	nA
			2		10		10		15		20			nA
I_B	Input Bias Current				60		75		100		175		250	nA
			2		80		100		125		200			nA
	Input Voltage Range		1		13.5		13.5		13.5		13.5		13.5	V
			1		-15.0		-15.0		-15.0		-15.0		-15.0	V
			2		3.5		3.5		3.5		3.5			V
			2		0		0		0		0			V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$			97		97		94		90		86	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$			100		98		94		86		80	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 10k$, $V_O = \pm 10V$			500		200		100		50		25	V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k$			± 12.5		± 12.5		± 12.5		± 12.5		± 12.5	V
		Output Low, No Load	2		25		30		40		50			mV
		Output Low, 600Ω to GND	2		10		10		10		10			mV
		Output Low, $I_{SINK} = 1mA$	2		0.6		0.8		1.0		1.6			V
		Output High, No Load	2		4.0		4.0		4.0		4.0			V
		Output High, 600Ω to GND	2		3.4		3.2		3.0		2.8			V
SR	Slew Rate	$R_L \geq 10k$			0.13		0.12		0.11		0.07		0.01	V/ μs
I_S	Supply Current	Per Amplifier			0.55		0.55		0.55		0.55		0.55	mA
			2		0.50		0.50		0.50		0.50			mA

Note 1: Guaranteed by design, characterization, or correlation to other tested parameters.**Note 2:** Specification applies for $V_{S+} = 5V$, $V_{S-} = 0V$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$.**Note 3:** Device is characterized at 10KRAD, 20KRAD, 50KRAD, 100KRAD and 200KRAD, but is production tested at 100KRAD only.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-PRF-38535 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Group C End Point Electrical Parameters	1, 2, 3
Group D End Point Electrical Parameters	1, 2, 3
Group E End Point Electrical Parameters	1

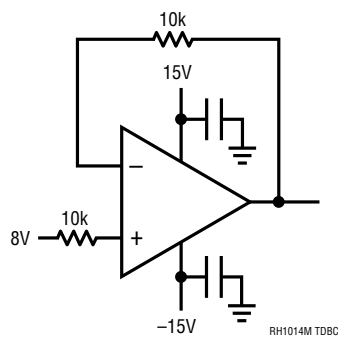
* PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

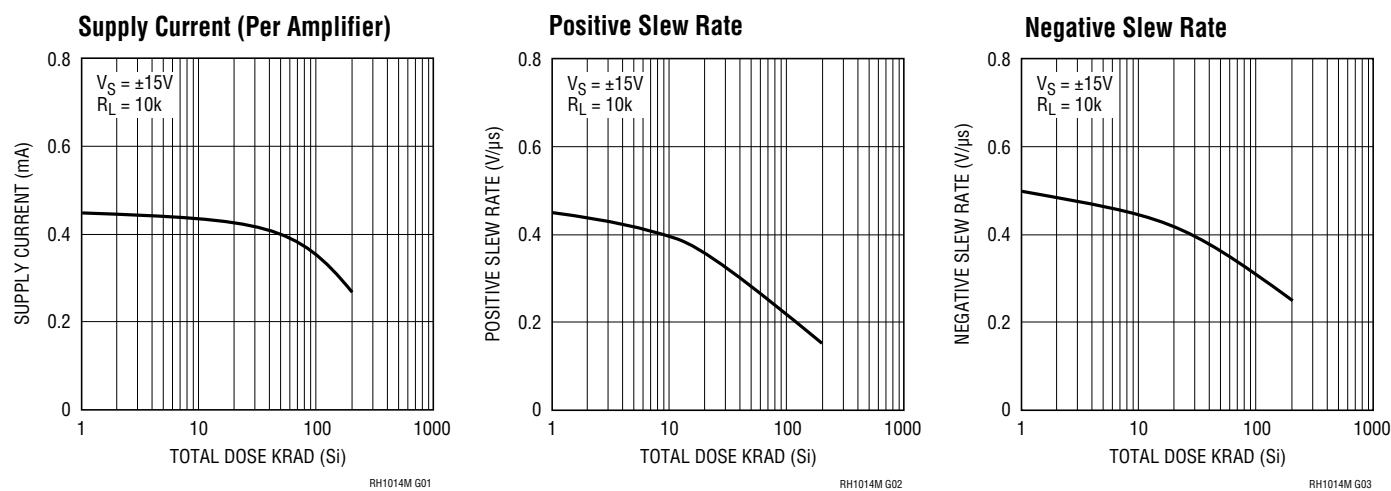
The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Analog Devices, Inc., reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

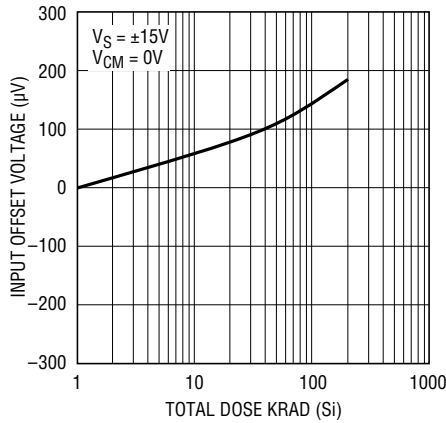


TYPICAL PERFORMANCE CHARACTERISTICS



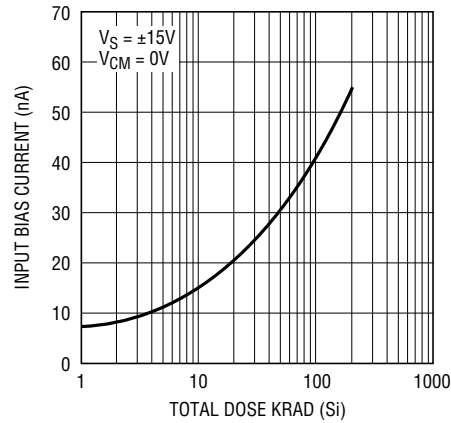
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



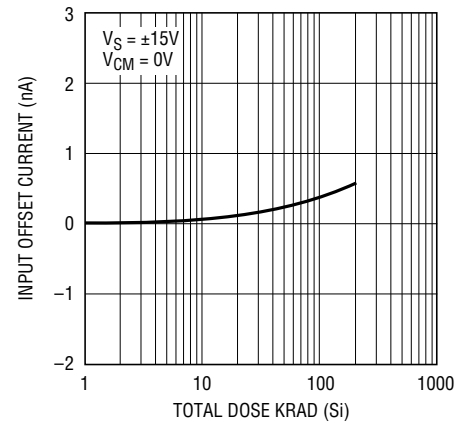
RH1014M G04

Input Bias Current



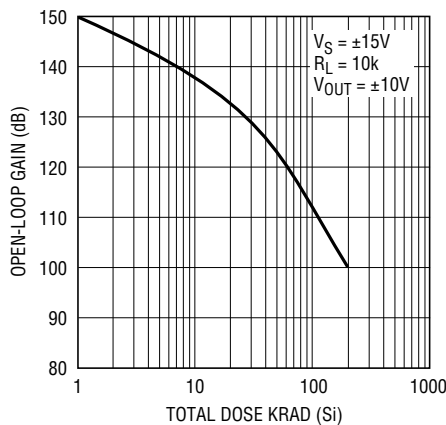
RH1014M G05

Input Offset Current



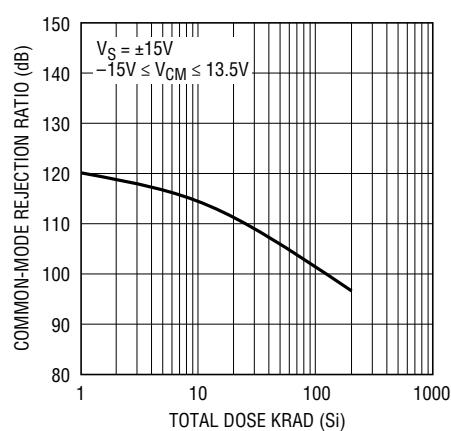
RH1014M G06

Open-Loop Gain



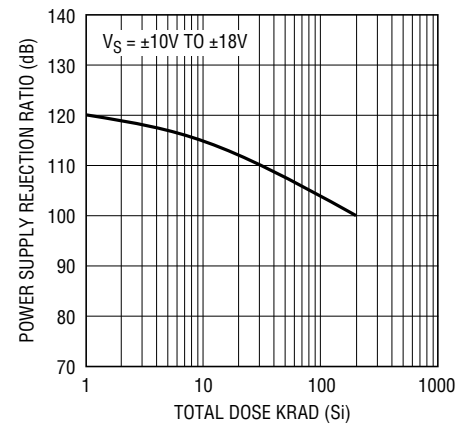
RH1014M G07

Common-Mode Rejection Ratio



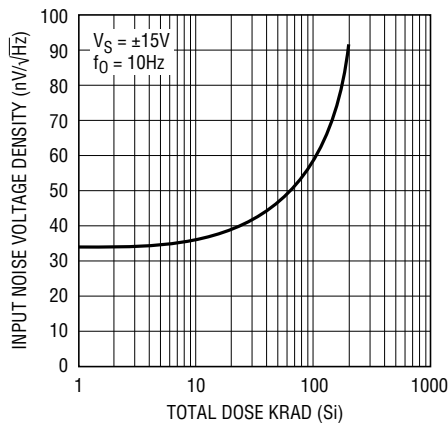
RH1014M G08

Power Supply Rejection Ratio



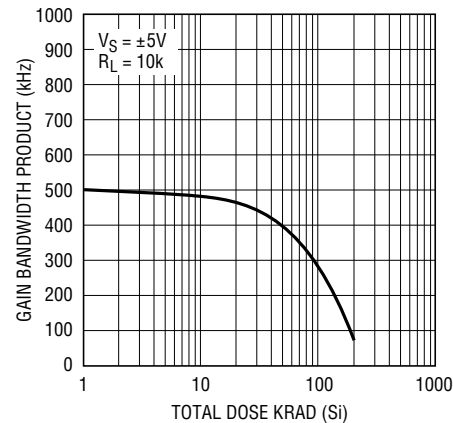
RH1014M G09

Input Noise Voltage Density



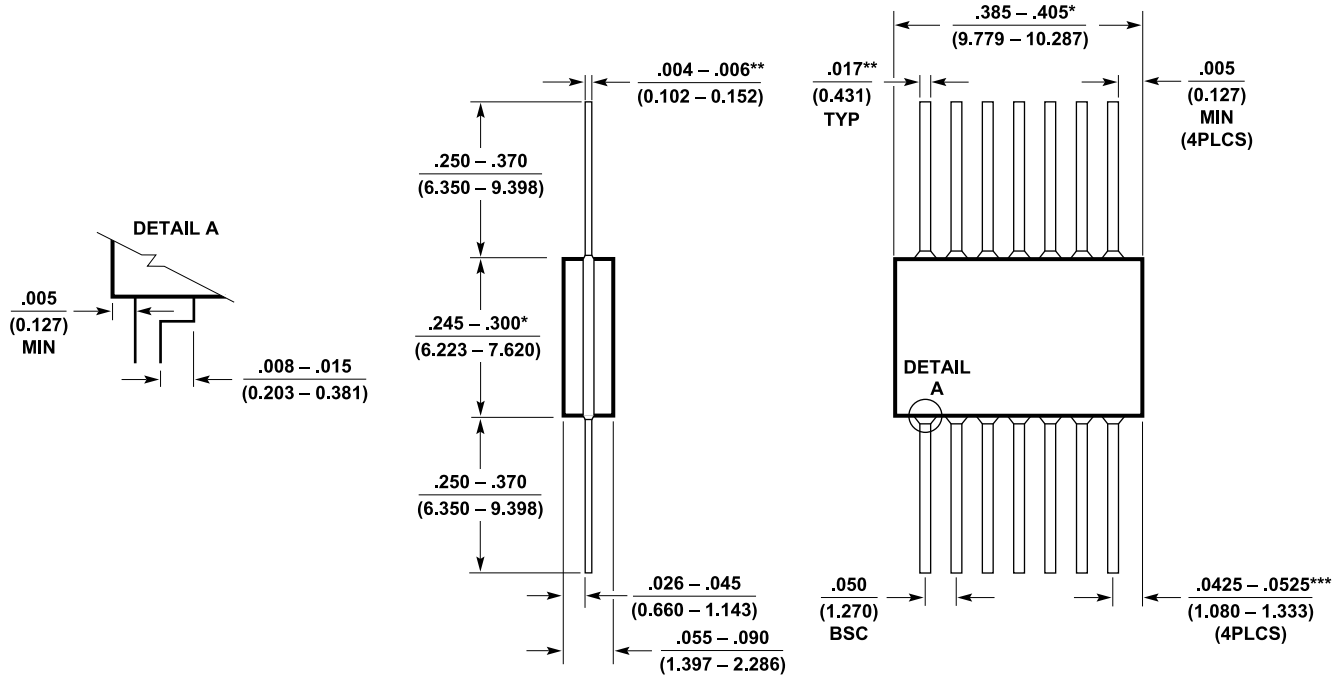
RH1014M G10

Gain Bandwidth Product



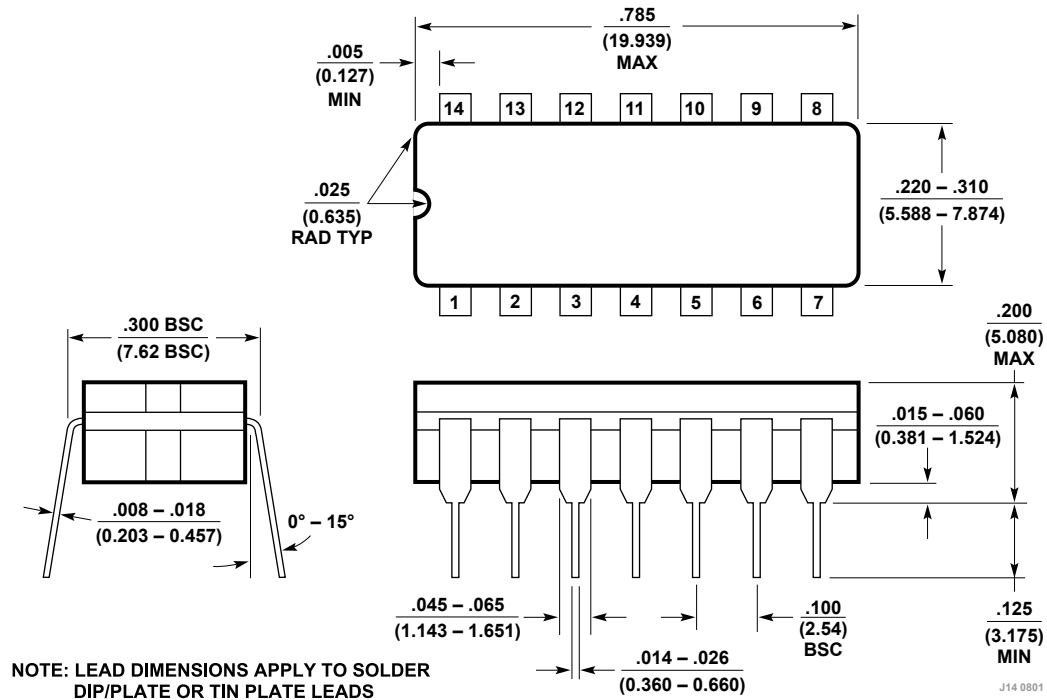
RH1014M G11

PACKAGE OUTLINE DRAWINGS



J Package
14-Lead Cerdip (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)
Dimensions shown in inches and (millimeters)

PACKAGE OUTLINE DRAWINGS



W Package
14-Lead Flatpak Glass Sealed (Hermetic)
(Reference LTC DWG # 05-08-1140 Rev A)
Dimensions shown in inches and (millimeters)

REVISION HISTORY (Revision history begins at Rev H)

REV	DATE	DESCRIPTION	PAGE NUMBER
H	03/19	Obsoleting J package and updating to ADI format	All Pages
I	08/24	Changes to Table 2: Electrical Test Requirements	4
J	07/25	Changes to Table 1A: Electrical Characteristics Added Package Outline Drawings	3 6, 7