

# MC100LVEL51

## 3.3 V ECL Differential Clock D Flip-Flop

### Description

The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V  $V_{CC}$ .

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to  $V_{EE}$  and the  $\overline{CLK}$  input will be biased at  $V_{CC}/2$ .

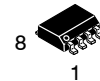
### Features

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: > 4 kV Human Body Model, > 200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-3.8\text{ V}$
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level
  - ◆ Level 1 for SOIC-8 NB
  - ◆ Level 3 for TSSOP-8
  - ◆ Level 1 for DFN-8
  - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 114 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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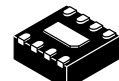
[www.onsemi.com](http://www.onsemi.com)



SOIC-8 NB  
D SUFFIX  
CASE 751

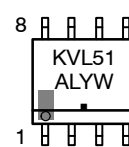


TSSOP-8  
DT SUFFIX  
CASE 948R

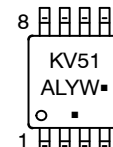


DFN-8  
MN SUFFIX  
CASE 506AA

### MARKING DIAGRAMS\*



SOIC-8



TSSOP-8



DFN-8

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
■ = Pb-Free Package

(Note: Microdot may be in either location)

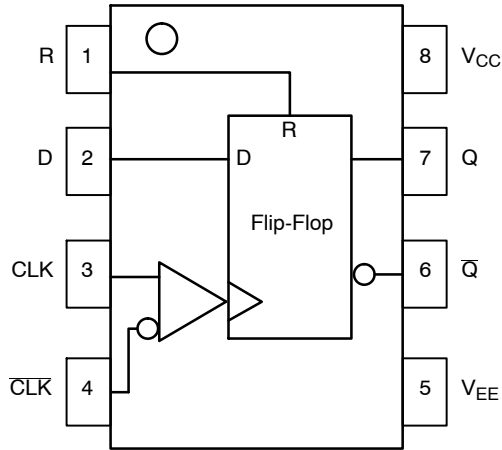
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device           | Package                | Shipping†        |
|------------------|------------------------|------------------|
| MC100LVEL51DG    | SOIC-8 NB<br>(Pb-Free) | 98 Units/Tube    |
| MC100LVEL51DR2G  | SOIC-8 NB<br>(Pb-Free) | 2500/Tape & Reel |
| MC100LVEL51DTG   | TSSOP-8<br>(Pb-Free)   | 100 Units/Tube   |
| MC100LVEL51DTR2G | TSSOP-8<br>(Pb-Free)   | 2500/Tape & Reel |
| MC100LVEL51MNR4G | DFN-8<br>(Pb-Free)     | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LVEL51



**Figure 1. Logic Diagram and Pinout Assignment**

**Table 1. PIN DESCRIPTION**

| PIN                          | FUNCTION                                                                                                                                                                       |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Differential Clock Input                                                                                                                                                   |
| Q, $\overline{\text{Q}}$     | ECL Differential Output                                                                                                                                                        |
| D                            | ECL D Input                                                                                                                                                                    |
| R                            | ECL Reset Input                                                                                                                                                                |
| V <sub>CC</sub>              | Positive Supply                                                                                                                                                                |
| V <sub>EE</sub>              | Negative Supply                                                                                                                                                                |
| EP                           | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

**Table 2. TRUTH TABLE**

| D | R | CLK | Q |
|---|---|-----|---|
| L | L | Z   | L |
| H | L | Z   | H |
| X | H | X   | L |

Z = LOW to HIGH Transition

X = Don't Care

# MC100LVEL51

**Table 3. MAXIMUM RATINGS**

| Symbol        | Parameter                                          | Condition 1                                    | Condition 2                            | Rating            | Unit |
|---------------|----------------------------------------------------|------------------------------------------------|----------------------------------------|-------------------|------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |                                        | 8 to 0            | V    |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0\text{ V}$                          |                                        | -8 to 0           | V    |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>-6 to 0 | V    |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |                                        | 50<br>100         | mA   |
| $T_A$         | Operating Temperature Range                        |                                                |                                        | -40 to +85        | °C   |
| $T_{stg}$     | Storage Temperature Range                          |                                                |                                        | -65 to +150       | °C   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8 NB                              | 190<br>130        | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8 NB                              | 41 to 44 ± 5%     | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8                                | 185<br>140        | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8                                | 41 to 44 ± 5%     | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | DFN-8                                  | 129<br>84         | °C/W |
| $T_{sol}$     | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260°C                           |                                        | 265               | °C   |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | (Note 1)                                       | DFN-8                                  | 35 to 40          | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 4. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3 \text{ V}$ ;  $V_{EE} = 0.0 \text{ V}$  (Note 1))

| Symbol      | Characteristic                                                                                                            | -40°C       |      |            | 25°C        |      |            | 85°C        |      |            | Unit          |
|-------------|---------------------------------------------------------------------------------------------------------------------------|-------------|------|------------|-------------|------|------------|-------------|------|------------|---------------|
|             |                                                                                                                           | Min         | Typ  | Max        | Min         | Typ  | Max        | Min         | Typ  | Max        |               |
| $I_{EE}$    | Power Supply Current                                                                                                      |             | 30   | 35         |             | 30   | 35         |             | 32   | 37         | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)                                                                                              | 2215        | 2295 | 2420       | 2275        | 2345 | 2420       | 2275        | 2345 | 2420       | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)                                                                                               | 1470        | 1605 | 1745       | 1490        | 1595 | 1680       | 1490        | 1595 | 1680       | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                                                                         | 2135        |      | 2420       | 2135        |      | 2420       | 2135        |      | 2420       | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                                                                          | 1490        |      | 1825       | 1490        |      | 1825       | 1490        |      | 1825       | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{PP} < 500 \text{ mV}$<br>$V_{PP} \geq 500 \text{ mV}$ | 1.2<br>1.4  |      | 3.0<br>3.0 | 1.1<br>1.3  |      | 3.0<br>3.0 | 1.1<br>1.3  |      | 3.0<br>3.0 | V             |
| $I_{IH}$    | Input HIGH Current                                                                                                        |             |      | 150        |             |      | 150        |             |      | 150        | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Others<br>CLK                                                                                        | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3 \text{ V}$ .
2. Outputs are terminated through a  $50 \Omega$  resistor to  $V_{CC} - 2.0 \text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1 \text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0 \text{ V}$ ;  $V_{EE} = -3.3 \text{ V}$  (Note 1))

| Symbol      | Characteristic                                                                                                            | -40°C        |       |              | 25°C         |       |              | 85°C         |       |              | Unit          |
|-------------|---------------------------------------------------------------------------------------------------------------------------|--------------|-------|--------------|--------------|-------|--------------|--------------|-------|--------------|---------------|
|             |                                                                                                                           | Min          | Typ   | Max          | Min          | Typ   | Max          | Min          | Typ   | Max          |               |
| $I_{EE}$    | Power Supply Current                                                                                                      |              | 30    | 35           |              | 30    | 35           |              | 32    | 37           | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)                                                                                              | -1085        | -1005 | -880         | -1025        | -955  | -880         | -1025        | -955  | -880         | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)                                                                                               | -1830        | -1695 | -1555        | -1810        | -1705 | -1620        | -1810        | -1705 | -1620        | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                                                                         | -1165        |       | -880         | -1165        |       | -880         | -1165        |       | -880         | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                                                                          | -1810        |       | -1475        | -1810        |       | -1475        | -1810        |       | -1475        | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{PP} < 500 \text{ mV}$<br>$V_{PP} \geq 500 \text{ mV}$ | -2.1<br>-1.9 |       | -0.3<br>-0.3 | -2.2<br>-2.0 |       | -0.3<br>-0.3 | -2.2<br>-2.0 |       | -0.3<br>-0.3 | V             |
| $I_{IH}$    | Input HIGH Current                                                                                                        |              |       | 150          |              |       | 150          |              |       | 150          | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Others<br>CLK                                                                                        | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3 \text{ V}$ .
2. Outputs are terminated through a  $50 \Omega$  resistor to  $V_{CC} - 2.0 \text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1 \text{ V}$ .

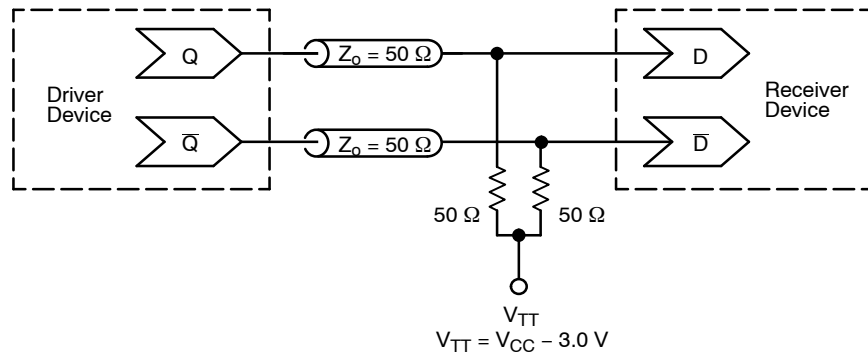
# MC100LVEL51

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol                 | Characteristic                             | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|------------------------|--------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                        |                                            | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{\max}$             | Maximum Toggle Frequency                   | 2.7        |            |            | 2.8        |            |            | 2.9        |            |            | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>to Output<br>CLK<br>R | 330<br>340 | 465<br>455 | 510<br>540 | 340<br>350 | 475<br>465 | 520<br>550 | 370<br>390 | 530<br>510 | 550<br>590 | ps   |
| $t_S$                  | Setup Time                                 | 150        | 0          |            | 150        | 0          |            | 150        | 0          |            | ps   |
| $t_H$                  | Hold Time                                  | 200        | 100        |            | 200        | 100        |            | 200        | 100        |            | ps   |
| $t_{RR}$               | Reset Recovery                             | 350        | 200        |            | 350        | 200        |            | 350        | 200        |            | ps   |
| $t_{PW}$               | Minimum Pulse<br>CLK<br>Width<br>Reset     | 400<br>500 |            |            | 400<br>500 |            |            | 400<br>500 |            |            | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter                      |            | TBD        |            |            | TBD        |            |            | TBD        |            | ps   |
| $V_{PP}$               | Input Swing (Note 2)                       | 150        |            | 1000       | 150        |            | 1000       | 150        |            | 1000       | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% – 80%)    | 120        |            | 320        | 120        |            | 320        | 120        |            | 320        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2.  $V_{PP}$  (min) is minimum input swing for which AC parameters are guaranteed.



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC100LVEL51

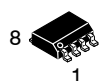
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

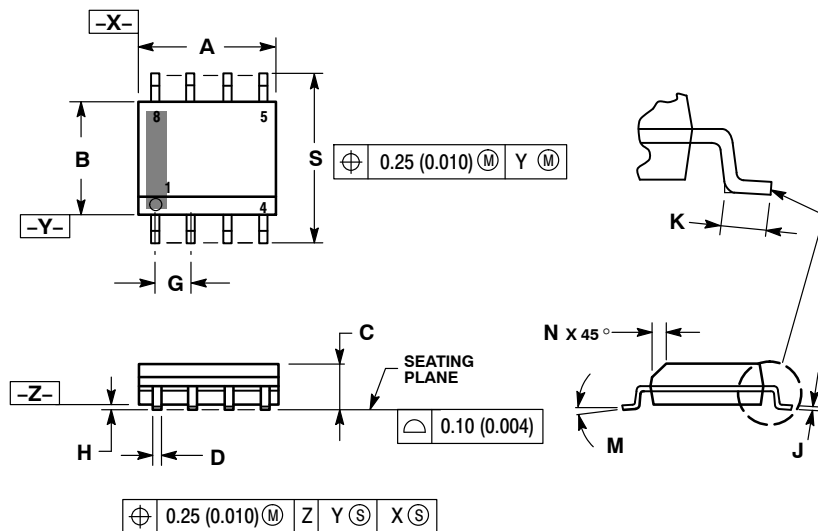
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SCALE 1:1

**SOIC-8 NB**  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

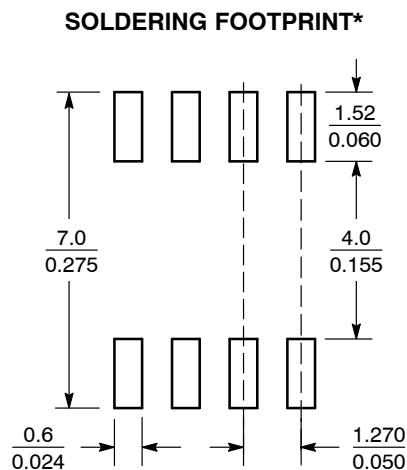


### NOTES:

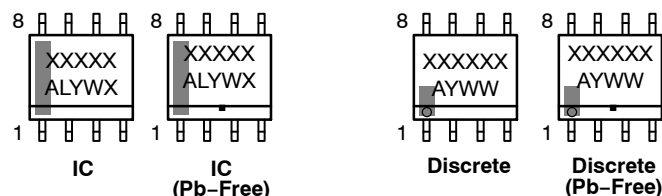
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### GENERIC MARKING DIAGRAM\*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                  |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                      |

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

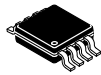
|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

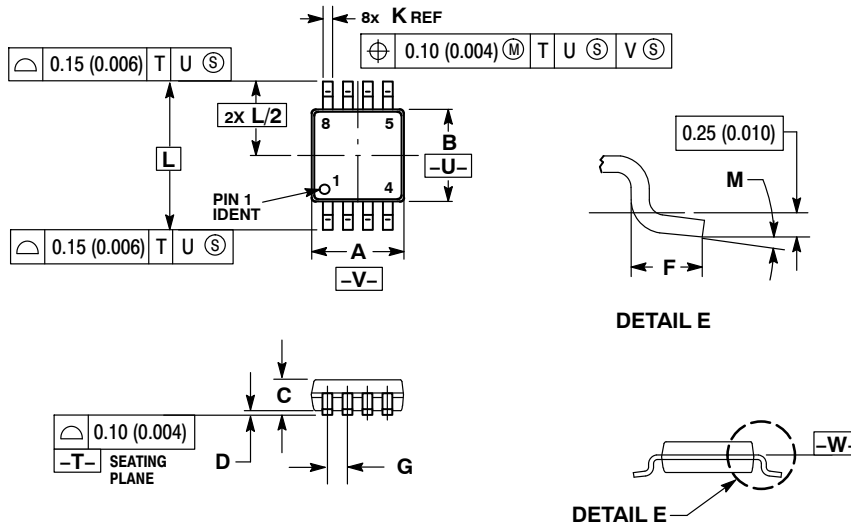
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SCALE 2:1

## TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

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