Data Sheet, Dec. 2000

C505
C505C
C505A
C505CA

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

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Edition 2000-12

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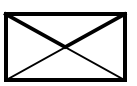
C505/C505C/C505A/C505CA Data Sheet Revision History : Current Version : 2000-12		
Previous Releases :		08.00, 06.00, 07.99, 12.97
Page (in previous version	Page (in current version)	Subjects (major changes since last revision)
24	24	Version register VR2 for C505A-4R/C505CA-4R BB step is updated.

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8-Bit Single-Chip Microcontroller
C500 Family

C505/C505C/C505A/
C505CA

Advance Information

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @16 MHz
  - 300 ns instruction cycle time @20 MHz (50 % duty cycle)
- On-chip program memory (with optional memory protection)
  - C505(C)(A)-2R : 16K byte on-chip ROM
  - C505A-4R/C505CA-4R: 32K byte on-chip ROM
  - C505A-4E/C505CA-4E: 32K byte on-chip OTP
  - alternatively up to 64k byte external program memory
- 256 byte on-chip RAM
- On-chip XRAM
  - C505/C505C : 256 byte
  - C505A/C505CA : 1K byte

(more features on next page)

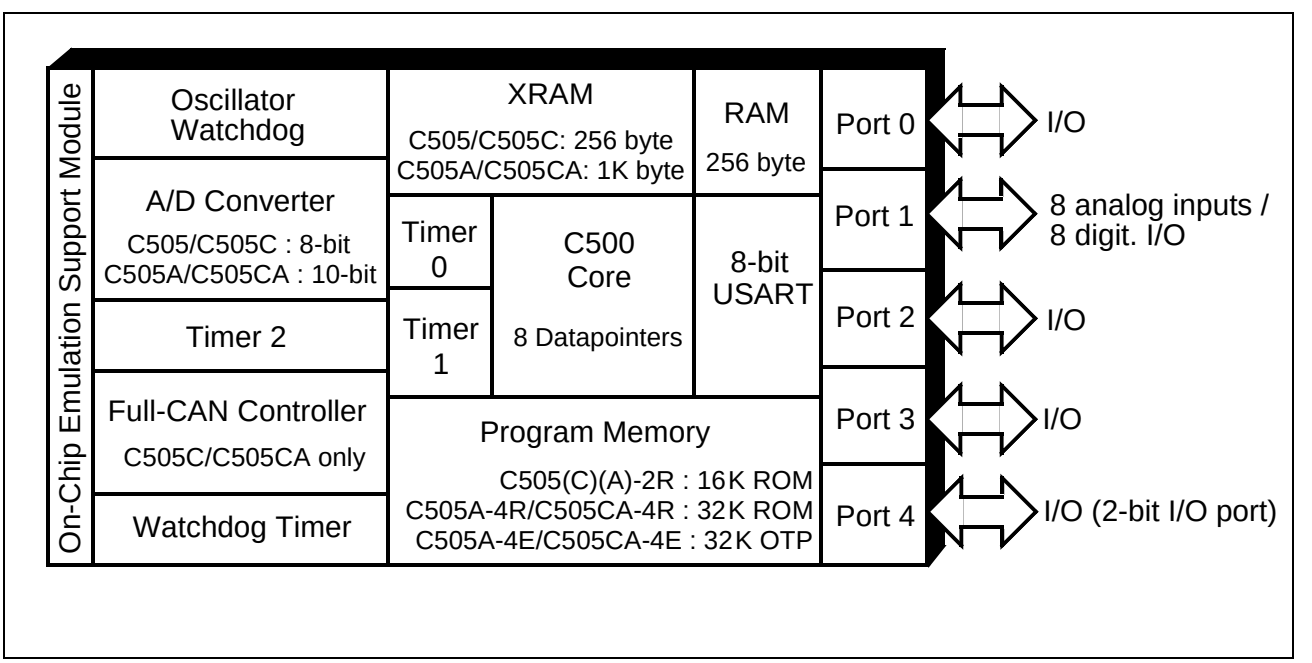


Figure 1
C505 Functional Units

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Features (continued) :

- 32 + 2 digital I/O lines
  - Four 8-bit digital I/O ports
  - One 2-bit digital I/O port (port 4)
  - Port 1 with mixed analog/digital I/O capability
- Three 16-bit timers/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 with 4 channels for 16-bit capture/compare operation
- Full duplex serial interface with programmable baudrate generator (USART)
- Full CAN Module, version 2.0 B compliant (C505C and C505CA only)
  - 256 register/data bytes located in external data memory area
  - 1 MBaud CAN baudrate when operating frequency is equal to or above 8 MHz
  - internal CAN clock prescaler when input frequency is over 10 MHz
- On-chip A/D Converter
  - up to 8 analog inputs
  - C505/C505C : 8-bit resolution
  - C505A/C505CA: 10-bit resolution
- Twelve interrupt sources with four priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- Programmable 15-bit watchdog timer
- Oscillator watchdog
- Fast power on reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake up capability through P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC pin
- P-MQFP-44 package
- Pin configuration is compatible to C501, C504, C511/C513-family
- Temperature ranges:

SAB-C505 versions	T_A = 0 to 70 °C
SAF-C505 versions	T_A = -40 to 85°C
SAH-C505 versions	T_A = -40 to 110°C
SAK-C505 versions	T_A = -40 to 125°C

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Table 1
Differences in Functionality of the C505 MCUs

Device	Internal Program Memory		XRAM Size	A/D Converter Resolution	CAN Controller
	ROM	OTP			
C505-2R	16K byte	–	256 byte	8 Bit	–
C505-L	–	–	256 byte	8 Bit	–
C505C-2R	16K byte	–	256 byte	8 Bit	√
C505C-L	–	–	256 byte	8 Bit	√
C505A-4R	32K byte	–	1K byte	10 Bit	–
C505A-2R	16K byte	–	1K byte	10 Bit	–
C505A-L	–	–	1K byte	10 Bit	–
C505CA-4R	32K byte	–	1K byte	10 Bit	√
C505CA-2R	16K byte	–	1K byte	10 Bit	√
C505CA-L	–	–	1K byte	10 Bit	√
C505A-4E	–	32K byte	1K byte	10 Bit	–
C505CA-4E	–	32K byte	1K byte	10 Bit	√

Note: The term C505 refers to all versions described within this document unless otherwise noted. However the term C505 may also be restricted by the context to refer to only CAN-less derivatives with 8-Bit ADC which are C505-2R and C505-L in this document.

Note: The term C505(C)(A)-2R, for simplicity, is used to stand for C505 16K byte ROM versions within this document which are C505-2R, C505C-2R, C505A-2R and C505CA-2R.

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set
- the specificed temperature rage
- the package and the type of delivery

For the available ordering codes for the C505 please refer to the "**Product information Microcontrollers**", which summarizes all available microcontroller variants.

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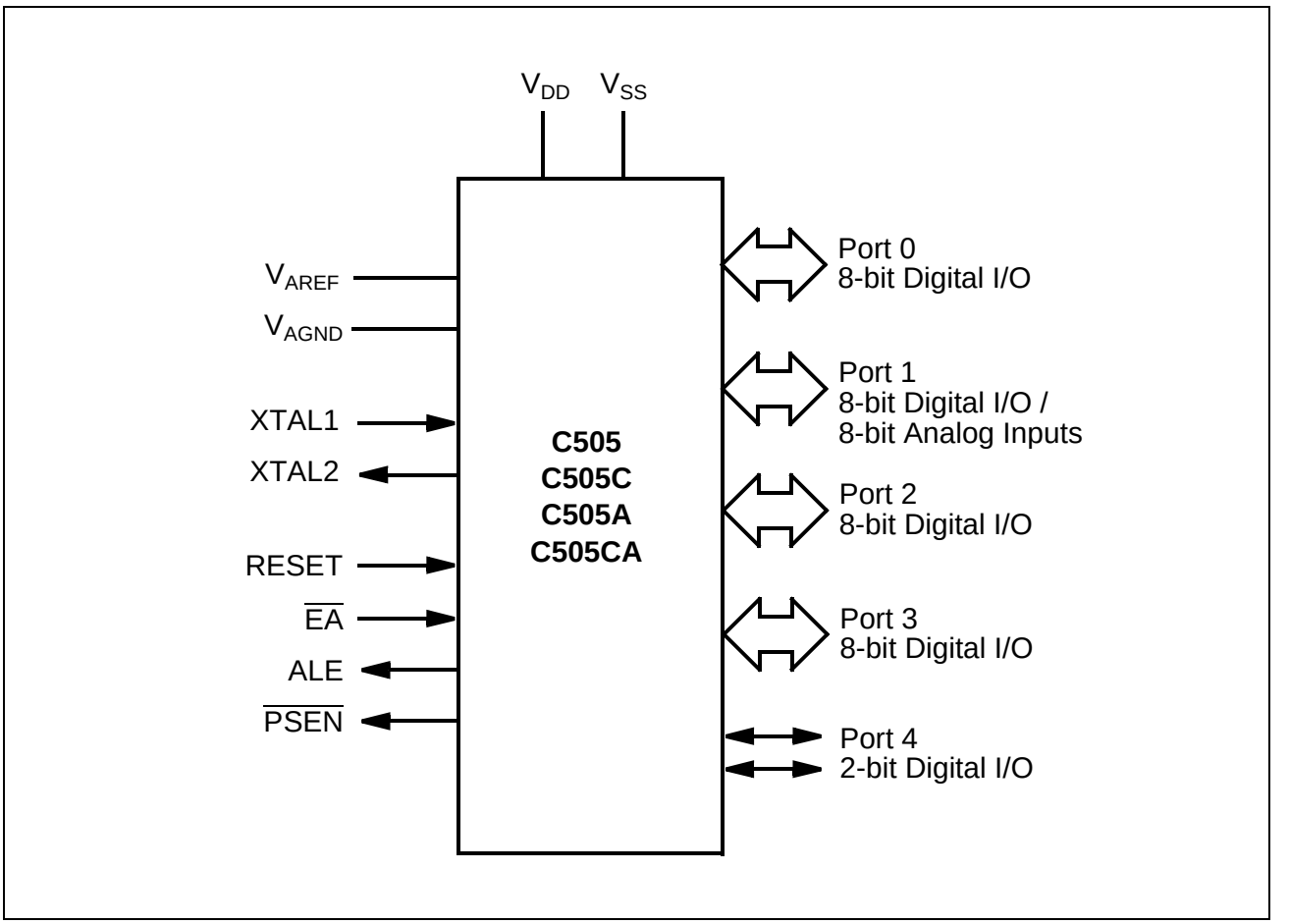


Figure 2
Logic Symbol

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

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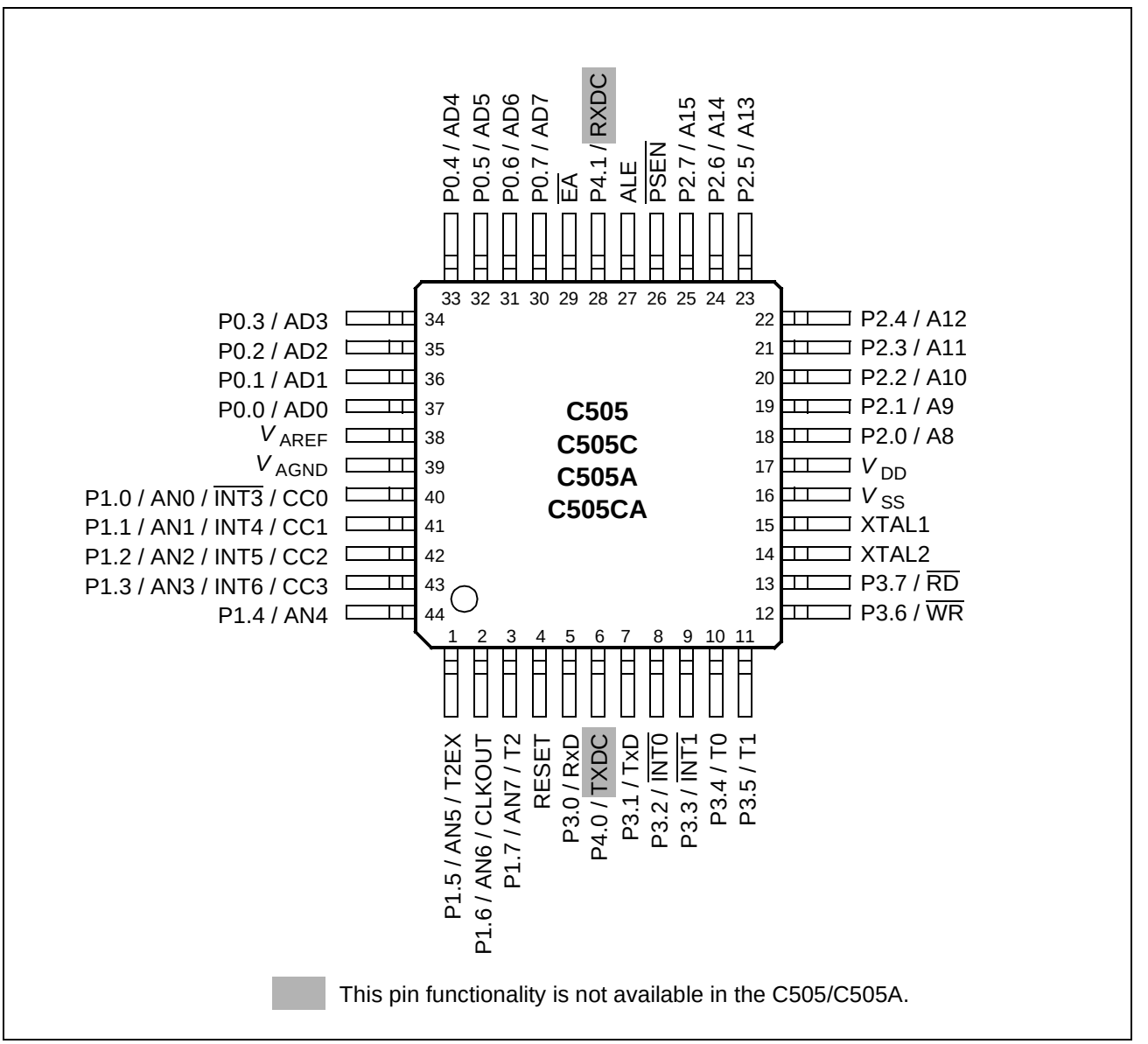


Figure 3
C505 Pin Configuration P-MQFP-44 Package (Top View)

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Table 2
Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function
P1.0-P1.7	40-44,1-3	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs of the A/D converter. Port 1 pins that have 1's written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 — Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O
	41		P1.1 / AN1 / INT4 / CC1 — Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O
	42		P1.2 / AN2 / INT5 / CC2 — Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
	43		P1.3 / AN3 / INT6 / CC3 — Analog input channel 3 interrupt 6 input / capture/compare channel 3 I/O
	44		P1.4 / AN4 — Analog input channel 4
	1		P1.5 / AN5 / T2EX — Analog input channel 5 / Timer 2 external reload / trigger input
	2		P1.6 / AN6 / CLKOUT — Analog input channel 6 / system clock output
	3		P1.7 / AN7 / T2 — Analog input channel 7 / counter 2 input
			Port 1 is used for the low-order address byte during program verification of the C505 ROM versions (i.e. C505(C)(A)-2R/ C505A-4R/C505CA-4R).

*) I = Input
O = Output

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Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
RESET	4	I	**RESET** A high level on this pin for two machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	9		P3.3 / $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	10		P3.4 / T0 — Timer 0 counter input
	11		P3.5 / T1 — Timer 1 counter input
	12		P3.6 / $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

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Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P4.0 P4.1	6 28	I/O I/O	**Port 4** is a 2-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to the secondary function RXDC must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows (C505C and C505CA only) : P4.0 / TXDC Transmitter output of CAN controller P4.1 / RXDC Receiver input of CAN controller
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of the etxernal clock signal of 50 % should be maintained. Minimum and maximum high and low times as well as rise/ fall times specified in the AC characteristics must be observed.

*) I = Input
O = Output

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Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal ROM or OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

*) I = Input
O = Output

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Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
$\overline{EA}$	29	I	**$\overline{External\ Access\ Enable}$** When held at high level, instructions are fetched from the internal program memory when the PC is less than 4000_H (C505(C)(A)-2R) or 8000_H (C505A-4R/C505CA-4R/C505A-4E/C505CA-4E). When held at low level, the C505 fetches all instructions from external program memory. For the C505 romless versions (i.e. C505-L, C505C-L, C505A-L and C505CA-L) this pin must be tied low. For the ROM protection version $\overline{EA}$ pin is latched during reset.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C505 ROM versions. External pullup resistors are required during program verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{DD}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

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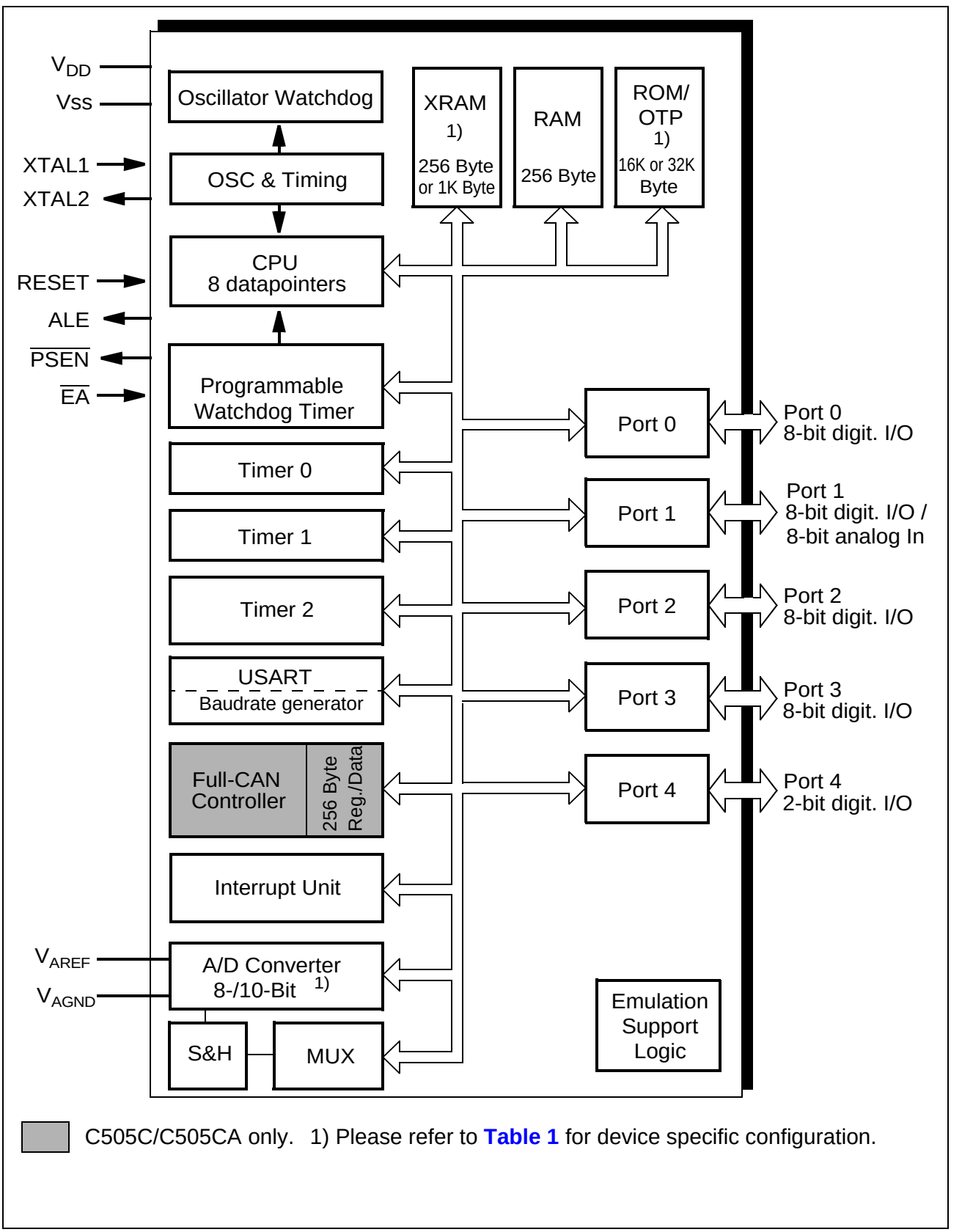


Figure 4
Block Diagram of the C505/C505C/C505A/C505CA

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CPU

The C505 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 16 MHz crystal, 58% of the instructions are executed in 375 ns (20MHz: 300 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	**Carry Flag** Used by arithmetic instruction.
AC	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
F0	**General Purpose Flag**
RS1 RS0	**Register Bank Select Control Bits** These bits are used to select one of the four register banks.
OV	**Overflow Flag** Used by arithmetic instruction.
F1	**General Purpose Flag**
P	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

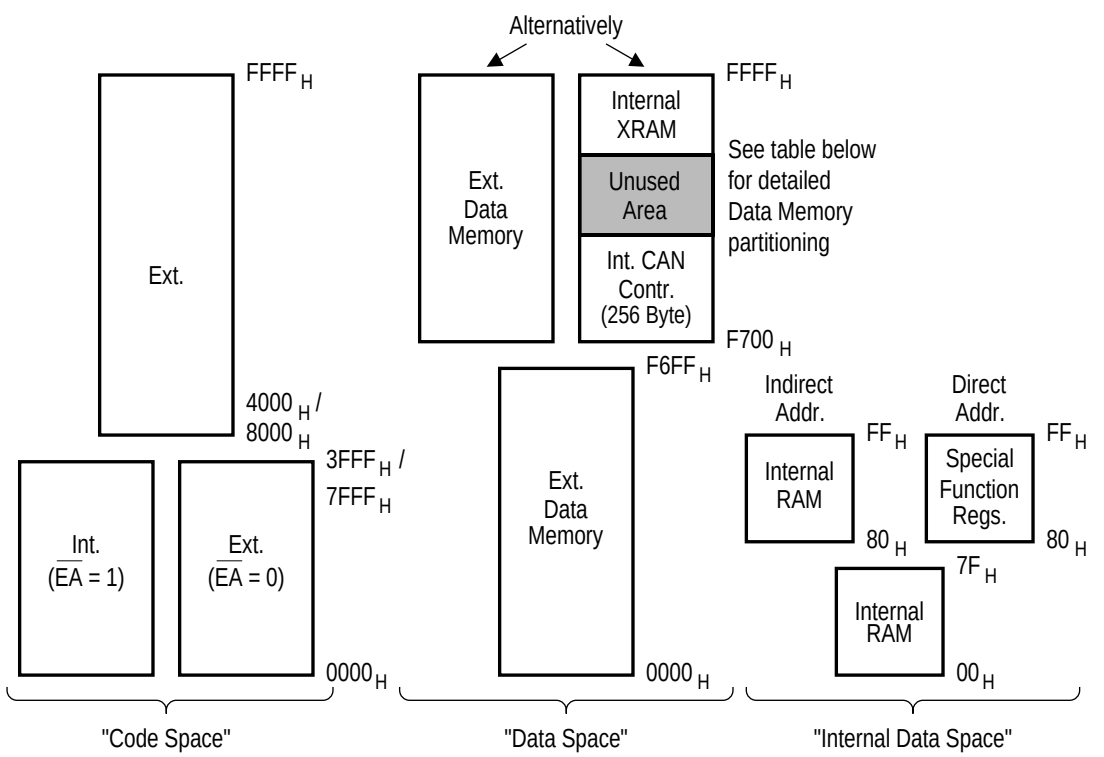
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Memory Organization

The C505 CPU manipulates operands in the following four address spaces:

- On-chip program memory : 16K byte ROM (C505(C)(A)-2R) or
  32K byte ROM (C505A-4R/C505CA-4R) or
  32K byte OTP (C505A-4E/C505CA-4E)
- Totally up to 64K byte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- Internal XRAM data memory : 256 byte (C505/C505C)
  1K byte (C505A/C505CA)
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C505 versions.



"Data Space" $F700_H$ to $FFFF_H$:

Device	CAN Area	Unused Area	XRAM Area
C505	–	$F700_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505C	$F700_H$–$F7FF_H$	$F800_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505A	–	$F700_H$–$FBFF_H$	$FC00_H$–$FFFF_H$
C505CA	$F700_H$–$F7FF_H$	$F800_H$–$FBFF_H$	$FC00_H$–$FFFF_H$

Figure 5
C505 Memory Map Memory Map

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Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the RESET pin to V_{DD} via a capacitor. **Figure 6** shows the possible reset circuitries.

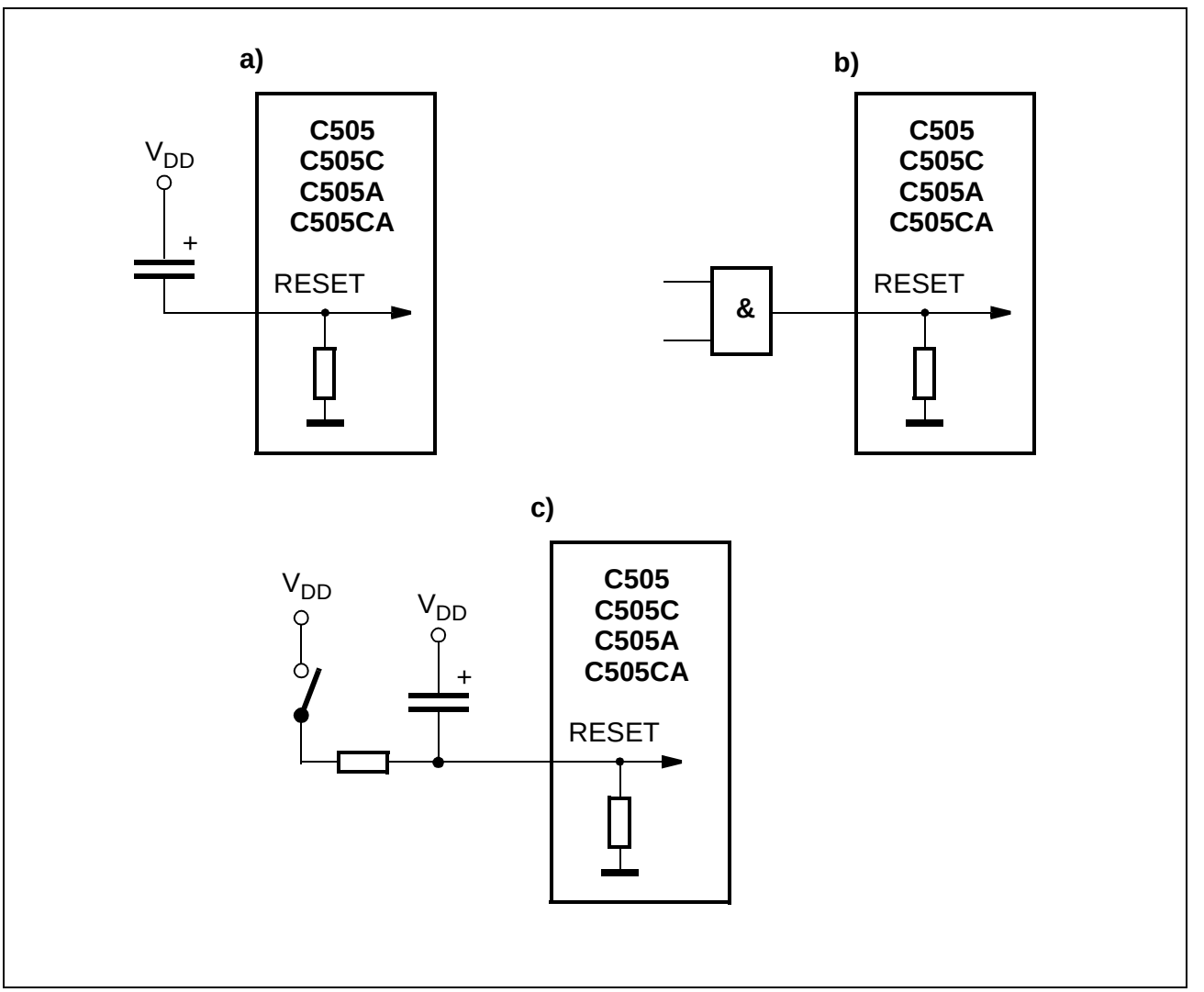


Figure 6
Reset Circuitries

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Figure 7 shows the recommended oscillator circuits for crystal and external clock operation.

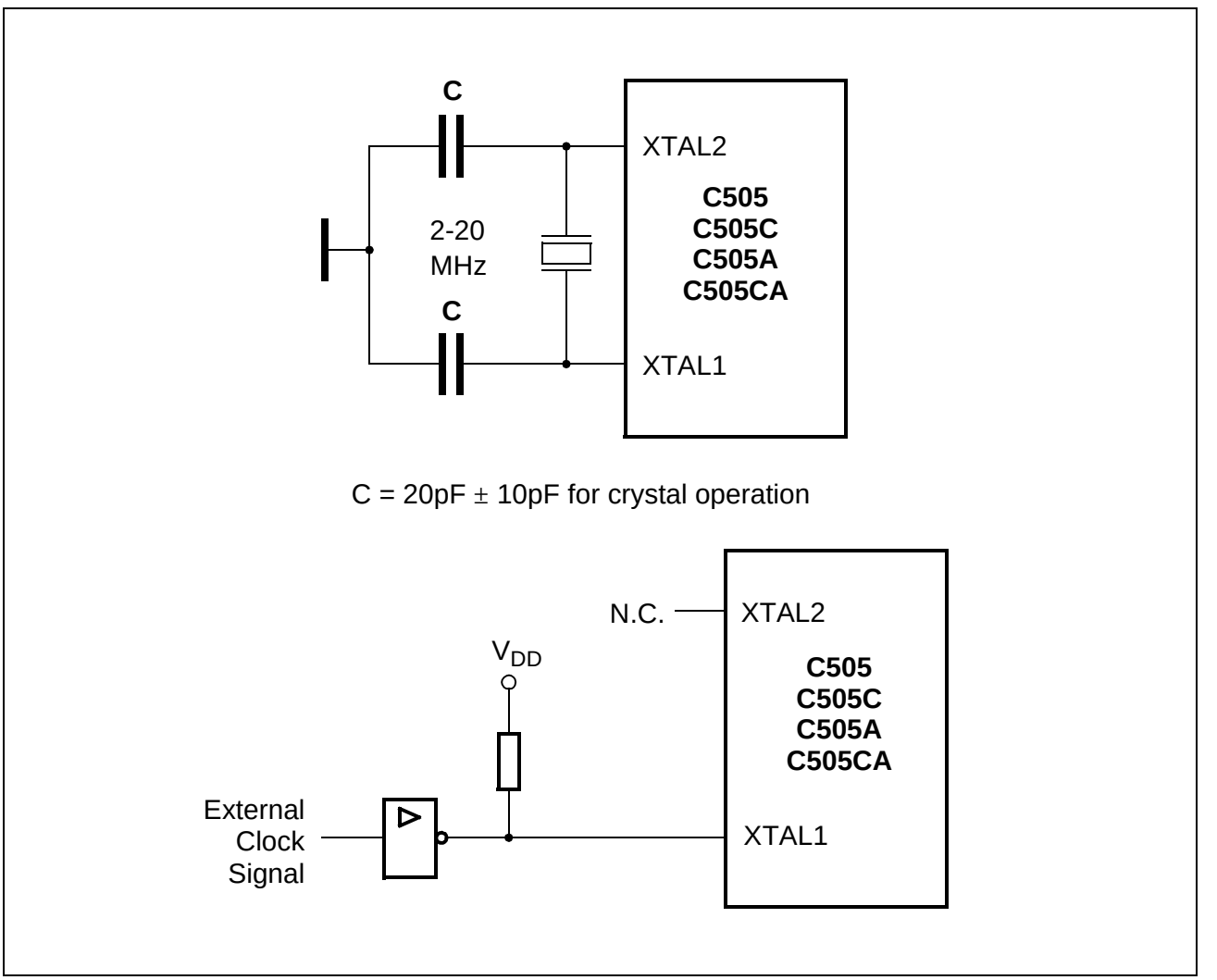


Figure 7
Recommended Oscillator Circuitries

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Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C505 contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function regsiter DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

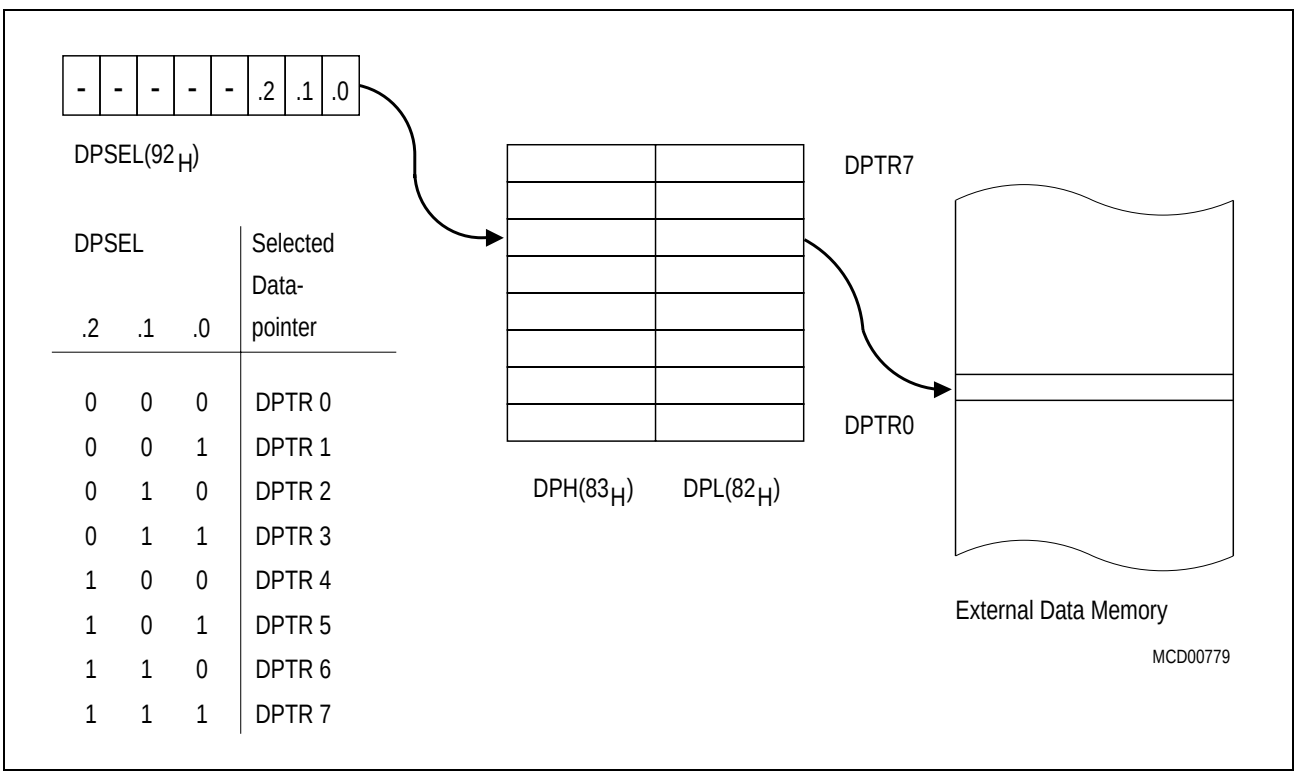


Figure 8
External Data Memory Addressing using Multiple Datapointers

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Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

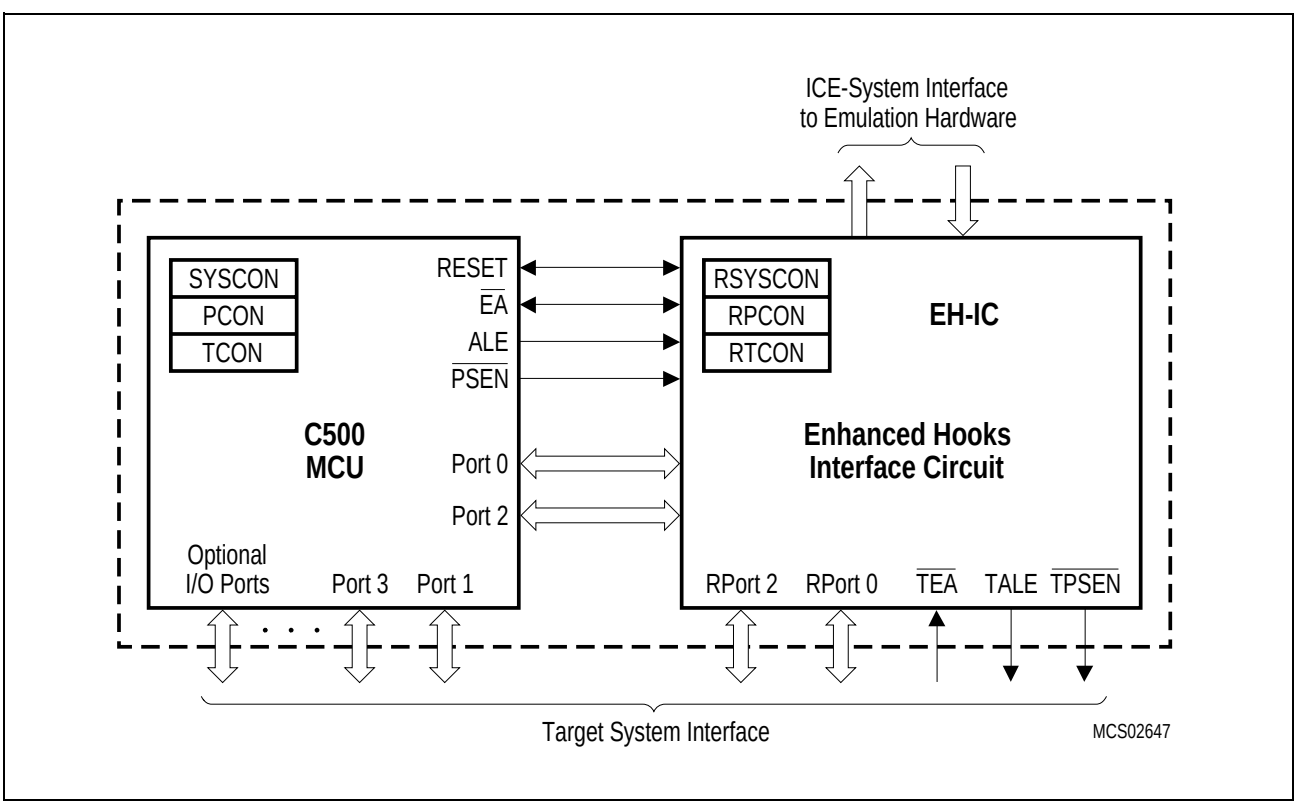


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

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Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions : the standard special function register area and the mapped special function register area. Five special function register of the C505 (PCON1,P1ANA, VR0, VR1, VR2) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

The registers and data locations of the CAN controller (CAN-SFRs) are located in the external data memory area at addresses $F700_H$ to $F7FF_H$..

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100X01_B$**
(C505CA only) **Reset Value : $XX100001_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	CMOD	CSWO 1)	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described here.
1) This bit is only available in the C505CA.

Bit	Function
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
CSWO	CAN Controller switch-off bit CSWO = 0 : CAN Controller is enabled (default after reset). CSWO = 1 : CAN Controller is switched off.

As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 52 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505 are listed in **Table 3** and **Table 4**. In **Table 3** they are organized in groups which refer to the functional blocks of the C505. The CAN-SFRs (applicable for the C505C and C505CA only) are also included in **Table 3**. **Table 4** illustrates the contents of the SFRs in numeric order of their addresses. **Table 5** list the CAN-SFRs in numeric order of their addresses.

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Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** 1)	00_H
	B	B-Register	**$F0_H$** 1)	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$ 3)
	PSW	Program Status Word Register	**$D0_H$** 1)	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON2)	System Control Register	$B1_H$	$XX100X01_B$ 3) 6) $XX100001_B$ 3) 7)
	VR0 4)	Version Register 0	FC_H	$C5_H$
	VR1 4)	Version Register 1	FD_H	05_H
	VR2 4)	Version Register 2	FE_H	5)
A/D-Converter	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ 3)
	ADDAT	A/D Converter Data Reg. (C505/C505C)	$D9_H$	00_H
	ADST	A/D Converter Start Reg. (C505/C505C)	DA_H	XX_H 3)
	ADDATH	A/D Converter High Byte Data Register (C505A/C505CA)	$D9_H$	00_H
	ADDATL	A/D Converter Low Byte Data Register (C505A/C505CA)	DA_H	$00XXXXXX_B$ 3)
	P1ANA 2) 4)	Port 1 Analog Input Selection Register	90_H	FF_H
Interrupt System	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ 3)
	TCON 2)	Timer Control Register	**88_H** 1)	00_H
	T2CON 2)	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$
	SCON 2)	Serial Channel Control Register	**98_H** 1)	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$** 1)	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON2)	System Control Register	$B1_H$	$XX100X01_B$ 3) 6) $XX100001_B$ 3) 7)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved
4) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The content of this SFR varies with the actual step of the C505 (eg. 01_H for the first step)
6) C505 / C505A/C505C only
7) C505CA only

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Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2) 4)	Port 1 Analog Input Selection Register	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**E8H** 1)	$XXXXXX11_B$
Serial Channel	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H 3)
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$ 3)
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
Pow. Save Modes	PCON 2)	Power Control Register	87_H	00_H
	PCON1 4)	Power Control Register 1	**88_H** 1)	$0XX0XXXX_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

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Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
CAN Controller (C505C/ C505CA only)	CR	Control Register	$F700_H$	01_H
	SR	Status Register	$F701_H$	XX_H 3)
	IR	Interrupt Register	$F702_H$	XX_H 3)
	BTR0	Bit Timing Register Low	$F704_H$	UU_H 3)
	BTR1	Bit Timing Register High	$F705_H$	$0UUUUUUU_B$ 3)
	GMS0	Global Mask Short Register Low	$F706_H$	UU_H 3)
	GMS1	Global Mask Short Register High	$F707_H$	$UUU11111_B$ 3)
	UGML0	Upper Global Mask Long Register Low	$F708_H$	UU_H 3)
	UGML1	Upper Global Mask Long Register High	$F709_H$	UU_H 3)
	LGML0	Lower Global Mask Long Register Low	$F70A_H$	UU_H 3)
	LGML1	Lower Global Mask Long Register High	$F70B_H$	$UUUUU000_B$ 3)
	UMLM0	Upper Mask of Last Message Register Low	$F70C_H$	UU_H 3)
	UMLM1	Upper Mask of Last Message Register High	$F70D_H$	UU_H 3)
	LMLM0	Lower Mask of Last Message Register Low	$F70E_H$	UU_H 3)
	LMLM1	Lower Mask of Last Message Register High	$F70F_H$	$UUUUU000_B$ 3)
		Message Object Registers :		
	MCR0	Message Control Register Low	$F7n0_H$ 5)	UU_H 3)
	MCR1	Message Control Register High	$F7n1_H$ 5)	UU_H 3)
	UAR0	Upper Arbitration Register Low	$F7n2_H$ 5)	UU_H 3)
	UAR1	Upper Arbitration Register High	$F7n3_H$ 5)	UU_H 3)
	LAR0	Lower Arbitration Register Low	$F7n4_H$ 5)	UU_H 3)
	LAR1	Lower Arbitration Register High	$F7n5_H$ 5)	$UUUUU000_B$ 3)
	MCFG	Message Configuration Register	$F7n6_H$ 5)	$UUUUUU00_B$ 3)
	DB0	Message Data Byte 0	$F7n7_H$ 5)	XX_H 3)
	DB1	Message Data Byte 1	$F7n8_H$ 5)	XX_H 3)
	DB2	Message Data Byte 2	$F7n9_H$ 5)	XX_H 3)
	DB3	Message Data Byte 3	$F7nA_H$ 5)	XX_H 3)
	DB4	Message Data Byte 4	$F7nB_H$ 5)	XX_H 3)
	DB5	Message Data Byte 5	$F7nC_H$ 5)	XX_H 3)
	DB6	Message Data Byte 6	$F7nD_H$ 5)	XX_H 3)
	DB7	Message Data Byte 7	$F7nE_H$ 5)	XX_H 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The notation "n" (n= 1 to F) in the message object address definition defines the number of the related message object.

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Table 4
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [3)]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	T2	CLK-OUT	T2EX	.4	INT6	INT5	INT4	.$\overline{INT3}$
90_H [3)]	P1ANA	FF_H	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	00_H	EA	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

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Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$[2)]	P3	FF_H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD
$B1_H$	SYSCON[3)]	$XX10\text{-}0X01_B$	–	–	EALE	RMAP	CMOD	–	XMAP1	XMAP0
$B1_H$	SYSCON[4)]	$XX10\text{-}0001_B$	–	–	EALE	RMAP	CMOD	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	ECAN	EADC
$B9_H$	IP1	$XX00\text{-}0000_B$	–	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	$00X0\text{-}0000_B$	T2PS	I3FR	–	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$[2)]	ADCON0	$00X0\text{-}0000_B$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) C505 /C505C/C505A only
4) C505CA only

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Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D9_H$	ADDAT [6)]	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D9_H$	ADDATH [7)]	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADST [6)]	$XXXX\text{-}XXXX_B$	–	–	–	–	–	–	–	–
DA_H	ADDATL [7)]	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DC_H	ADCON1	$01XX\text{-}X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	RXDC	TXDC
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FC_H[3)4)]	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H[3)4)]	VR1	05_H	0	0	0	0	0	1	0	1
FE_H[3)4)]	VR2 [5)]	01_H[8)] 12_H[9)] 33_H[10)]	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) These are read-only registers
5) The content of this SFR varies with the actual of the step C505 (eg. 01_H or 11_H or 21_H for the first step)
6) C505 / C505C only
7) C505A / C505CA only
8) C505 / C505C AB step only
9) C505A-4E / C505CA-4E BA step only (11_H for the AA step)
10) C505A-4R / C505CA-4R BB step only (32_H for the BA step)

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Table 5
Contents of the CAN Registers in numeric order of their addresses (C505C/C505CA only)

Addr. n=1-F$_H$ 1)	Register	Content after Reset 2)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F700$_H$	CR	01$_H$	TEST	CCE	0	0	EIE	SIE	IE	INIT
F701$_H$	SR	XX$_H$	BOFF	EWRN	–	RXOK	TXOK	LEC2	LEC1	LEC0
F702$_H$	IR	XX$_H$	INTID							
F704$_H$	BTR0	UU$_H$	SJW		BRP					
F705$_H$	BTR1	0UUU. UUUU$_B$	0	TSEG2			TSEG1			
F706$_H$	GMS0	UU$_H$	ID28-21							
F707$_H$	GMS1	UUU1. 1111$_B$	ID20-18			1	1	1	1	1
F708$_H$	UGML0	UU$_H$	ID28-21							
F709$_H$	UGML1	UU$_H$	ID20-13							
F70A$_H$	LGML0	UU$_H$	ID12-5							
F70B$_H$	LGML1	UUUU. U000$_B$	ID4-0					0	0	0
F70C$_H$	UMLM0	UU$_H$	ID28-21							
F70D$_H$	UMLM1	UU$_H$	ID20-18			ID17-13				
F70E$_H$	LMLM0	UU$_H$	ID12-5							
F70F$_H$	LMLM1	UUUU. U000$_B$	ID4-0					0	0	0
F7n0$_H$	MCR0	UU$_H$	MSGVAL		TXIE		RXIE		INTPND	
F7n1$_H$	MCR1	UU$_H$	RMTPND		TXRQ		MSGLST CPUUPD		NEWDAT	
F7n2$_H$	UAR0	UU$_H$	ID28-21							
F7n3$_H$	UAR1	UU$_H$	ID20-18			ID17-13				
F7n4$_H$	LAR0	UU$_H$	ID12-5							
F7n5$_H$	LAR1	UUUU. U000$_B$	ID4-0					0	0	0

1) The notation “n“ (n= 1 to F) in the address definition defines the number of the related message object.
2) “X“ means that the value is undefined and the location is reserved. “U“ means that the value is unchanged by a reset operation. “U“ values are undefined (as “X“) after a power-on reset operation

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Table 5
Contents of the CAN Registers in numeric order of their addresses (cont'd)
(C505C/C505CA only)

Addr. n=1-F$_H$ **1)**	**Register**	**Content after Reset 2)**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
F7n6$_H$	MCFG	UUUU. UU00$_B$	DLC				DIR	XTD	0	0
F7n7$_H$	DB0	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7n8$_H$	DB1	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7n9$_H$	DB2	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nA$_H$	DB3	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nB$_H$	DB4	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nC$_H$	DB5	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nD$_H$	DB6	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0
F7nE$_H$	DB7	XX$_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) The notation "n" (n= 1 to F) in the address definition defines the number of the related message object.
2) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation

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I/O Ports

The C505 has four 8-bit I/O ports and one 2-bit I/O port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 4 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 4 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET .

Port 4 is 2-bit I/O port with CAN controller specific alternate functions. The eight analog input lines are realized as mixed digital/analog inputs. The 8 analog inputs, AN0-AN7, are located at the port 1 pins P1.0 to P1.7. After reset, all analog inputs are disabled and the related pins of port 1 are configured as digital inputs. The analog function of a specific port 1 pin is enabled by bits in the SFR P1ANA. Writing a 0 to a bit position of P1ANA assigns the corresponding pin to operate as analog input.

Note : P1ANA is a mapped SFR and can be only accessed if bit RMAP in SFR SYSCON is set.

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Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{osc}/6x32	f_{osc}/12x32
1	16-bit timer/counter	0	1	f_{osc}/6	f_{osc}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{osc}/6.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{osc}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

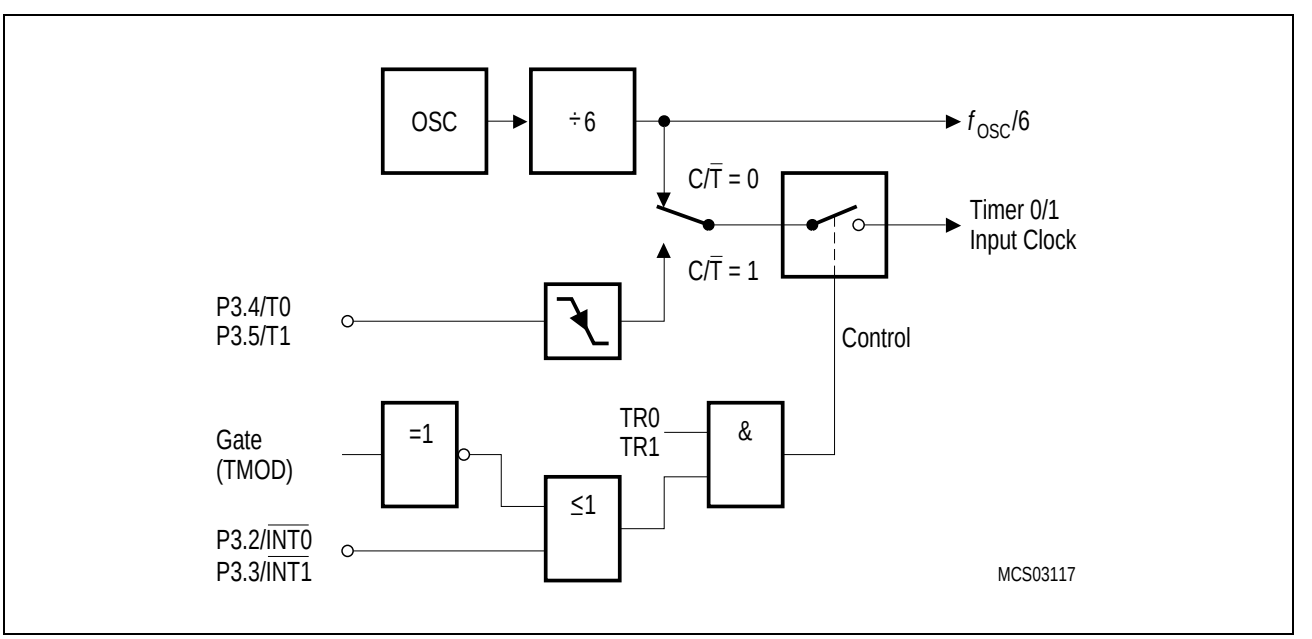


Figure 10
Timer/Counter 0 and 1 Input Clock Logic

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Timer/Counter 2 with Compare/Capture/Reload

The timer 2 of the C505 provides additional compare/capture/reload features. which allow the selection of the following operating modes:

- Compare : up to 4 PWM signals with 16-bit/300 ns resolution (@ 20 MHz clock)
- Capture : up to 4 high speed capture inputs with 300 ns resolution
- Reload : modulation of timer 2 cycle time

The block diagram in **Figure 11** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can used for timer 2 control are located as multifunctional port functions at port 1.

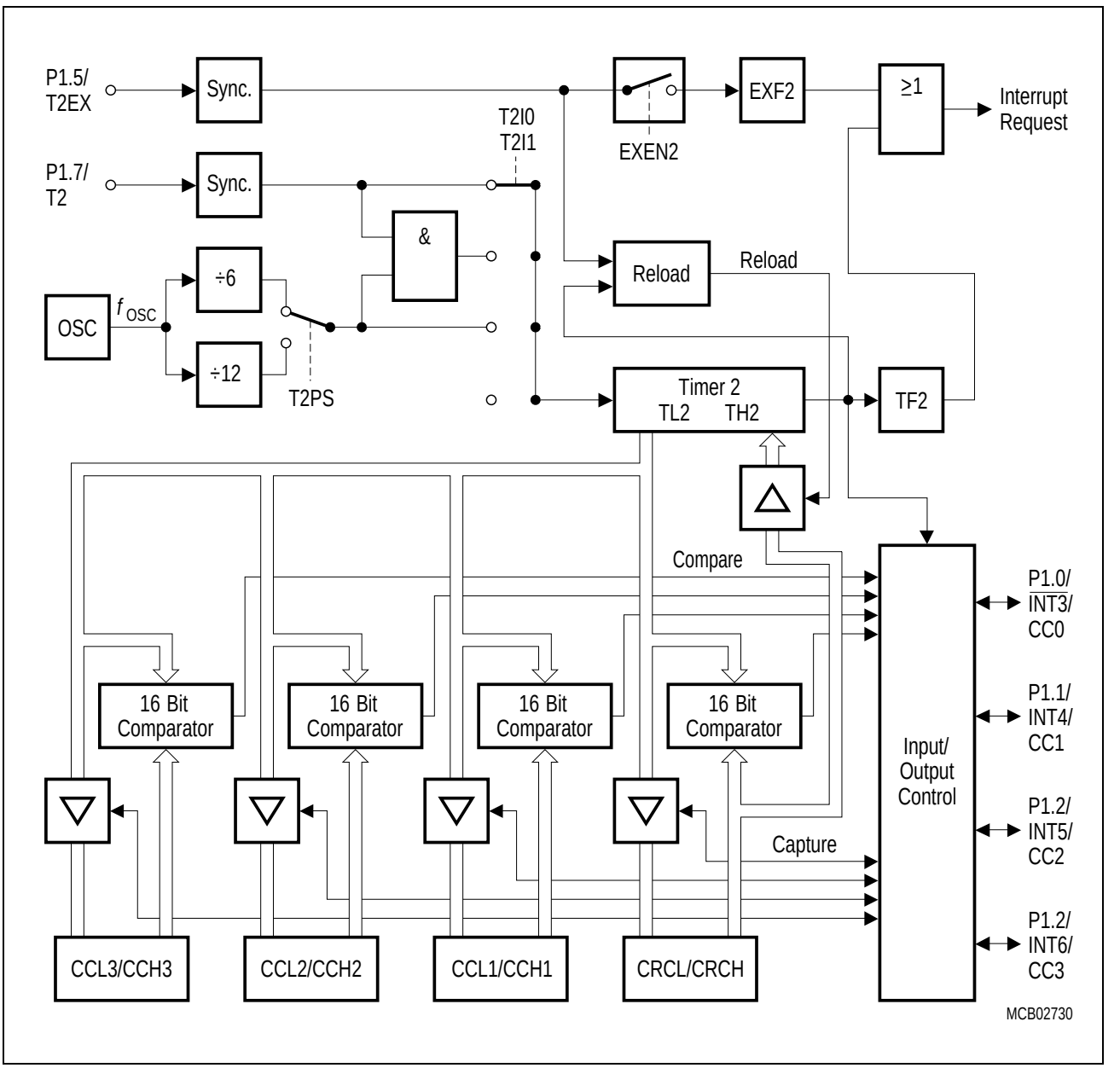


Figure 11
Timer 2 Block Diagram

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Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode : In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode : In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode : In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2 : Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

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Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 12** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

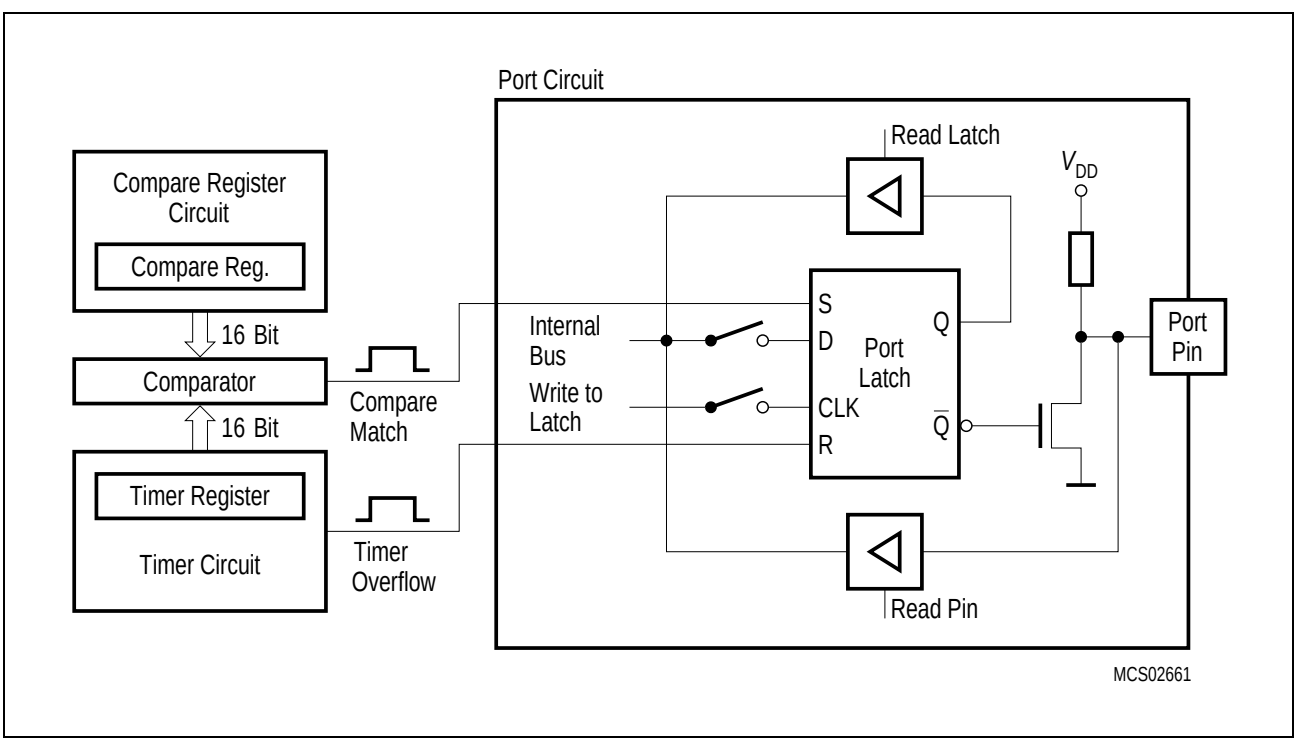


Figure 12
Port Latch in Compare Mode 0

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Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be choosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **Figure 13**) the port circuit consists of two separate latches. One latch (which acts as a "shadow latch") can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

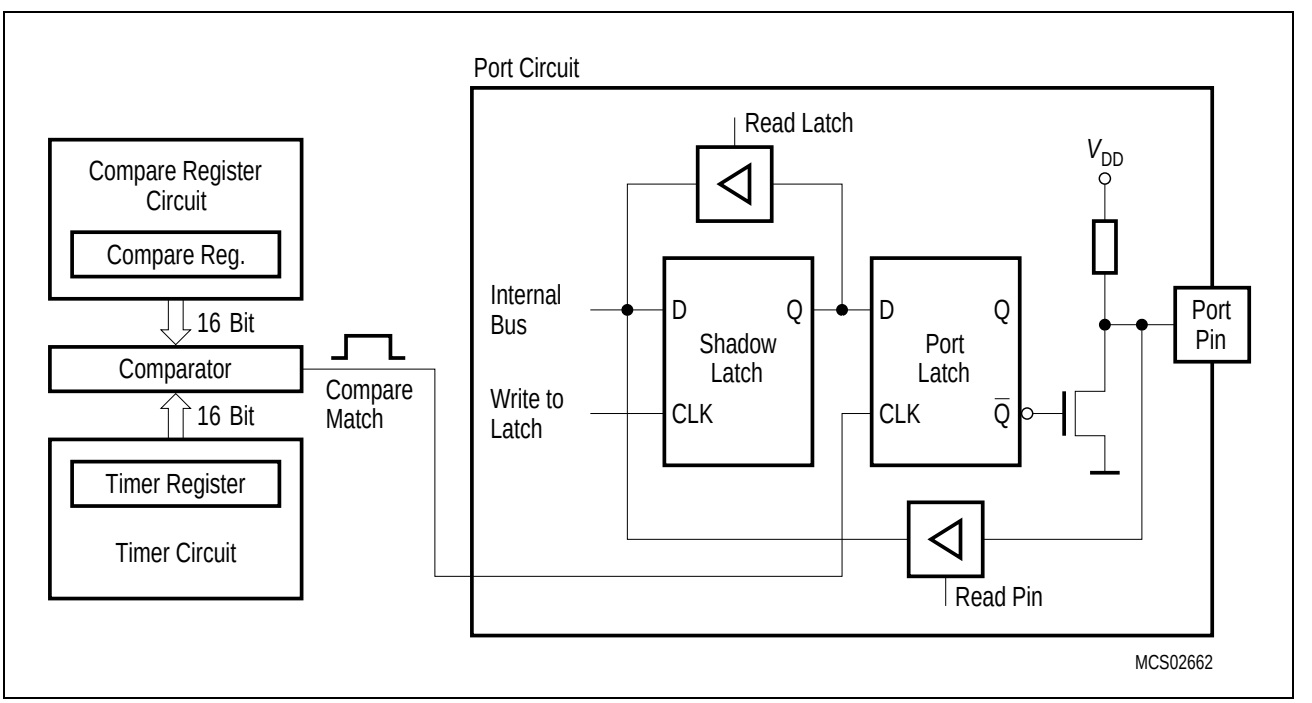


Figure 13
Compare Function in Compare Mode 1

Timer 2 Capture Modes

Each of the compare/capture registers CC1 to CC3 and the CRC register can be used to latch the current 16-bit value of the timer 2 registers TL2 and TH2. Two different modes are provided for this function.

In mode 0, the external event causing a capture is :

- for CC registers 1 to 3: a positive transition at pins CC1 to CC3 of port 1
- for the CRC register: a positive or negative transition at the corresponding pin, depending on the status of the bit I3FR in SFR T2CON.

In mode 1 a capture occurs in response to a write instruction to the low order byte of a capture register. The write-to-register signal (e.g. write-to-CRCL) is used to initiate a capture. The timer 2 contents will be latched into the appropriate capture register in the cycle following the write instruction. In this mode no interrupt request will be generated.

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Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 7**.

Table 7
USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode, fixed baud rate Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	9-bit UART, variable baud rate Like mode 2

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **Figure 14** to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abbrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a decdicated baud rate generator (see **Figure 14**).

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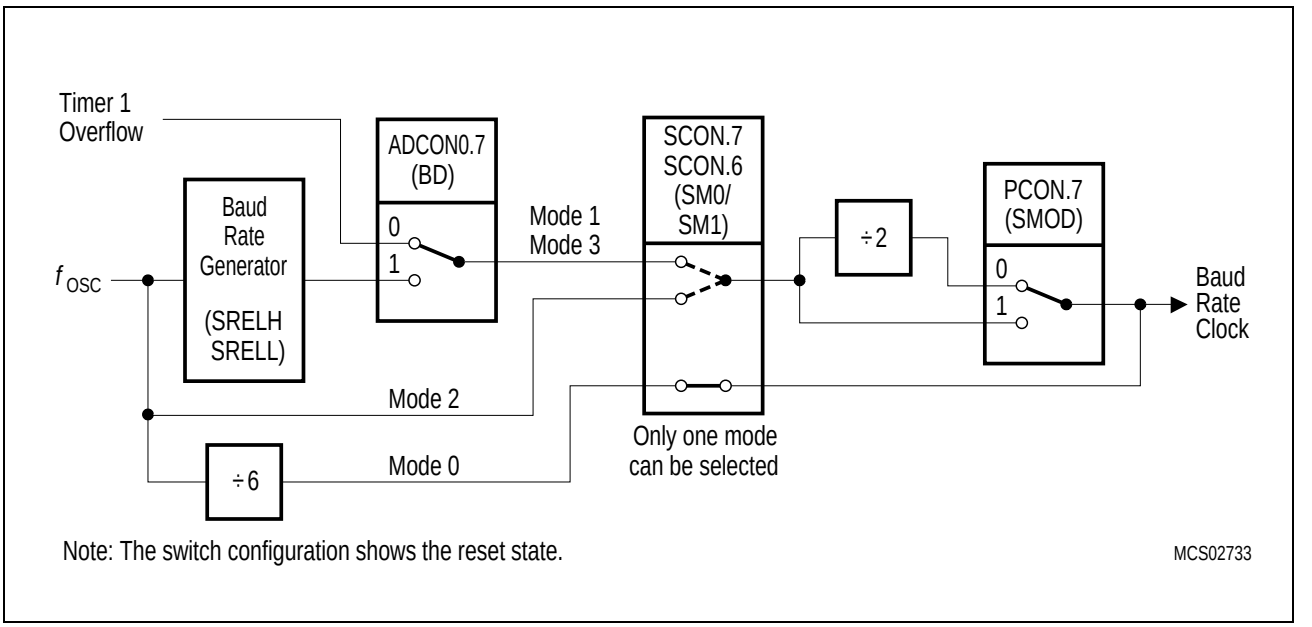


Figure 14
Block Diagram of Baud Rate Generation for the Serial Interface

Table 8 below lists the values/formulas for the baud rate calculation of the serial interface with its dependencies of the control bits BD and SMOD.

Table 8
Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	f_{OSC} / 6
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	X	Controlled by timer 1 overflow : (2^{SMOD} × timer 1 overflow rate) / 32
	1	X	Controlled by baud rate generator (2^{SMOD} × f_{OSC}) / (32 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	0 1	f_{OSC} / 32 f_{OSC} / 16

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CAN Controller (C505C and C505CA only)

The on-chip CAN controller, compliant to version 2.0B, is the functional heart which provides all resources that are required to run the standard CAN protocol (11-bit identifiers) as well as the extended CAN protocol (29-bit identifiers). It provides a sophisticated object layer to relieve the CPU of as much overhead as possible when controlling many different message objects (up to 15). This includes bus arbitration, resending of garbled messages, error handling, interrupt generation, etc. In order to implement the physical layer, external components have to be connected to the C505C/C505CA.

The internal bus interface connects the on-chip CAN controller to the internal bus of the microcontroller. The registers and data locations of the CAN interface are mapped to a specific 256 byte wide address range of the external data memory area ($F700_H$ to $F7FF_H$) and can be accessed using MOVX instructions. **Figure 15** shows a block diagram of the on-chip CAN controller.

The **TX/RX Shift Register** holds the destuffed bit stream from the bus line to allow the parallel access to the whole data or remote frame for the acceptance match test and the parallel transfer of the frame to and from the Intelligent Memory.

The **Bit Stream Processor (BSP)** is a sequencer controlling the sequential data stream between the TX/RX Shift Register, the CRC Register, and the bus line. The BSP also controls the EML and the parallel data stream between the TX/RX Shift Register and the Intelligent Memory such that the processes of reception, arbitration, transmission, and error signalling are performed according to the CAN protocol. Note that the automatic retransmission of messages which have been corrupted by noise or other external error conditions on the bus line is handled by the BSP.

The **Cyclic Redundancy Check Register (CRC)** generates the Cyclic Redundancy Check code to be transmitted after the data bytes and checks the CRC code of incoming messages. This is done by dividing the data stream by the code generator polynomial.

The **Error Management Logic (EML)** is responsible for the fault confinement of the CAN device. Its counters, the Receive Error Counter and the Transmit Error Counter, are incremented and decremented by commands from the Bit Stream Processor. According to the values of the error counters, the CAN controller is set into the states error *active*, error *passive* and busoff.

The **Bit Timing Logic (BTL)** monitors the busline input RXDC and handles the busline related bit timing according to the CAN protocol. The BTL synchronizes on a *recessive* to *dominant* busline transition at *Start of Frame* (hard synchronization) and on any further *recessive* to *dominant* busline transition, if the CAN controller itself does not transmit a *dominant* bit (resynchronization). The BTL also provides programmable time segments to compensate for the propagation delay time and for phase shifts and to define the position of the Sample Point in the bit time. The programming of the BTL depends on the baudrate and on external physical delay times.

The **Intelligent Memory** (CAM/RAM array) provides storage for up to 15 message objects of maximum 8 data bytes length. Each of these objects has a unique identifier and its own set of control and status bits. After the initial configuration, the Intelligent Memory can handle the reception and transmission of data without further microcontroller actions.

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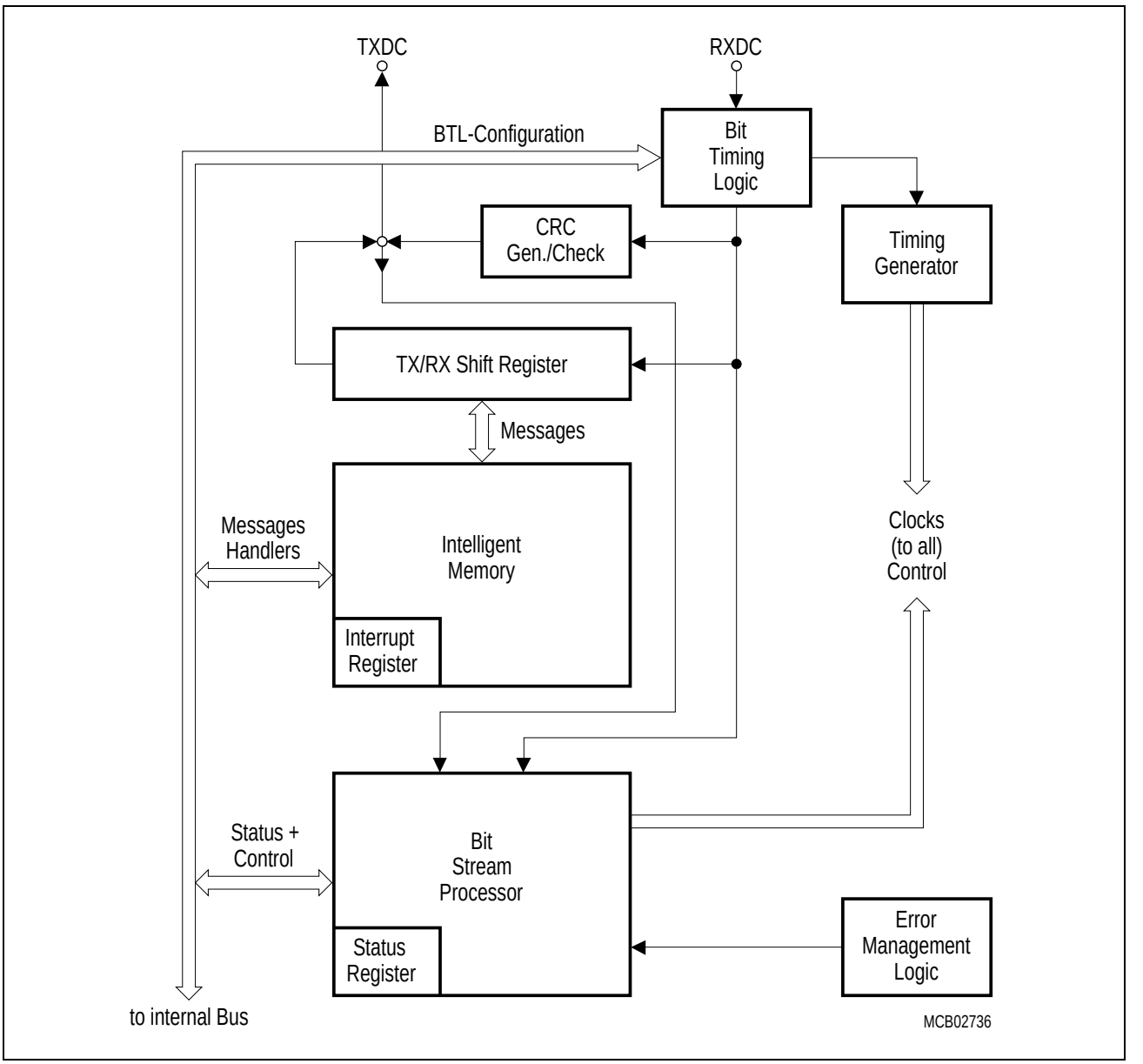


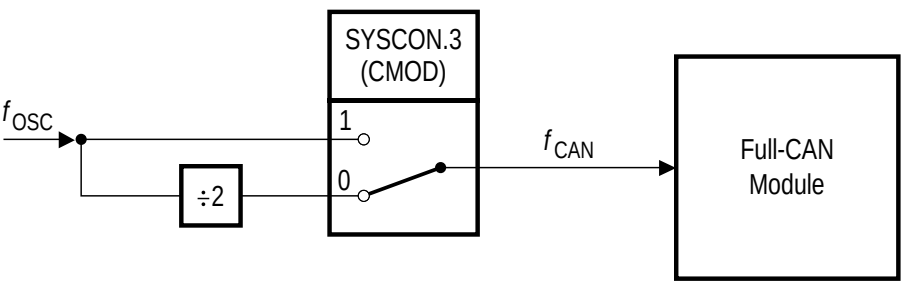
Figure 15
CAN Controller Block Diagram

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CAN Controller Software Initialization

The very first step of the initialization is the CAN controller input clock selection. A divide-by-2 prescaler is enabled by default after reset (**Figure 16**). Setting bit CMOD (SYSCON.3) disables the prescaler. The purpose of the prescaler selection is:

- to ensure that the CAN controller is operable when f_{OSC} is over 10 MHz (bit CMOD =0)
- to achieve the maximum CAN baudrate of 1 Mbaud when f_{OSC} is 8 MHz (bit CMOD=1)



Frequency (MHz)		CMOD (SYSCON.3)	BRP (BTR0.0-5)	CAN baudrate (Mbaud/sec)
f_{OSC}	f_{CAN}			
8	8	1	000000_B	1
8	4	0	000000_B	0.5
16	8	0	000000_B	1

Note : The switch configuration shows the reset state of bit CMOD.

Figure 16
CAN controller Input Clock Selection

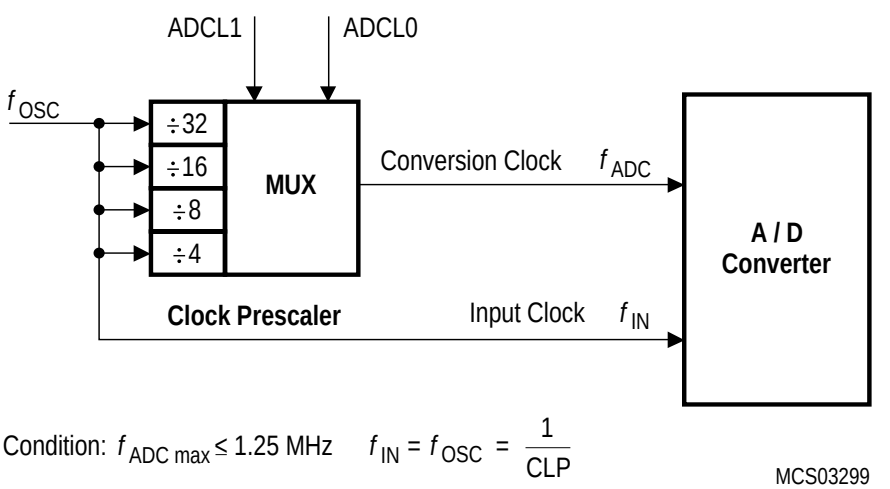
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8-Bit A/D Converter (C505 and C505C only)

The C505/C505C includes a high performance / high speed 8-bit A/D converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital outputs/inputs
- 8-bit resolution
- Internal start-of-conversion trigger
- Interrupt request generation after each conversion
- Single or continuous conversion mode

The 8-bit ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (1/t_{IN}). f_{ADC} is derived from the C505 system clock f_{OSC} which is applied at the XTAL pins via the ADC clock prescaler as shown in **Figure 17**. The input clock is equal to f_{OSC}. The conversion clock f_{ADC} is limited to a maximum frequency of 1.25 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 1.25 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
5 MHz	5	÷ 4	1.25	0	0
6 MHz	6	÷ 8	0.75	0	1
10 MHz	10	÷ 8	1.25	0	1
12 MHz	12	÷ 16	0.75	1	0
16 MHz	16	÷ 16	1	1	0
20 MHz	20	÷ 16	1.25	1	0

Figure 17
8-Bit A/D Converter Clock Selection

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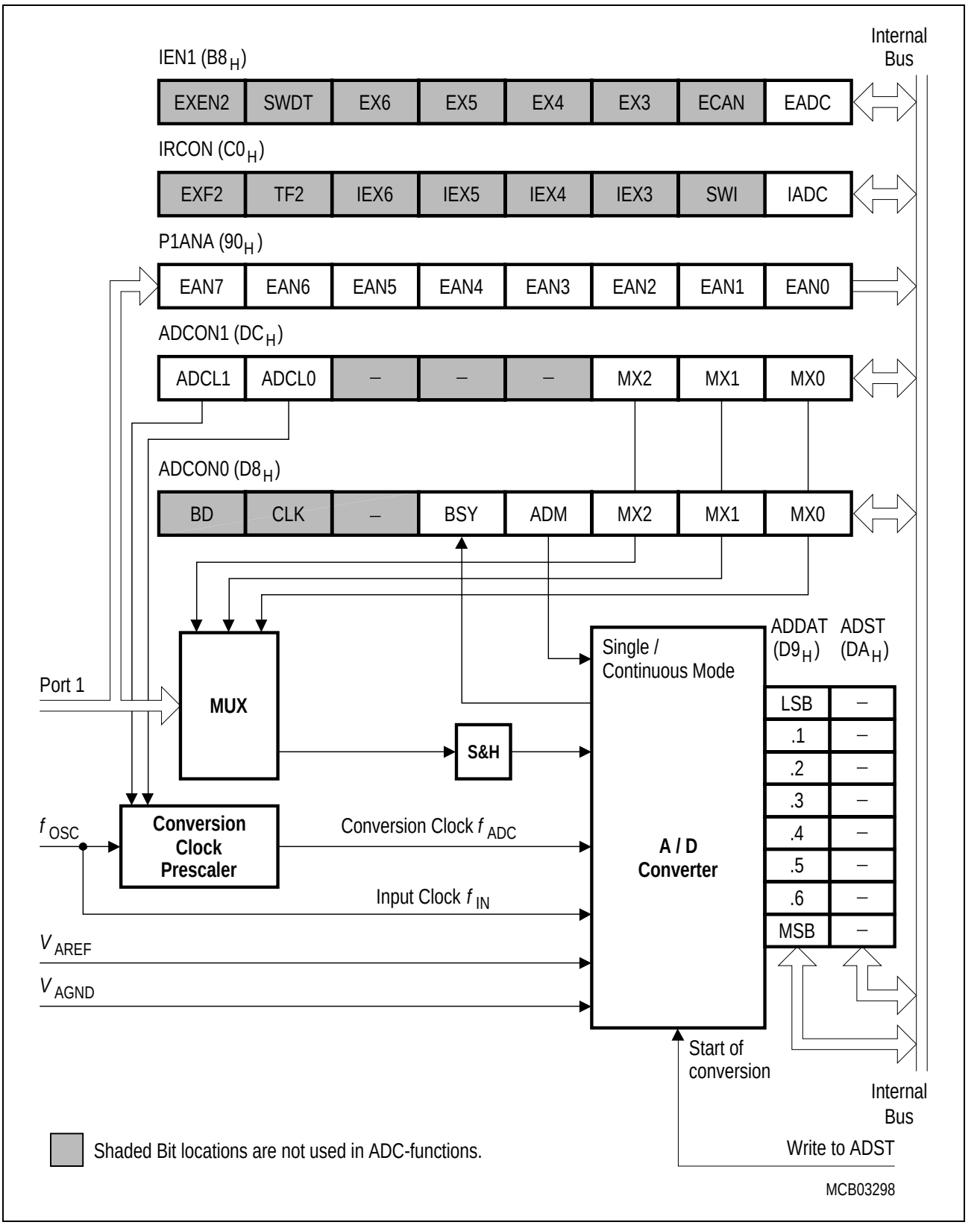


Figure 18
Block Diagram of the 8-Bit A/D Converter

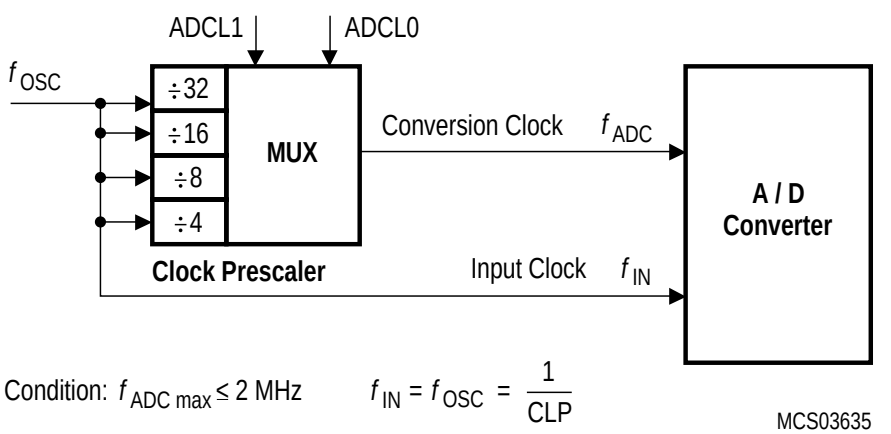
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10-Bit A/D Converter (C505A and C505CA only)

The C505A/C505CA includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital inputs/outputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The 10-bit ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (=1/t_{IN}). f_{ADC} is derived from the C505 system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is equal to f_{OSC} The conversion f_{ADC} clock is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
6 MHz	6	÷ 4	1.5	0	0
8 MHz	8	÷ 4	2	0	0
12 MHz	12	÷ 8	1.5	0	1
16 MHz	16	÷ 8	2	0	1
20 MHz	20	÷ 16	1.25	1	0

Figure 19
10-Bit A/D Converter Clock Selection

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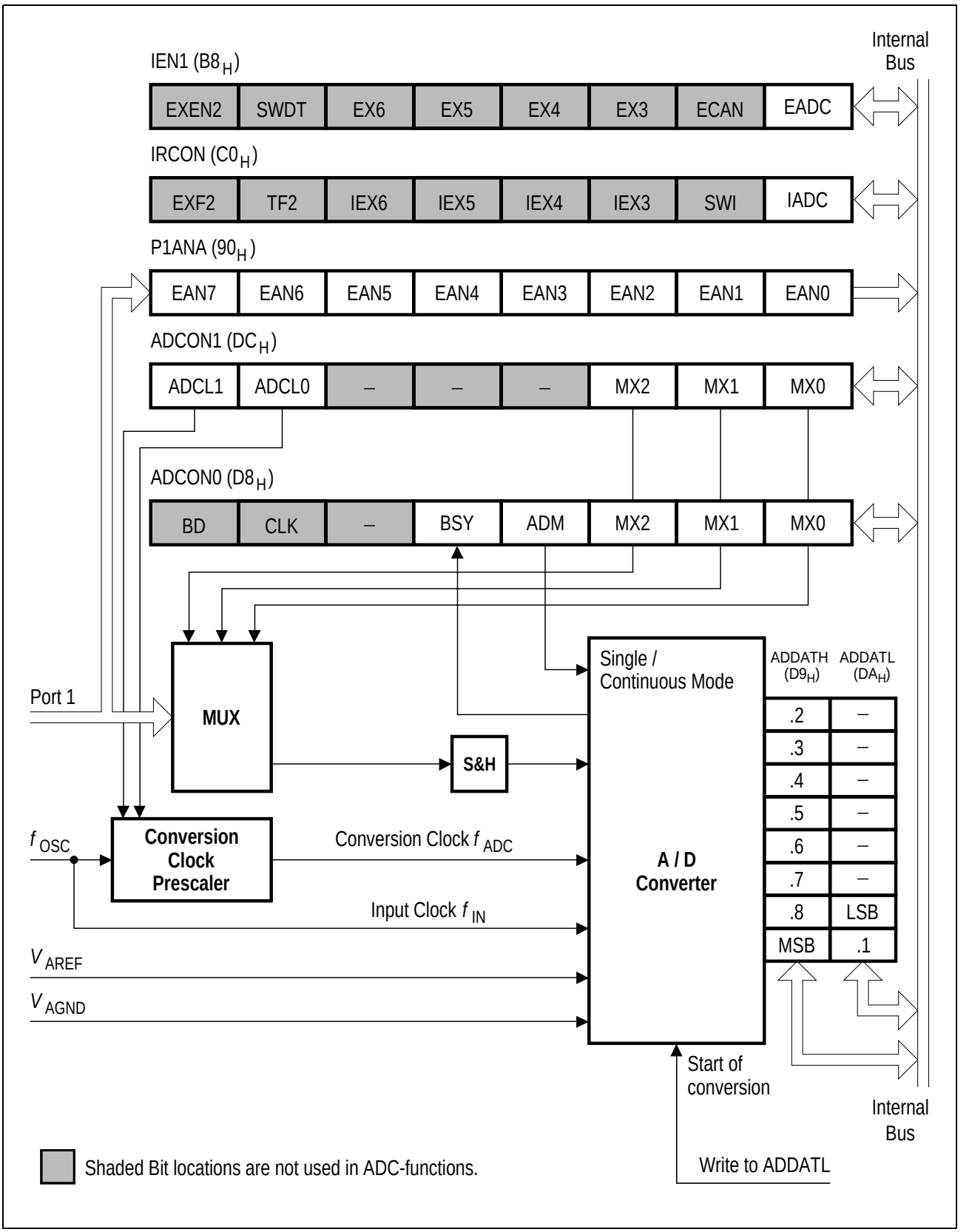


Figure 20
Block Diagram of the 10-Bit A/D Converter

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Interrupt System

The C505 provides 12 interrupt vectors with four priority levels. Five interrupt requests can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial interface, A/D converter). One interrupt can be generated by the CAN controller (C505C and C505CA only) or by a software setting and in this case the interrupt vector is the same. Six interrupts may be triggered externally (P3.2/$\overline{\text{INT0}}$, P3.3/$\overline{\text{INT1}}$, P1.0/AN0/$\overline{\text{INT3}}$/CC0, P1.1/AN1/INT4/CC1, P1.2/AN2/INT5/CC2, P1.3/AN3/INT6/CC3). Additionally, the P1.5/AN5/T2EX can trigger an interrupt. The wake-up from power-down mode interrupt has a special functionality which allows to exit from the software power-down mode by a short low pulse at either pin P3.2/$\overline{\text{INT0}}$ or the pin P4.1/RXDC.

Figure 21 to **Figure 23** give a general overview of the interrupt sources and illustrate the request and the control flags which are described in the next sections. **Table 9** lists all interrupt sources with their request flags and interrupt vector addresses.

Table 9
Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel	0023_H	RI / TI
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
CAN Controller / Software Interrupt	$004B_H$	– / SWI
External interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External interrupt 6	$006B_H$	IEX6
Wake-up from power-down mode	$007B_H$	–

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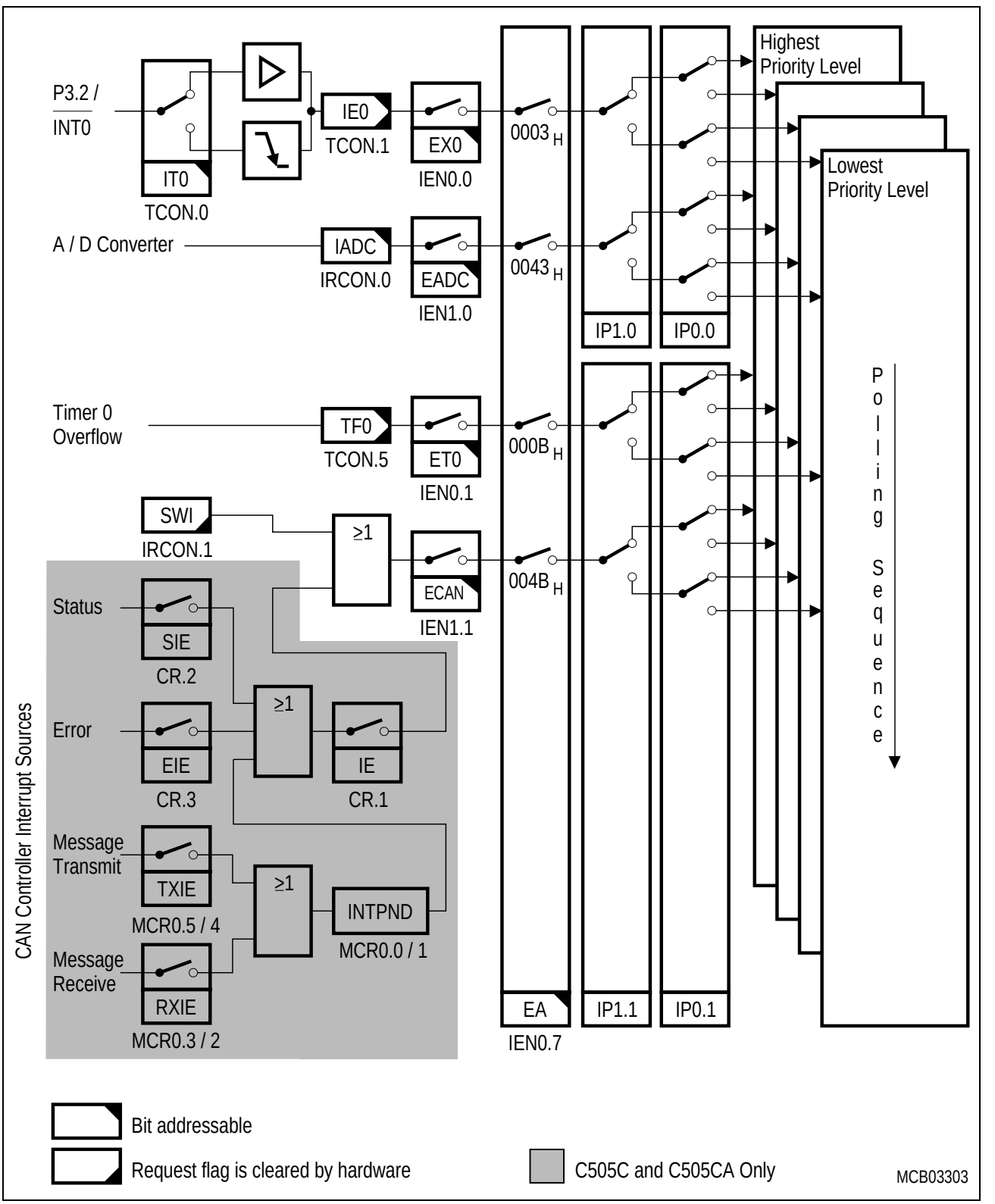


Figure 21
Interrupt Structure, Overview Part 1

*Note: Each of the 15 CAN controller message objects (C505C and C505CA only), shown in the shaded area of **Figure 21** provides the bits/flags.*

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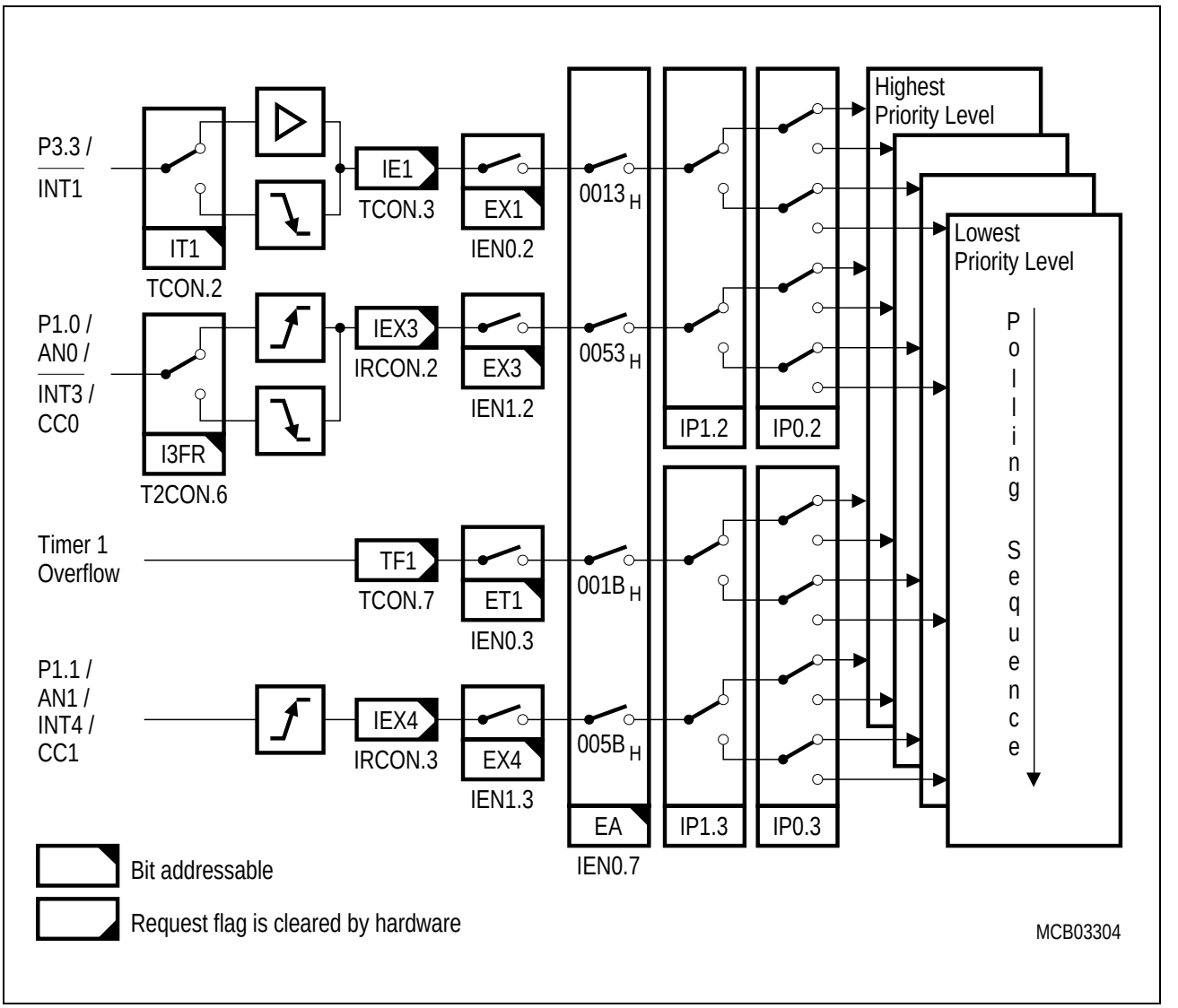


Figure 22
Interrupt Structure, Overview Part 2

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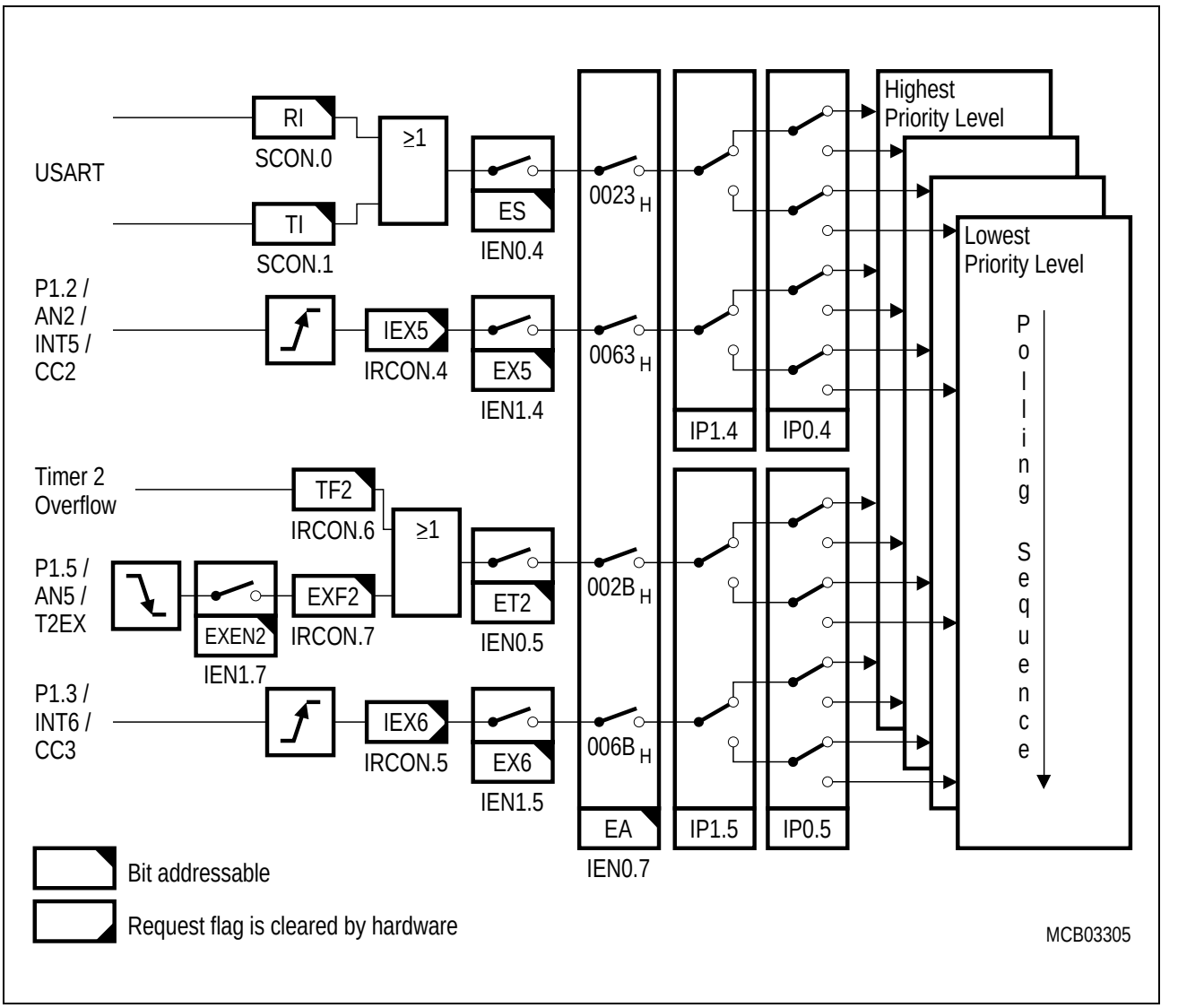


Figure 23
Interrupt Structure, Overview Part 3

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Fail Save Mechanisms

The C505 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 192 µs up to approx. 393.2 ms at 16 MHz (314.5 ms at 20 MHz).
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C505 is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ upto $f_{OSC}/192$. The system clock of the C505 is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bits of the watchdog timer can be written. **Figure 24** shows the block diagram of the watchdog timer unit.

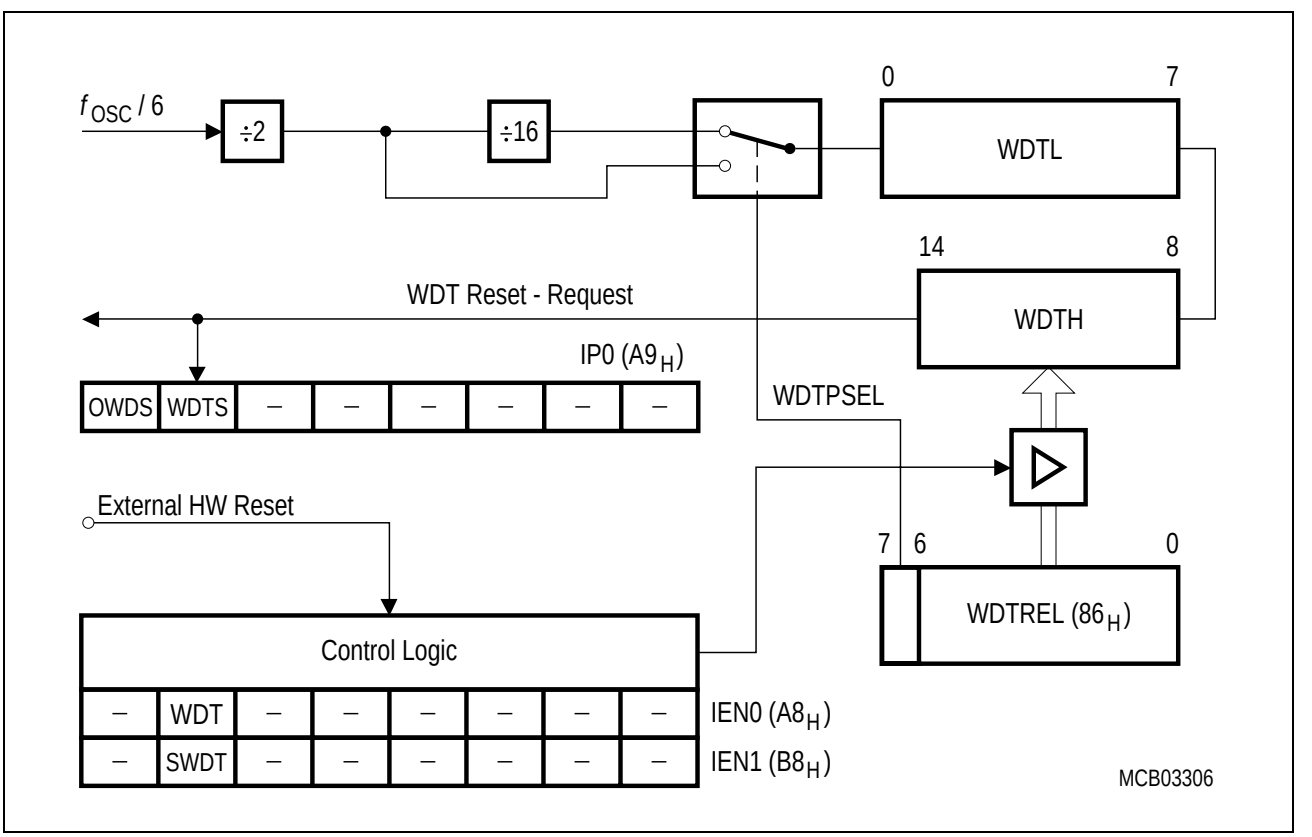


Figure 24
Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT in SFR IEN1) but it cannot be stopped during active mode of the device. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transfered to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consequtive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

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Oscillator Watchdog

The oscillator watchdog unit serves for three functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part, in order to allow the oscillator to stabilize, executes a final reset phase of typ. 1 ms; then the oscillator watchdog reset is released and the part starts program execution from address 0000_H again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the power-down mode is left by a low level at the P3.2/$\overline{\text{INT0}}$ pin or the P4.1/RXDC pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts program execution by processing a power down interrupt after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

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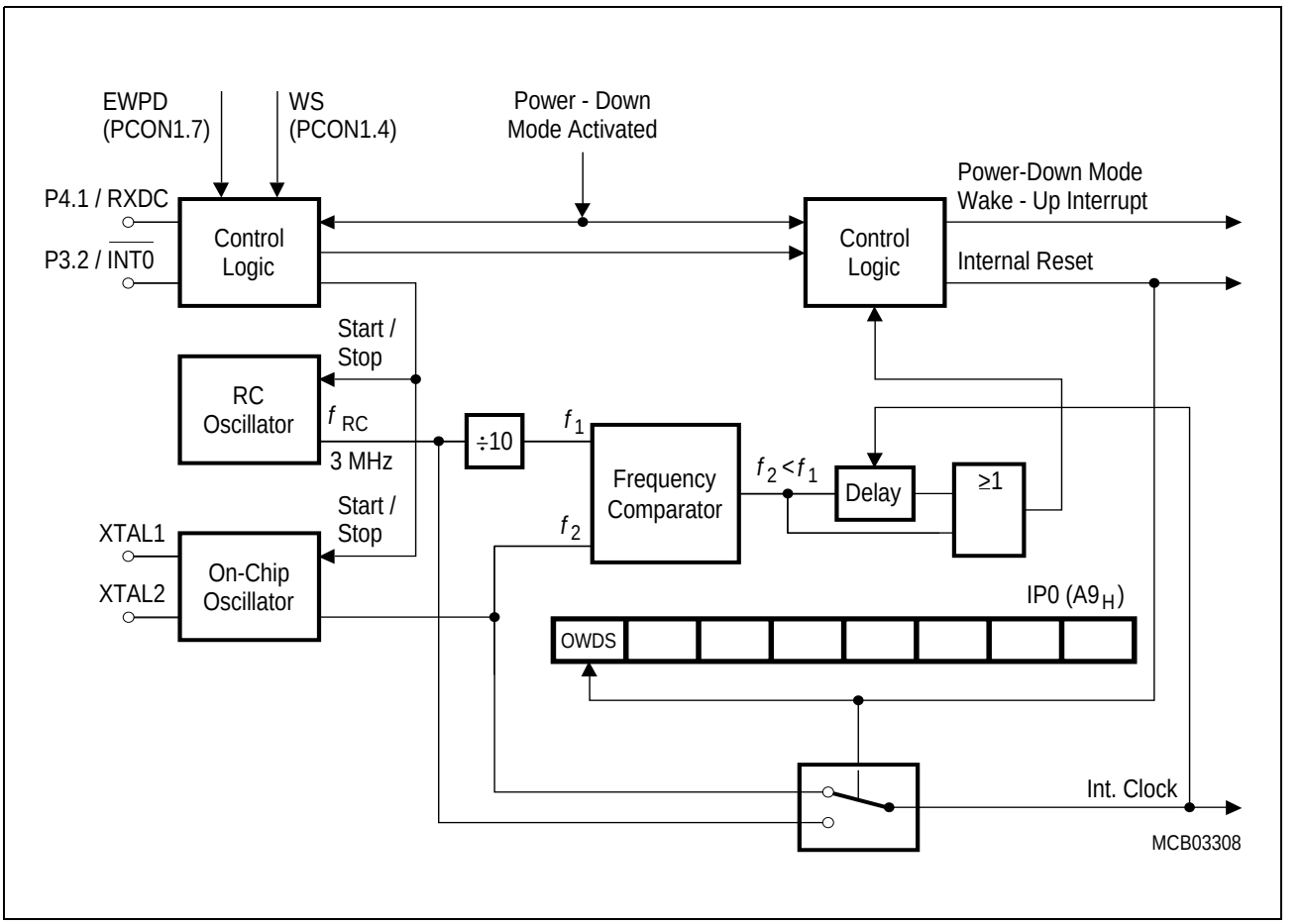


Figure 25
Functional Block Diagram of the Oscillator Watchdog

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Power Saving Modes

The C505 provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  In the idle mode the main oscillator of the C505 continues to run, but the CPU is gated off from the clock signal. All peripheral units are further provided with the clock. The CPU status is preserved in its entirety. The idle mode can be terminated by any enabled interrupt of a peripheral unit or by a hardware reset.
- **Power down mode**
  The operation of the C505 is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. Power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/$\overline{\text{INT0}}$.or P4.1/RXDC.
- **Slow down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32-th of their normal operating frequency. Slowing down the frequency significantly reduces power consumption.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated. **Table 10** gives a general overview of the entry and exit procedures of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering (Instruction Example)	Leaving by	Remarks
Idle Mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC	
Slow Down Mode	ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Oscillator frequency is reduced to 1/32 of its nominal frequency

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OTP Memory Operation (C505A-4E and C505CA-4E only)

The C505A-4E/C505CA-4E contains a 32K byte one-time programmable (OTP) program memory. With the C505A-4E/C505CA-4E fast programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected.

For programming of the device, the C505A-4E/C505CA-4E must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C505A-4E/C505CA-4E operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5V programming voltage. **Figure 26** shows the pins of the C505A-4E/C505CA-4E which are required for controlling of the OTP programming mode.

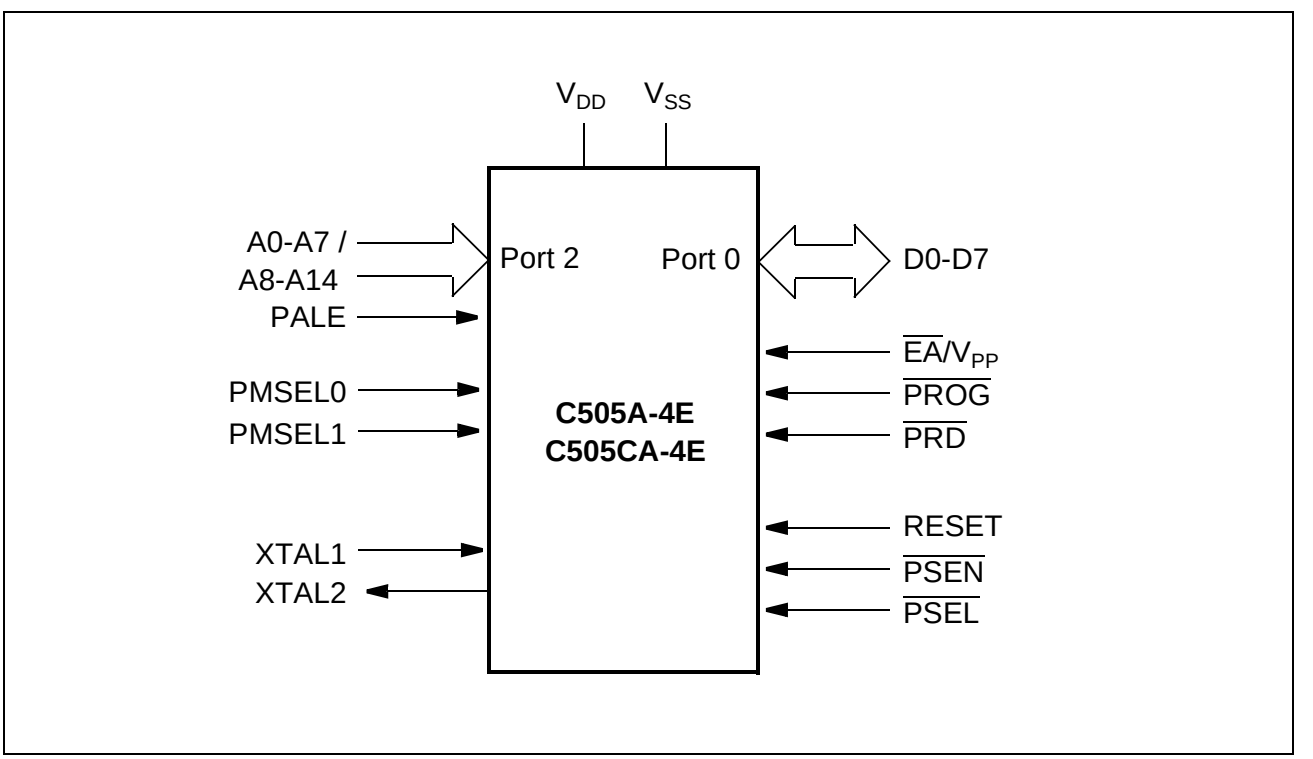


Figure 26
Programming Mode Configuration

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Pin Configuration in Programming Mode

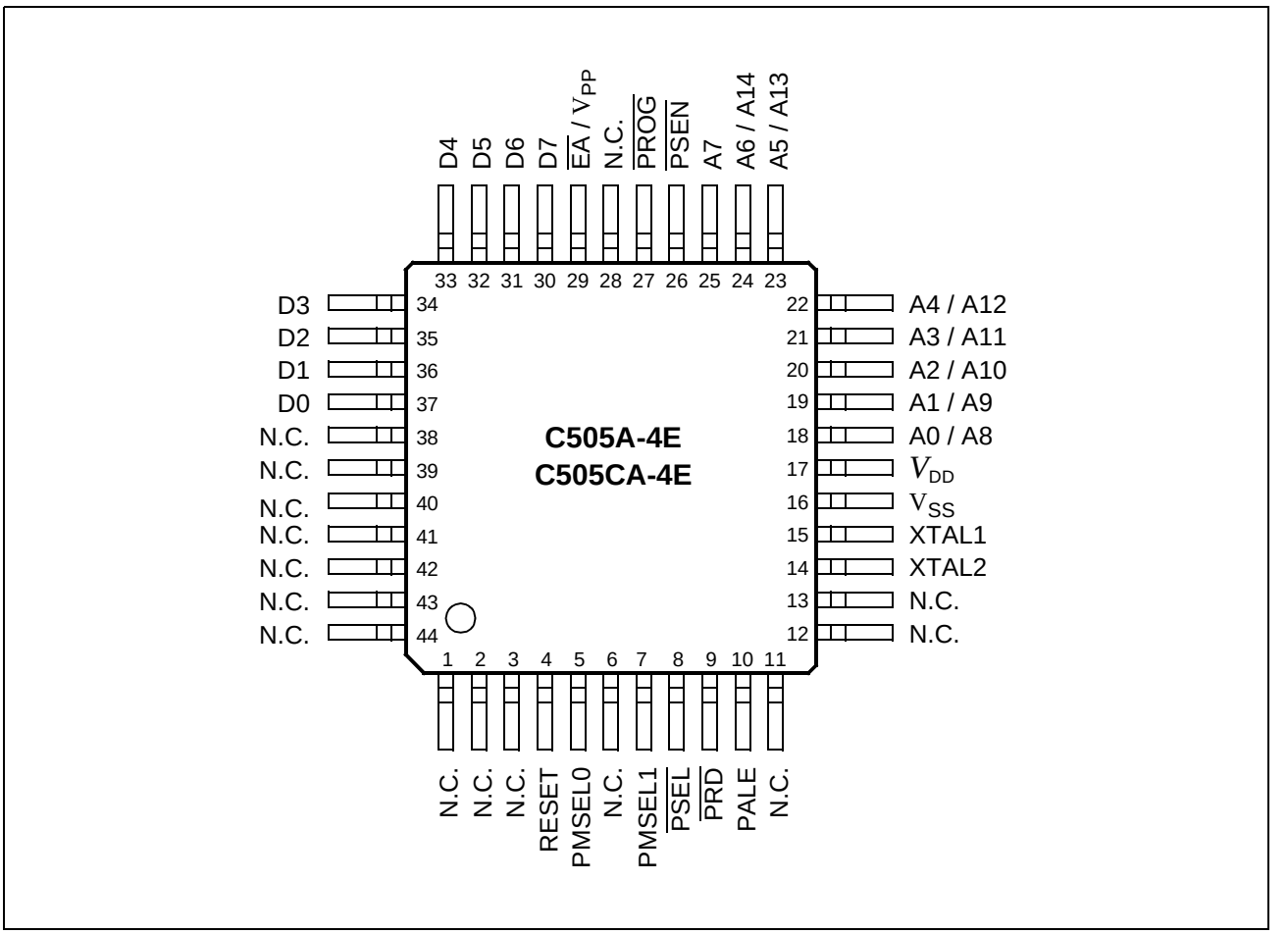


Figure 27
P-MQFP-44 Pin Configuration of the C505A-4E/C505CA-4E in Programming Mode (Top View)

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The following **Table 11** contains the functional description of all C505A-4E/C505CA-4E pins which are required for OTP memory programming.

Table 11
Pin Definitions and Functions in Programming Mode

<table>
<tr><th>Symbol</th><th>Pin Number</th><th>I/O *)</th><th>Function</th></tr>
<tr><td>RESET</td><td>4</td><td>I</td><td>Reset
This input must be at static “1“ (active) level during the whole programming mode.</td></tr>
<tr><td>PMSEL0
PMSEL1</td><td>5
7</td><td>I
I</td><td>Programming mode selection pins
These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
<table>
<tr><th>PMSEL1</th><th>PMSEL0</th><th>Access Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Read version bytes</td></tr>
<tr><td>1</td><td>0</td><td>Program/read lock bits</td></tr>
<tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{PSEL}}$</td><td>8</td><td>I</td><td>Basic programming mode select
This input is used for the basic programming mode selection and must be switched according Figure 28.</td></tr>
<tr><td>$\overline{\text{PRD}}$</td><td>9</td><td>I</td><td>Programming mode read strobe
This input is used for read access control for OTP memory read, Version Register read, and lock bit read operations.</td></tr>
<tr><td>PALE</td><td>10</td><td>I</td><td>Programming address latch enable
PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.</td></tr>
<tr><td>XTAL2</td><td>14</td><td>O</td><td>XTAL2
Output of the inverting oscillator amplifier.</td></tr>
<tr><td>XTAL1</td><td>15</td><td>I</td><td>XTAL1
Input to the oscillator amplifier.</td></tr>
<tr><td>V_{SS}</td><td>16</td><td>–</td><td>Circuit ground potential
must be applied in programming mode.</td></tr>
<tr><td>V_{DD}</td><td>17</td><td>–</td><td>Power supply terminal
must be applied in programming mode.</td></tr>
</table>

*) I = Input
O = Output

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Table 11
Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-7	18-25	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A14. A8-A14 must be latched with PALE.
$\overline{\text{PSEN}}$	26	I	**Program store enable** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	27	I	**Programming mode write strobe** This input is used in programming mode as a write strobe for OTP memory program, and lock bit write operations During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	29	–	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at V_{IH} high level. This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
D7-0	30-37	I/O	**Data lines 0-7** During programming mode, data bytes are transferred via the bidirectional port 0 data lines.
N.C.	1-3, 6, 11-13, 28, 38-44	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

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Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 28**.

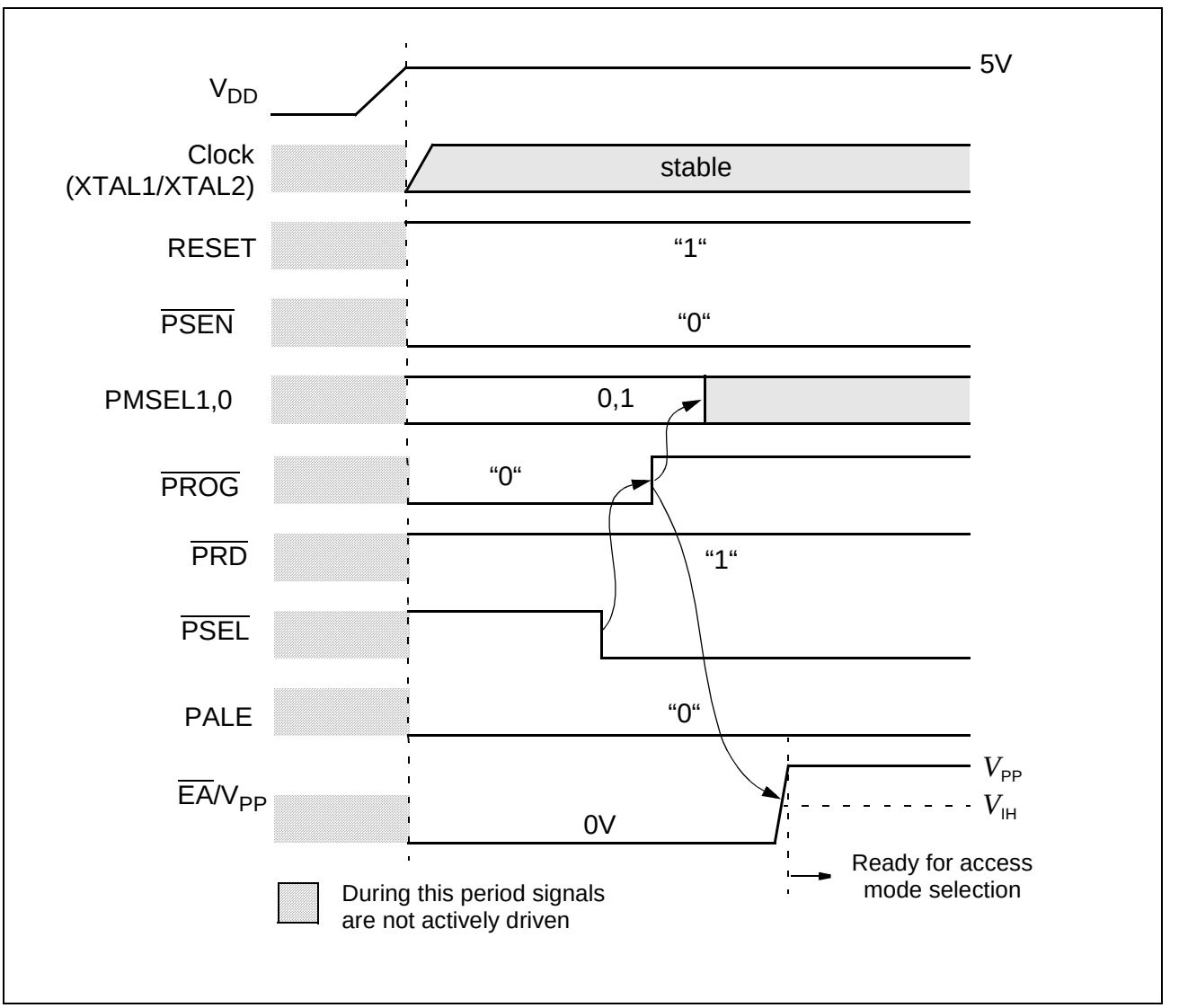


Figure 28
Basic Programming Mode Selection

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Table 12
Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-14	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1,D0 see Table 13
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of sign. byte	D0-7

Lock Bits Programming / Read

The C505A-4E/C505CA-4E has two programmable lock bits which, when programmed according to **Table 13**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 13
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	D0		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C505A-4E/C505CA-4E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C505A-4E/C505CA-4E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible using the ROM/OTP verification mode 2 for protection level 1. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C505A-4E/ C505CA-4E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

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Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	– 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	– 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition		– 10	10	mA	–
Absolute sum of all input currents during overload condition			| 100 mA |	mA	–
Power dissipation	P_{DISS}		1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

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Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode, $f_{osc\ max}$ = 20 MHz
		2	5.5	V	PowerDown mode
Ground voltage	V_{SS}	0		V	Reference voltage
Ambient temperature				°C	–
SAB-C505	T_A	0	70		
SAF-C505	T_A	-40	85		
SAH-C505	T_A	-40	110		
SAK-C505	T_A	-40	125		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND} -0.2	V_{AREF} +0.2	V	–
XTAL clock	f_{osc}	2	20 (with 50% duty cycle)	MHz	1)

1) For the extended temperature range -40 °C to 110 °C (SAH) and -40 °C to 125 °C (SAK), the devices C505-2R, C505-L, C505C-2R and C505C-L have the max. operating frequency of 16MHz with 50% clock duty cycle.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C505 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the C505 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective characteristics to the C505.

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DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except $\overline{EA}$, RESET $\overline{EA}$ pin RESET pin	 V_{IL} V_{IL1} V_{IL2}	 – 0.5 – 0.5 – 0.5	 0.2 V_{DD} - 0.1 0.2 V_{DD} - 0.3 0.2 V_{DD} + 0.1	 V V V	 – – –
Input high voltages all except XTAL1, RESET XTAL1 pin RESET pin	 V_{IH} V_{IH1} V_{IH2}	 0.2 V_{DD} + 0.9 0.7 V_{DD} 0.6 V_{DD}	 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5	 V V V	 – – –
Output low voltages Ports 1, 2, 3, 4 Port 0, ALE, $\overline{PSEN}$	 V_{OL} V_{OL1}	 – –	 0.45 0.45	 V V	 I_{OL} = 1.6 mA [1] I_{OL} = 3.2 mA [1]
Output high voltages Ports 1, 2, 3, 4 Port 0 in external bus mode, ALE, $\overline{PSEN}$	 V_{OH} V_{OH2}	 2.4 0.9 V_{DD} 2.4 0.9 V_{DD}	 – – – –	 V V V V	 I_{OH} = – 80 µA I_{OH} = – 10 µA I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
Logic 0 input current Ports 1, 2, 3, 4	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current Ports 1, 2, 3, 4	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current Port 0, AN0-7 (Port 1), $\overline{EA}$	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{DD}
Input high current to RESET	I_{IH}	5	100	µA	[14] 0.6 V_{DD} < V_{IN} < V_{DD}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[3] [4]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5% [5]
Supply current at $\overline{EA}$/V_{PP}			30	mA	[6]

Notes see **Page 60**

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Power Supply Currents

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[12]	max.[13]		
C505 / C505C	Active Mode	12 MHz 20 MHz	I_{DD} I_{DD}	19.3 31.3	27.0 39	mA	[7]
	Idle Mode	12 MHz 20 MHz	I_{DD} I_{DD}	10.3 16.2	13.0 21.0	mA	[8]
	Active Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.9 4.8	5.5 7.5	mA	[9]
	Idle Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.2 4.0	5.0 7.0	mA	[10]
	Power down mode		I_{PD}	10	50	µA	V_{DD} = 2..5.5 V [11]
C505A-4E /C505CA-4E	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	28.7 35.2	30.7 37.6	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	14.9 17.7	15.9 18.9	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	9.9 12.3	12.8 15.6	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.1 6.3	5.6 6.8	mA	[10]
	Power down mode		I_{PD}	5.6	20	µA	V_{DD} = 2..5.5 V [11]
C505A-4R / C505CA-4R /C505A-2R / C505CA-2R /C505A-L / C505CA-L	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	22.8 27.6	29.2 35.3	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	12.7 15.0	16.3 19.3	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	6.6 7.3	8.2 9.3	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.0 5.3	5.9 6.5	mA	[10]
	Power down mode		I_{PD}	5.3	30	µA	V_{DD} = 2..5.5 V [11]

Notes see **Page 60**

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Note:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.

3) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input currents on all port pins may not exceed 50 mA. The supply voltage V_{DD} and V_{SS} must remain within the specified limits.

4) Not 100% tested, guaranteed by design characterization.

5) Only valid for C505A-4E and C505CA-4E.

6) Only valid for C505A-4E and C505CA-4E in programming mode.

7) I_{DD} (active mode) is measured with:
XTAL1 driven with t_R , t_F = 5 ns, 50% duty cycle , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port 0 = RESET =V_{DD} ; all other pins are disconnected.

8) I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R , t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{DD} ; all other pins are disconnected; the microcontroller is put into idle mode by software;

9) I_{DD} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R , t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; all other pins are disconnected; the microcontroller is put into slow-down mode by software;

10) I_{DD} (idle mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R , t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{DD} ; all other pins are disconnected; the microcontroller is put into idle mode with slow-down enabled by software;

11) I_{PD} (power-down mode) is measured under following conditions:
Port 0 = $\overline{EA}$ = V_{DD} ; RESET =V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; V_{AGND} = V_{SS} ; V_{AREF} = V_{DD} ;
all other pins are disconnected.

12) The typical I_{DD} values are periodically measured at T_A = +25 °C but not 100% tested.

13) The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or -40 °C and V_{DD} = 5.5 V)

14) The values are valid for C505CA-4R, C505CA-2R, C505CA-L, C505A-4R, C505A-2R and C505A-L only.

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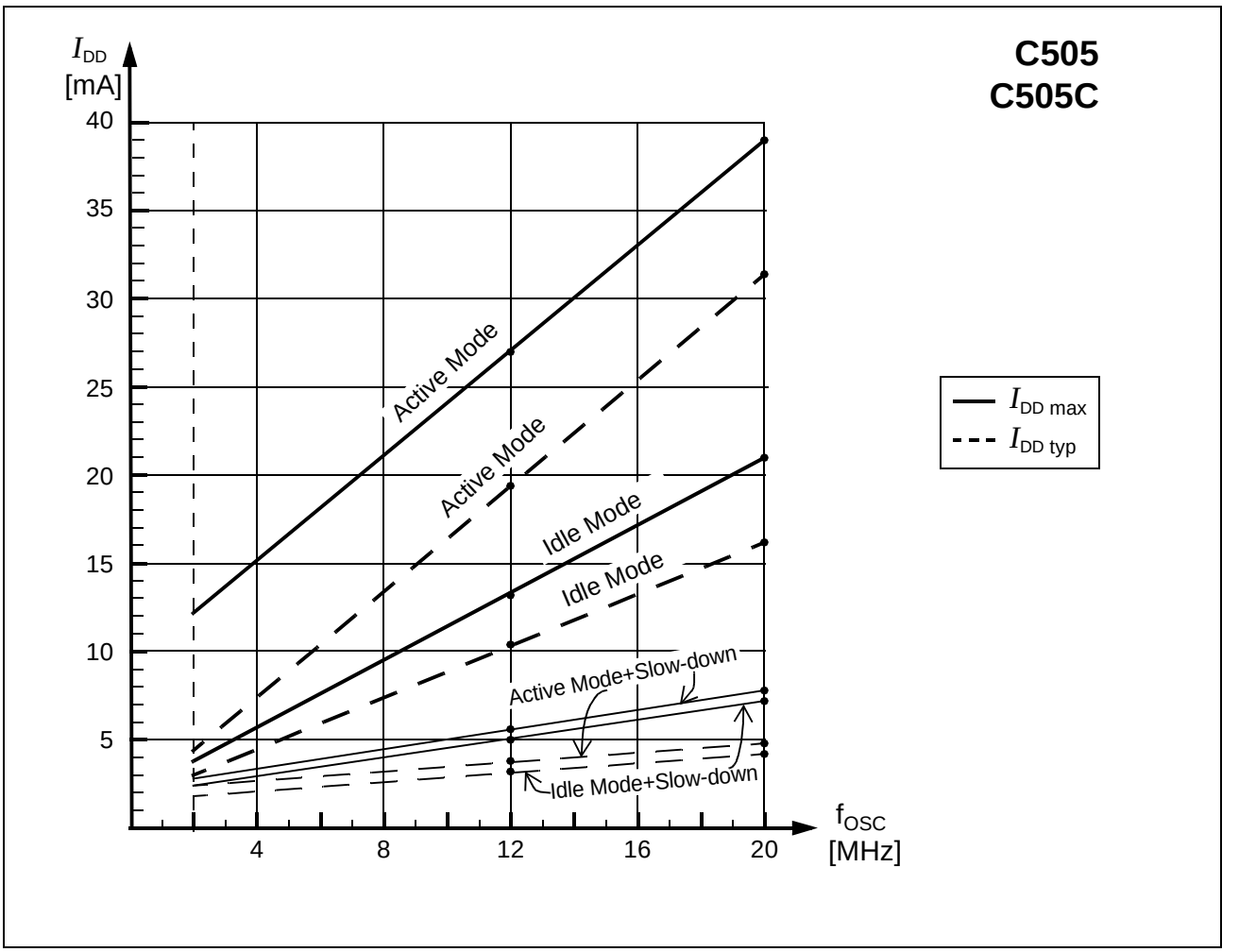


Figure 29
I_{DD} Diagram of C505 and C505C

C505/C505C : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.5 * f_{OSC} + 1.3$ $1.5 * f_{OSC} + 9.0$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.74 * f_{OSC} + 1.4$ $1.0 * f_{OSC} + 1.0$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.11 * f_{OSC} + 2.6$ $0.25 * f_{OSC} + 2.5$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.1 * f_{OSC} + 2.0$ $0.25 * f_{OSC} + 2.0$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

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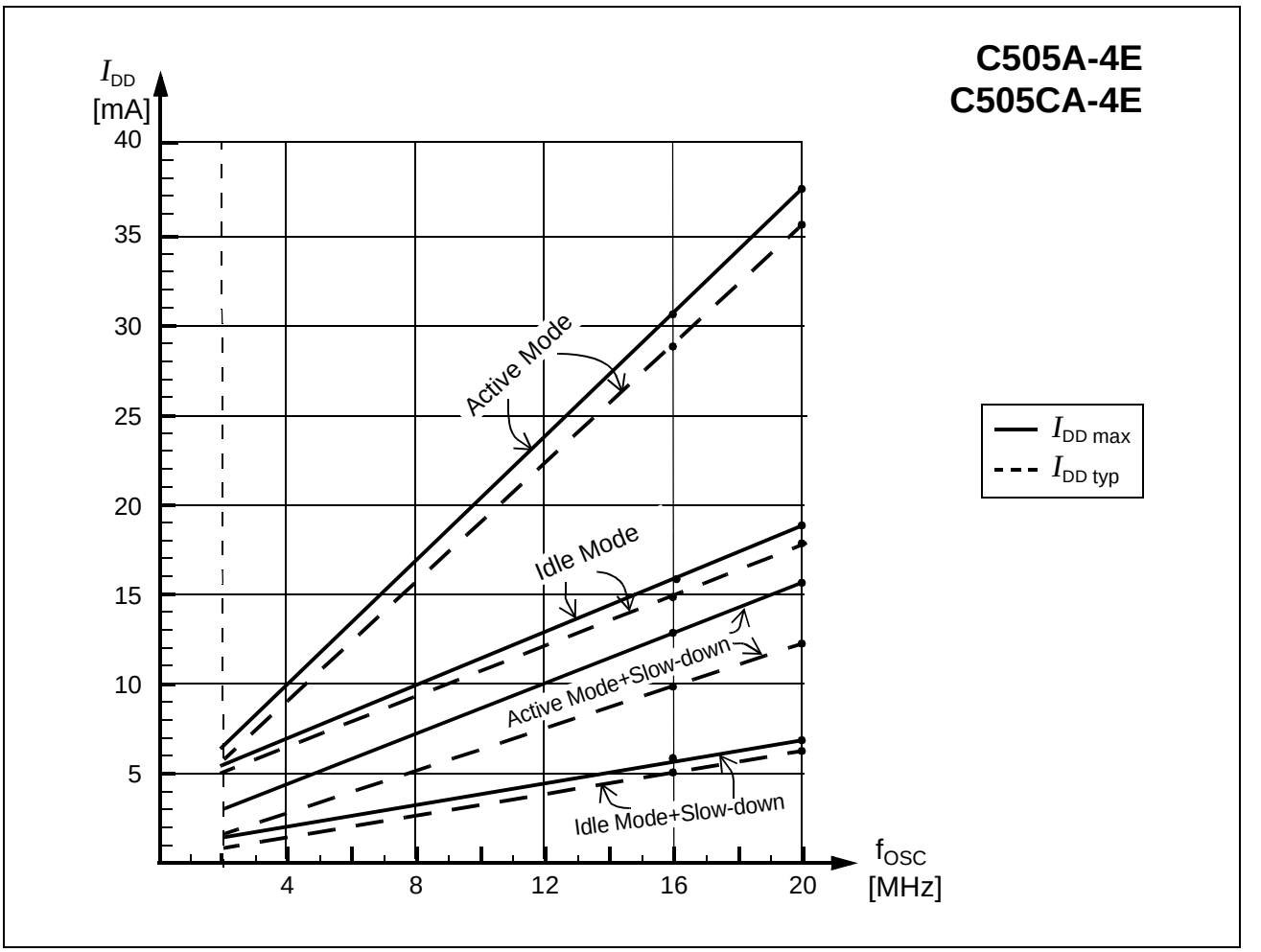


Figure 30
I_{DD} Diagram of C505A-4E and C505CA-4E

C505A-4E/C505CA-4E : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.63 * f_{OSC} + 2.6$ $1.74 * f_{OSC} + 2.8$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.69 * f_{OSC} + 3.9$ $0.74 * f_{OSC} + 4.1$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.6 * f_{OSC} + 0.3$ $0.7 * f_{OSC} + 1.6$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.3 * f_{OSC} + 0.3$ $0.3 * f_{OSC} + 0.8$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

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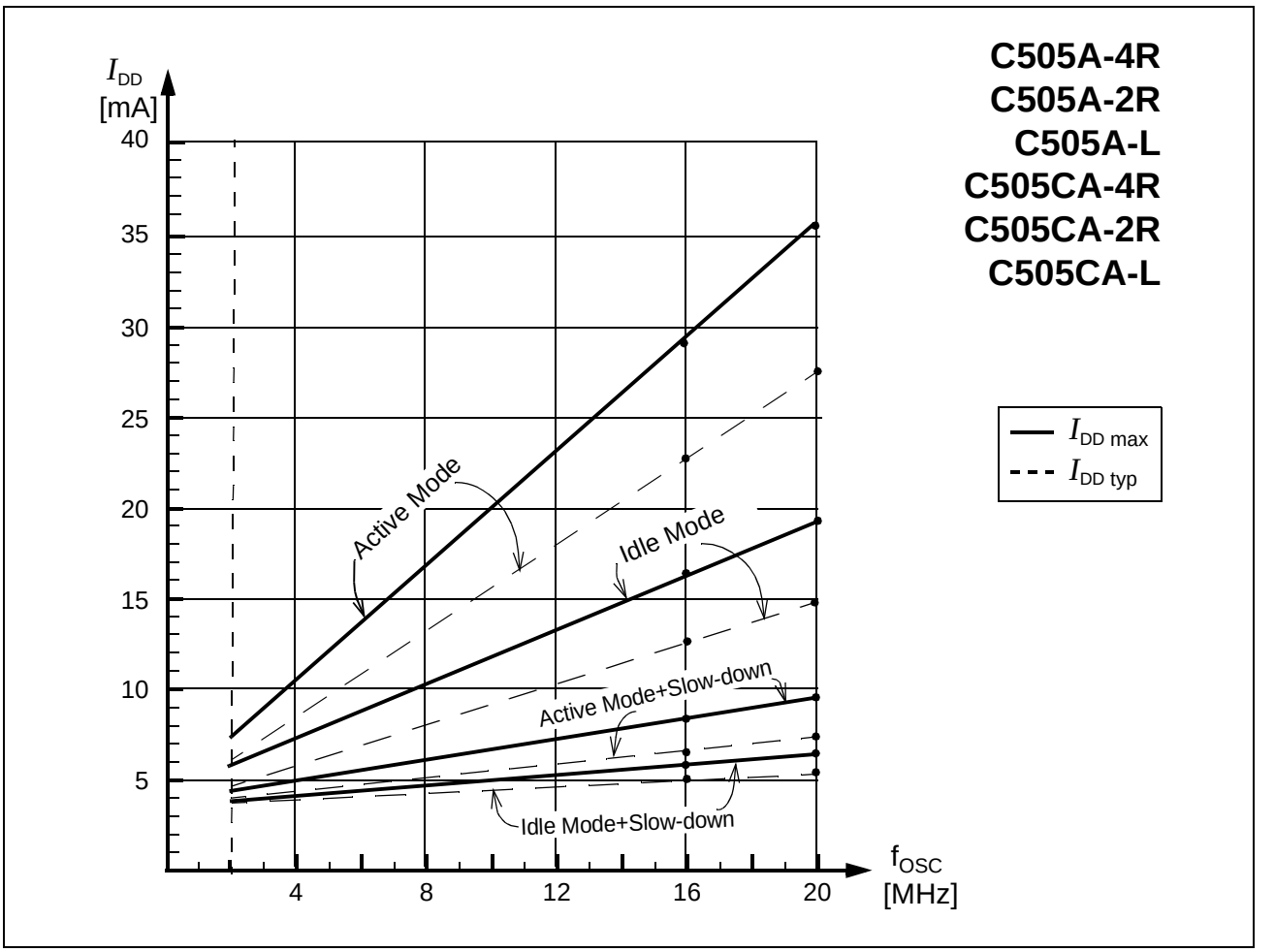


Figure 31
I_{DD} Diagram of C505A-4R/C505A-2R/C505A-L/C505CA-4R/C505CA-2R/C505CA-L

C505A-4R/C505A-2R/C505A-L/C505CA-4R/C505CA-2R/C505CA-L :
Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	1.19 * f_{OSC} + 3.77 1.54 * f_{OSC} + 4.47
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	0.57 * f_{OSC} + 3.55 0.75 * f_{OSC} + 4.26
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	0.18 * f_{OSC} + 3.74 0.28 * f_{OSC} + 3.67
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	0.07 * f_{OSC} + 3.91 0.14 * f_{OSC} + 3.64

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

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A/D Converter Characteristics of C505 and C505C

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND} - 0.2	V_{AREF} + 0.2	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	320 x t_{IN} 160 x t_{IN} 80 x t_{IN} 40 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{DD}-0.5V 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 500 - 1	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 1	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	320 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	160 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	80 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	40 x t_{IN}

Further timing conditions : t_{ADC} min = 800 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

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Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} (max.) is tested at $-40 \le T_A \le 125$ °C ; $V_{DD} \le 5.5$ V; $V_{AREF} \le V_{DD} + 0.1$ V and $V_{SS} \le V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

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A/D Converter Characteristics of C505A and C505CA

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{DD}-0.5V 4)
		–	± 4	LSB	V_{SS} < V_{AIN} < V_{DD}+0.5V V_{DD} - 0.5 V < V_{AIN} < V_{DD} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

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Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

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AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} -15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} -15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP - 50	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	TCL_{Lmin} -15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} -15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}- 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} -55	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

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AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	158	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	158	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	100	–	2 CLP+ TCL_{Hmin} - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP + TCL_{Hmin} -75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	73	103	CLP + TCL_{Lmin} - 15	CLP+ TCL_{Lmin}+ 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	95	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	TCL_{Hmin} - 15	TCL_{Hmin} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	TCL_{Hmin} - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

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AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 16 MHz Duty Cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 16 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	62.5	62.5	62.5	500	ns
High time	TCL_H	25	–	25	CLP - TCL_L	ns
Low time	TCL_L	25	–	25	CLP - TCL_H	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 - 25 / CLP	–
Clock cycle	TCL	25	37.5	CLP * DC_{min}	CLP * DC_{max}	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

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AC Characteristics (20 MHz, 0.5 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	CLP/2 - 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	CLP/2 - 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	55	–	2 CLP - 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	CLP/2 - 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	3/2 CLP - 15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	25	–	3/2 CLP - 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	CLP/2 - 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	CLP/2 - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	65	–	5/2 CLP - 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	- 5	–	- 5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

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AC Characteristics (20 MHz, 0.5 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	35	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5/2 CLP- 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9/2 CLP - 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3/2 CLP - 15	3/2 CLP + 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	CLP/2 - 15	CLP/2 + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	CLP/2 - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7/2 CLP - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	CLP/2 - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 2 MHz to 20 MHz		
		min.	max.	
Oscillator period	CLP	50	500	ns
High time	TCL_H	15	$CLP-TCL_L$	ns
Low time	TCL_L	15	$CLP-TCL_H$	ns
Rise time	t_R	–	10	ns
Fall time	t_F	–	10	ns
Oscillator duty cycle	DC	0.5	0.5	–

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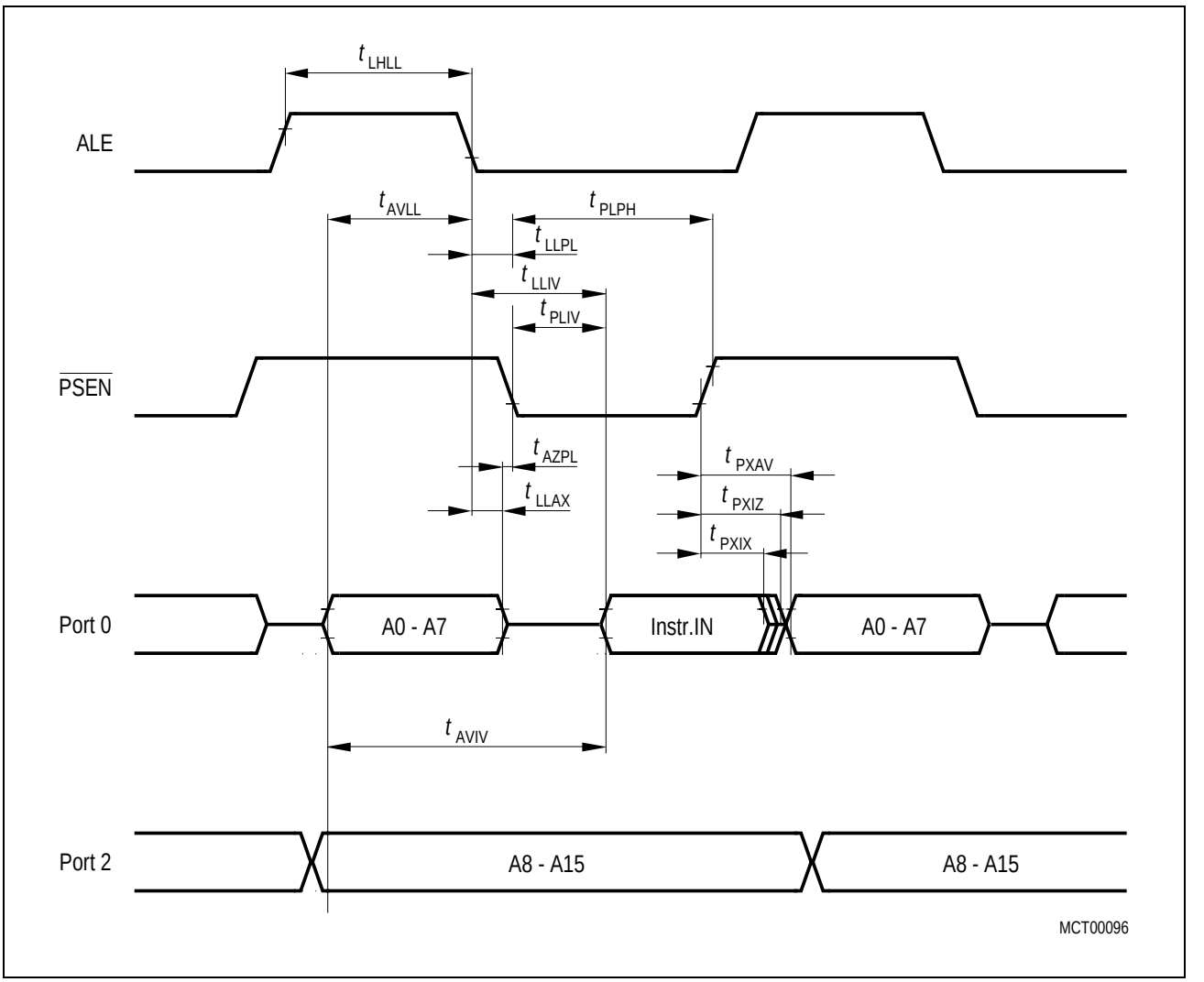


Figure 32
Program Memory Read Cycle

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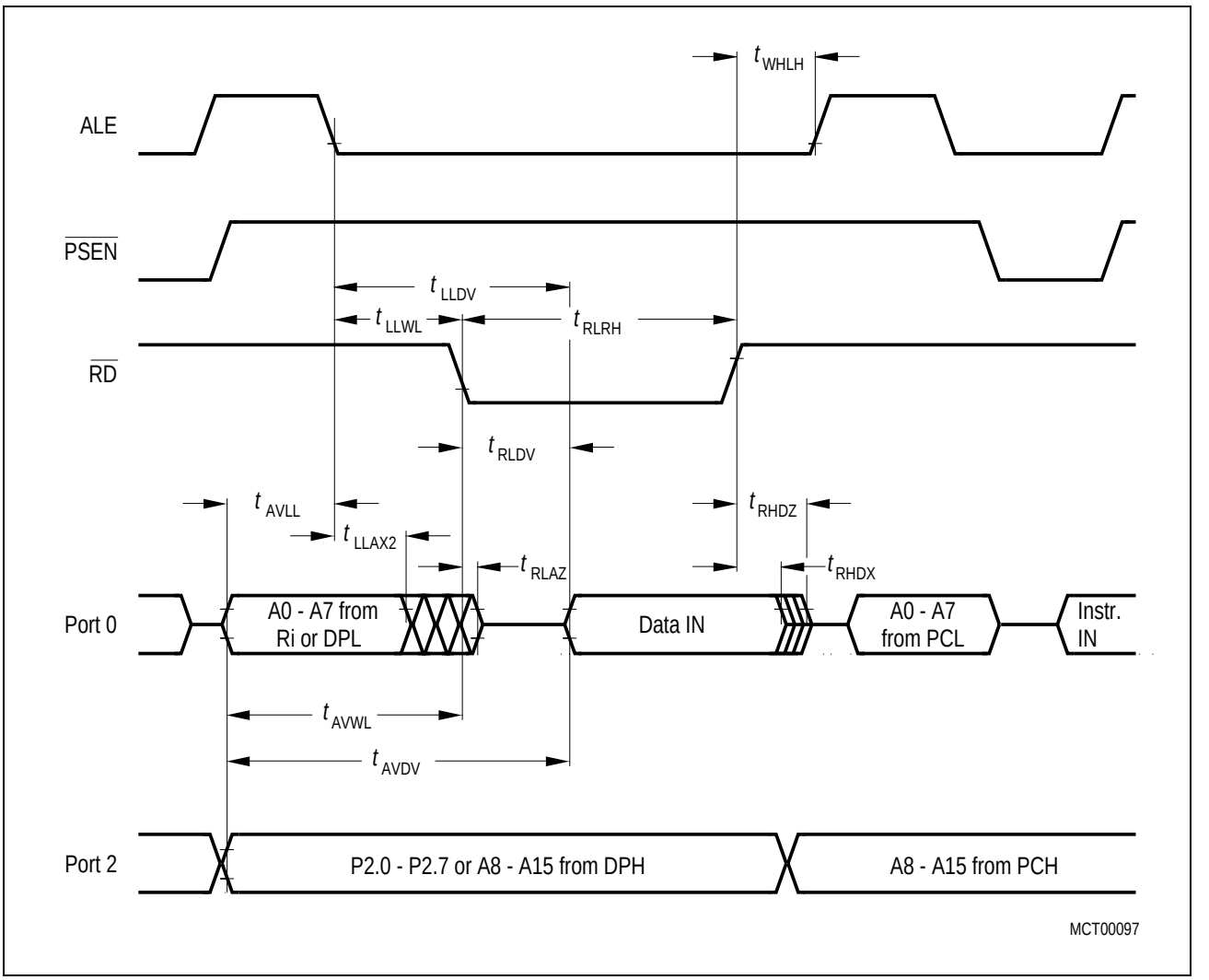


Figure 33
Data Memory Read Cycle

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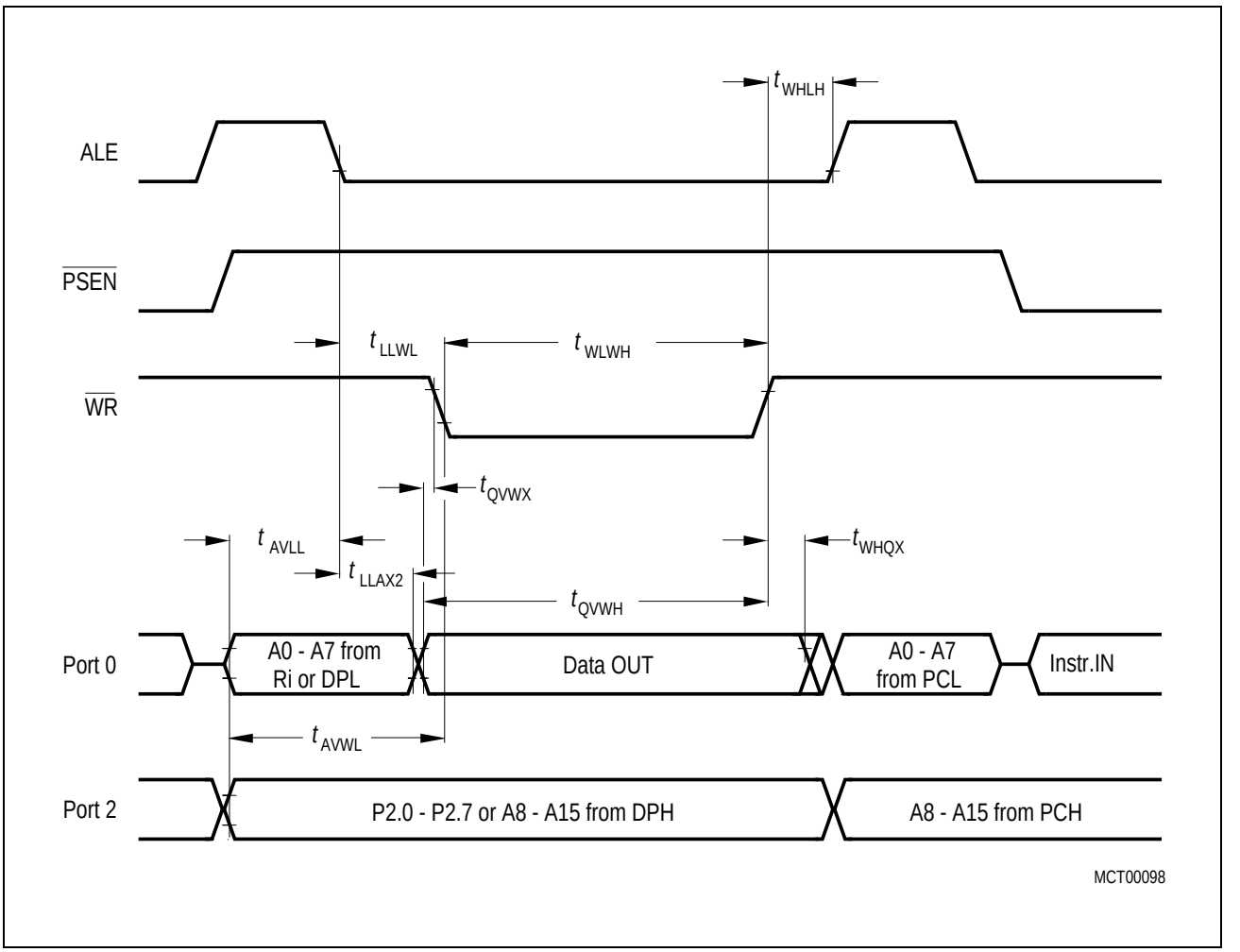


Figure 34
Data Memory Write Cycle

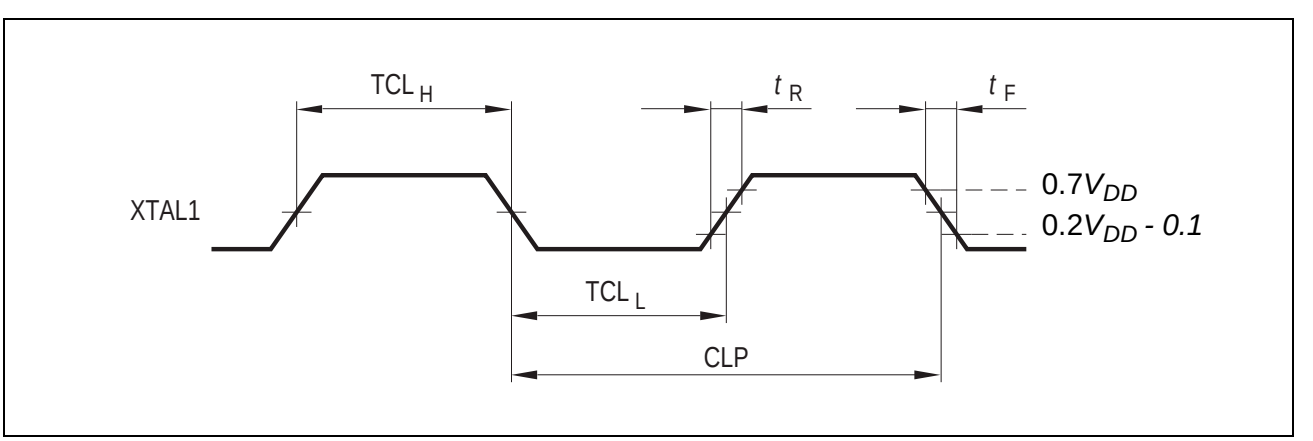


Figure 35
External Clock Drive on XTAL1

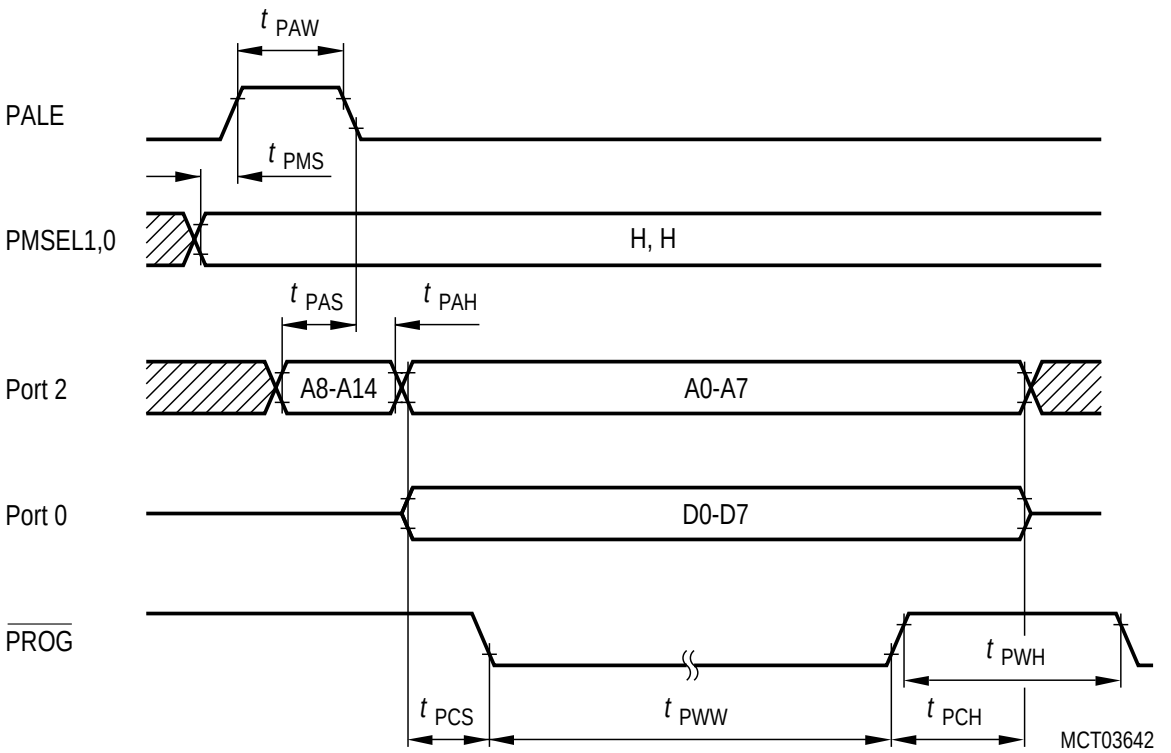
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AC Characteristics of Programming Mode (C505A-4E and C505CA-4E only)

V_{DD} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to PALE rising edge	t_{PMS}	10	–	
Address setup to PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	83.3	500	ns

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Notes: $\overline{PRD}$ must be high during a programming write cycle.

Figure 36
Programming Code Byte - Write Cycle Timing

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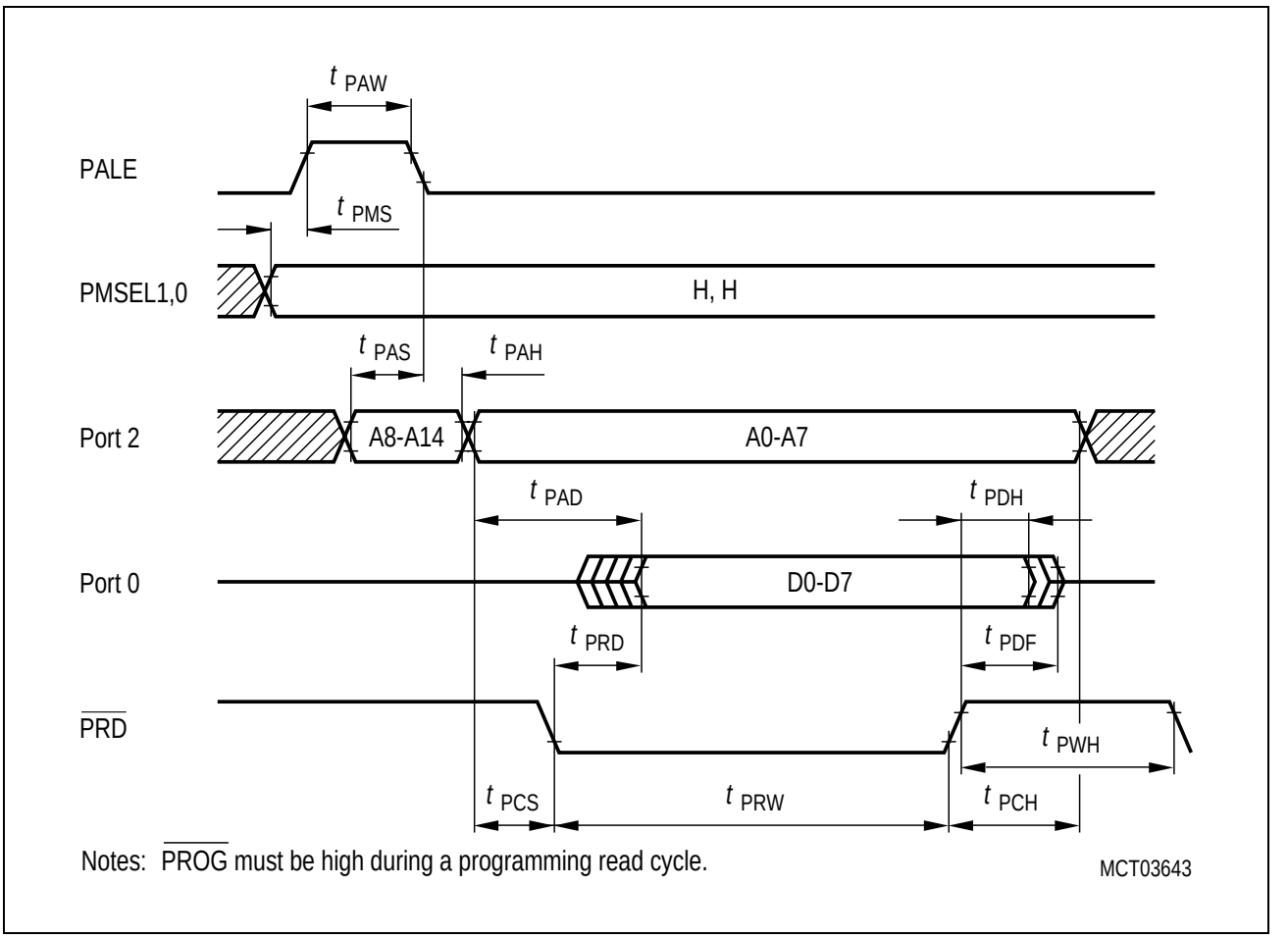
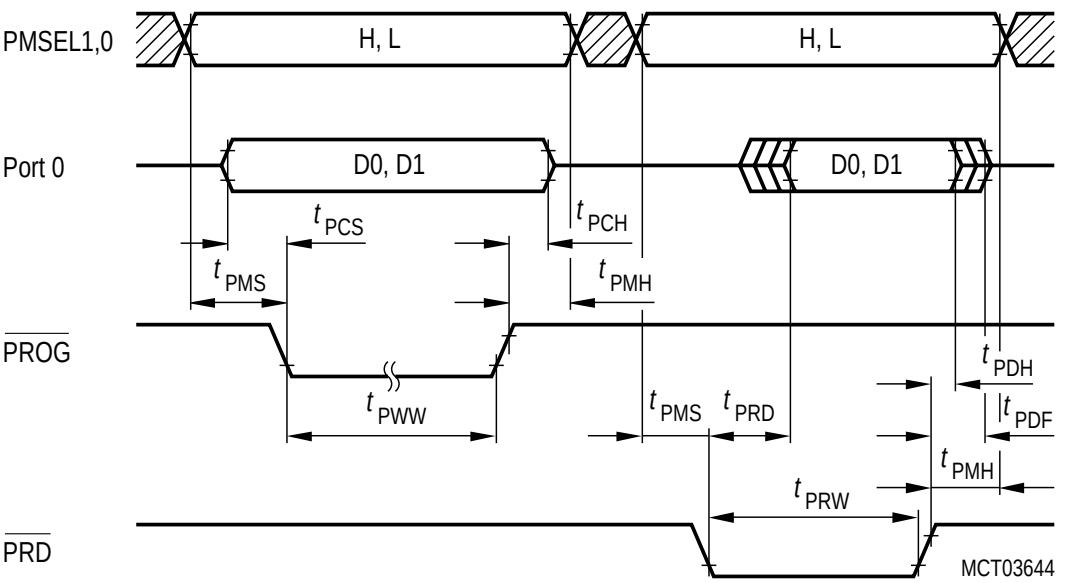


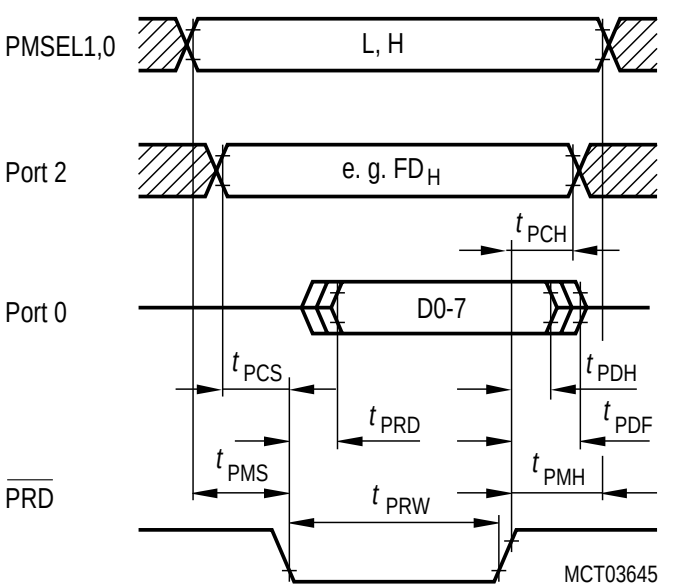
Figure 37
Verify Code Byte - Read Cycle Timing

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Note: PALE should be low during a lock bit read / write cycle.

Figure 38
Lock Bit Access Timing



Note: $\overline{\text{PROG}}$ must be high during a programming read cycle.

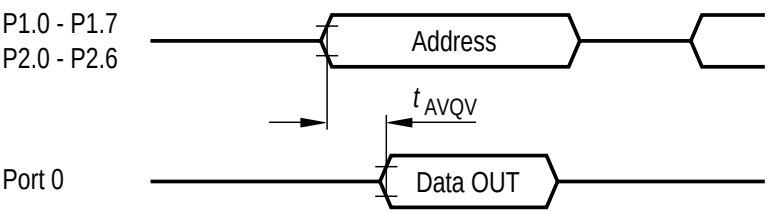
Figure 39
Version Byte Read Timing

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ROM/OTP Verification Characteristics for C505

ROM Verification Mode 1 (C505(C)(A)-2R and C505(C)A-4R only)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	5 CLP	ns



Address: P1.0 - P1.7 = A0 - A7
P2.0 - P2.6 = A8 - A14
Data: P0.0 - P0.7 = D0 - D7

Inputs: P2.7, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IH2}

Note: P2.6 should be connected to V_{SS} for C505(C)(A)-2R

Figure 40
ROM Verification Mode 1

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ROM/OTP Verification Characteristics for C505 (cont'd)

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz

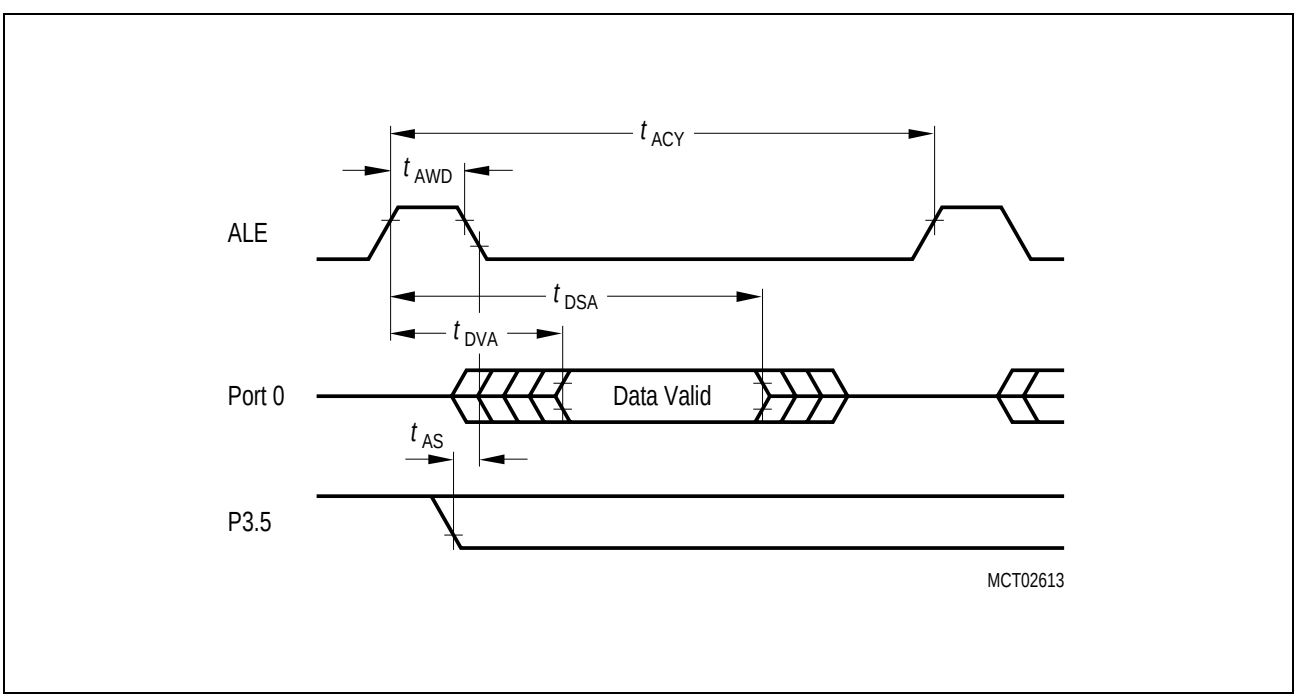
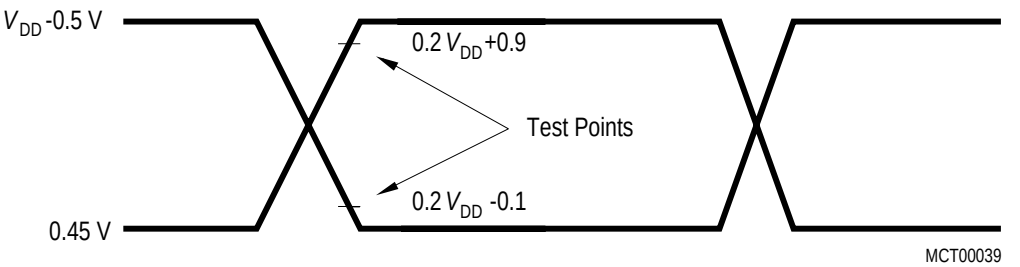


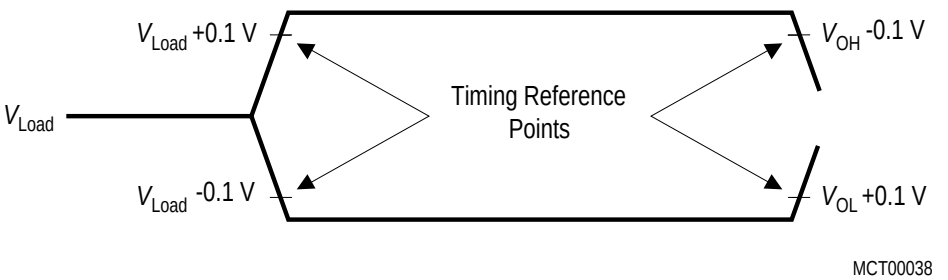
Figure 41
ROM/OTP Verification Mode 2

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AC Inputs during testing are driven at V_{DD} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 42
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 43
AC Testing : Float Waveforms

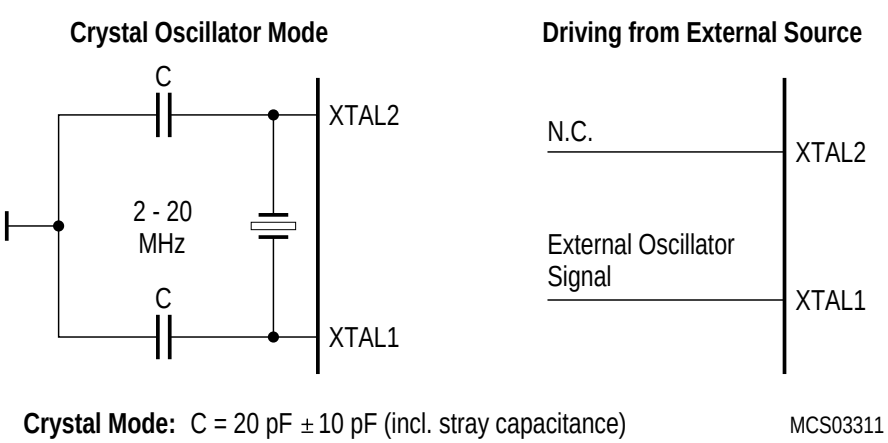


Figure 44
Recommended Oscillator Circuits for Crystal Oscillator

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P-MQFP-44-2 (SMD)
(Plastic Metric Quad Flat Package)

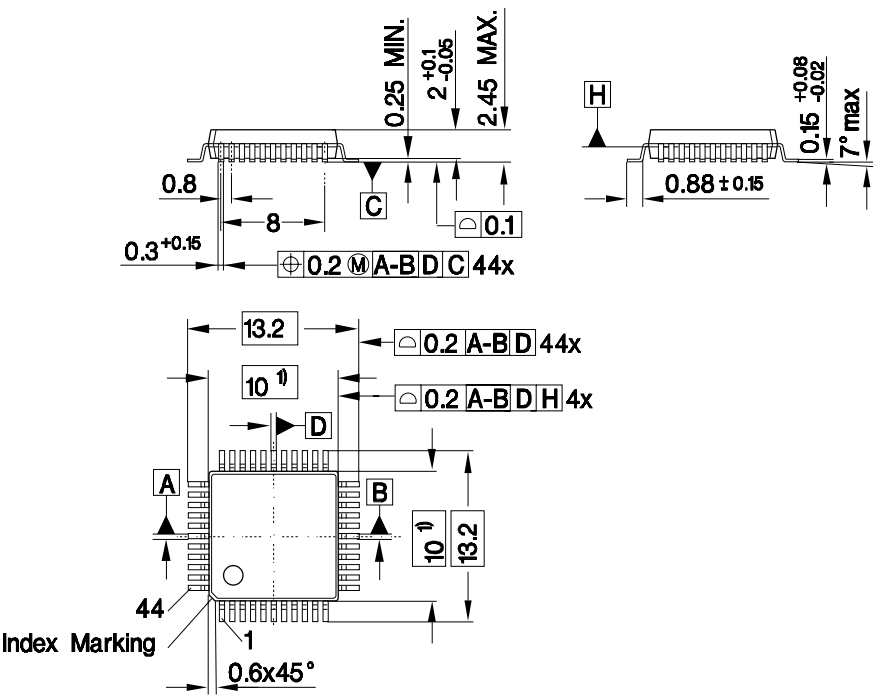


Figure 45
P-MQFP-44 Package Outline

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

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