

MOSFET – Power, Single N-Channel

40 V, 83 A, 4.2 mΩ

NVD5C454N

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | | Value | Unit |
|-------------------|--|---|---------------------------|------|
| V_{DSS} | Drain-to-Source Voltage | | 40 | V |
| V_{GS} | Gate-to-Source Voltage | | ± 20 | V |
| I_D | Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3) | | $T_C = 25^\circ\text{C}$ | 82 |
| | | | $T_C = 100^\circ\text{C}$ | 58 |
| P_D | Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | 56 |
| | | | $T_C = 100^\circ\text{C}$ | 28 |
| I_D | Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3) | Steady State | $T_A = 25^\circ\text{C}$ | 19 |
| | | | $T_A = 100^\circ\text{C}$ | 14 |
| P_D | Power Dissipation $R_{\theta JA}$ (Notes 1 & 2) | Steady State | $T_A = 25^\circ\text{C}$ | 3.1 |
| | | | $T_A = 100^\circ\text{C}$ | 1.5 |
| I_{DM} | Pulsed Drain Current | $T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$ | 446 | A |
| T_J , T_{stg} | Operating Junction and Storage Temperature | | -55 to 175 | °C |
| I_S | Source Current (Body Diode) | | 46 | A |
| E_{AS} | Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $I_{L(pk)} = 8.3 \text{ A}$) | | 205 | mJ |
| T_L | Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | 260 | °C |

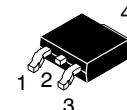
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

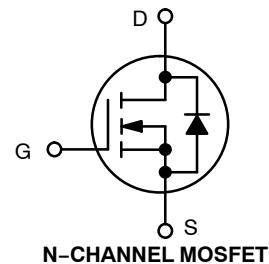
| Symbol | Parameter | Value | Unit |
|-----------------|---|-------|------|
| $R_{\theta JC}$ | Junction-to-Case (Drain) (Note 1) | 2.7 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient – Steady State (Note 2) | 48.4 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

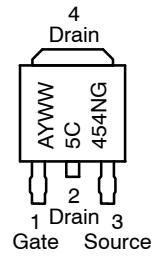
| $V_{(BR)DSS}$ | $R_{DS(on)}$ | I_D |
|---------------|---------------|-------|
| 40 V | 4.2 mΩ @ 10 V | 83 A |



DPAK
CASE 369C
STYLE 2



MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
 Y = Year
 WW = Work Week
 5C454N = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NVD5C454N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|------------------------------------|---|--|------------------------|----|-----|-------|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 250 μA | 40 | – | – | V |
| V _{(BR)DSS/T_J} | Drain-to-Source Breakdown Voltage Temperature Coefficient | | – | 15 | | mV/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{GS} = 0 V, V _{DS} = 40 V | T _J = 25°C | – | 10 | μA |
| | | | T _J = 125°C | – | 250 | |
| I _{GSS} | Gate-to-Source Leakage Current | V _{DS} = 0 V, V _{GS} = 20 V | – | – | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-----------------------------------|--|--|-----|-----|-----|-------|
| V _{GS(TH)} | Gate Threshold Voltage | V _{GS} = V _{DS} , I _D = 70 μA | 2.0 | – | 4.0 | V |
| V _{GS(TH)/T_J} | Negative Threshold Temperature Coefficient | | – | 6.9 | – | mV/°C |
| R _{DS(on)} | Drain-to-Source On Resistance | V _{GS} = 10 V, I _D = 40 A | – | 3.6 | 4.2 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} = 3 V, I _D = 40 A | – | 80 | – | S |

CHARGES, CAPACITANCES AND GATE RESISTANCES

| | | | | | | |
|---------------------|------------------------------|--|---|------|---|----|
| C _{iss} | Input Capacitance | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | – | 1900 | – | pF |
| C _{oss} | Output Capacitance | | – | 950 | – | |
| C _{rss} | Reverse Transfer Capacitance | | – | 48 | – | |
| Q _{G(TOT)} | Total Gate Charge | V _{GS} = 10 V, V _{DS} = 32 V, I _D = 40 A | – | 32 | – | nC |
| Q _{G(TH)} | Threshold Gate Charge | | – | 5.7 | – | |
| Q _{GS} | Gate-to-Source Charge | | – | 9.5 | – | |
| Q _{GD} | Gate-to-Drain Charge | | – | 6.6 | – | |
| V _{GP} | Plateau Voltage | | – | 4.8 | – | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|---------------------|--|---|----|---|----|
| t _{d(on)} | Turn-On Delay Time | V _{GS} = 10 V, V _{DS} = 32 V, I _D = 40 A, R _G = 2.5 Ω | – | 11 | – | ns |
| t _r | Rise Time | | – | 47 | – | |
| t _{d(off)} | Turn-Off Delay Time | | – | 24 | – | |
| t _f | Fall Time | | – | 8 | – | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-----------------|-----------------------|---|------------------------|----|-----|-----|---|
| V _{SD} | Forward Diode Voltage | V _{GS} = 0 V, I _S = 40 A | T _J = 25°C | – | 0.9 | 1.2 | V |
| | | | T _J = 125°C | – | 0.8 | – | |
| t _{RR} | Reverse Recovery Time | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 40 A | – | 45 | – | ns | |
| | | | – | 24 | – | | |
| | | | – | 21 | – | | |
| | | | – | 20 | – | | |
| | | | – | – | – | nC | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

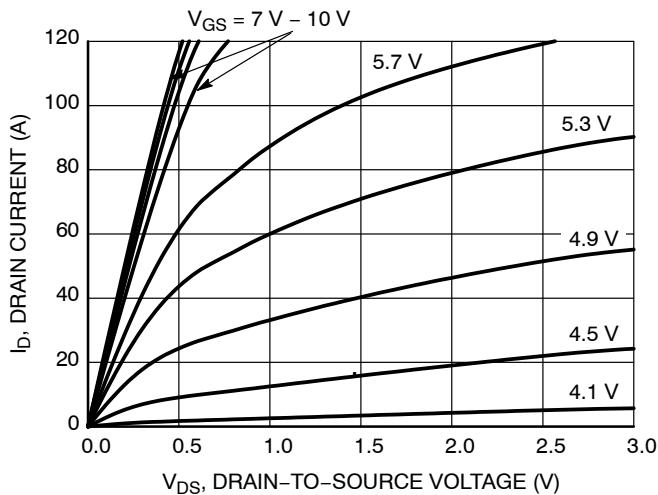


Figure 1. On-Region Characteristics

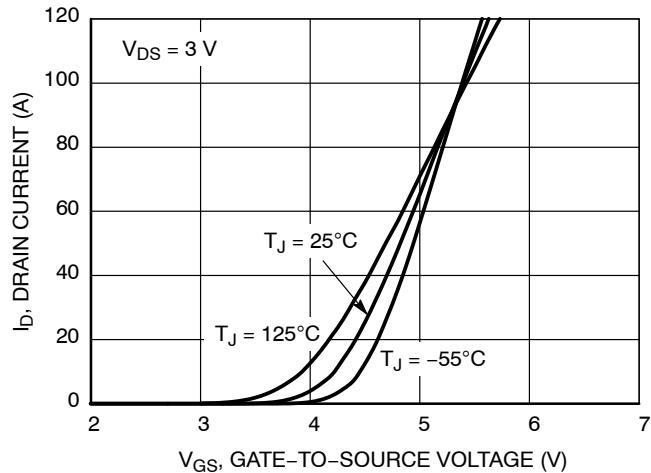


Figure 2. Transfer Characteristics

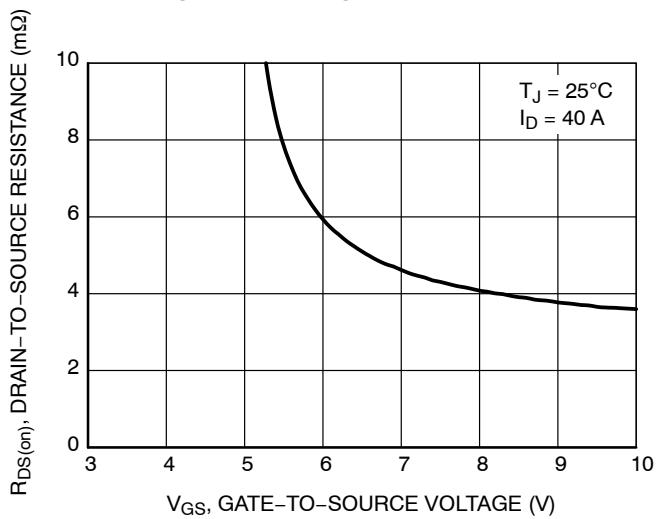


Figure 3. On-Resistance vs. Gate-to-Source Voltage

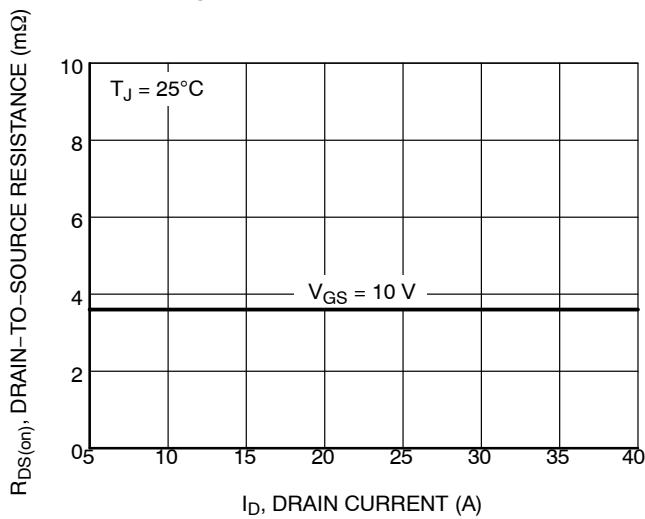


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

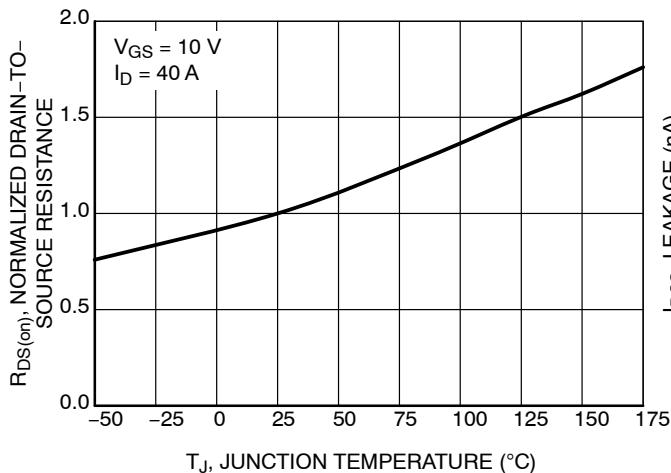


Figure 5. On-Resistance Variation with Temperature

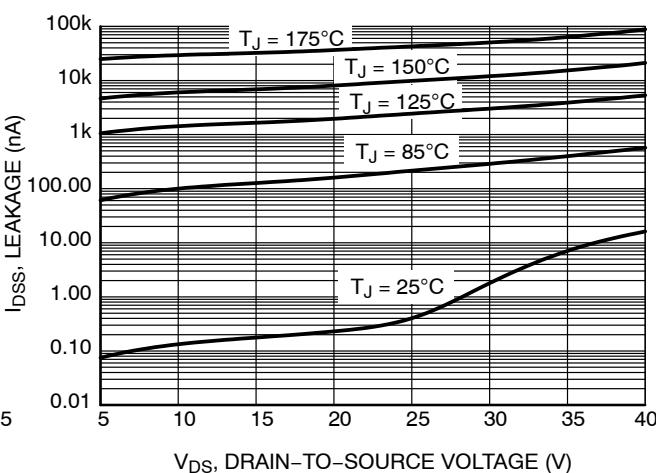


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

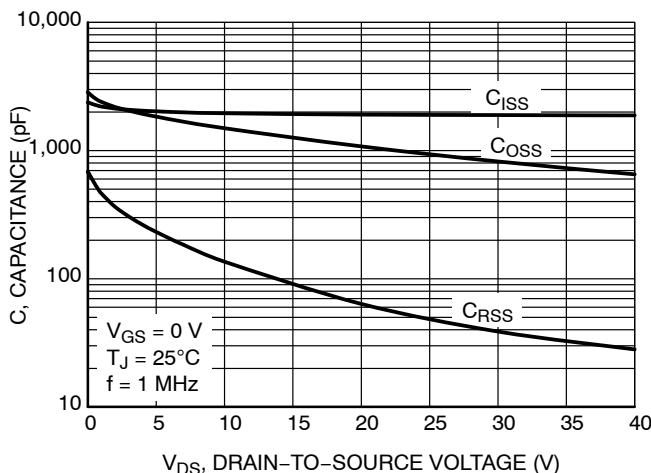


Figure 7. Capacitance Variation

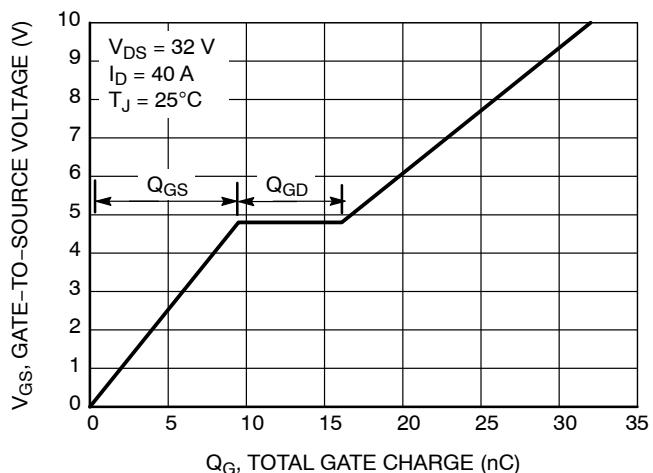


Figure 8. Gate-to-Source vs. Total Charge

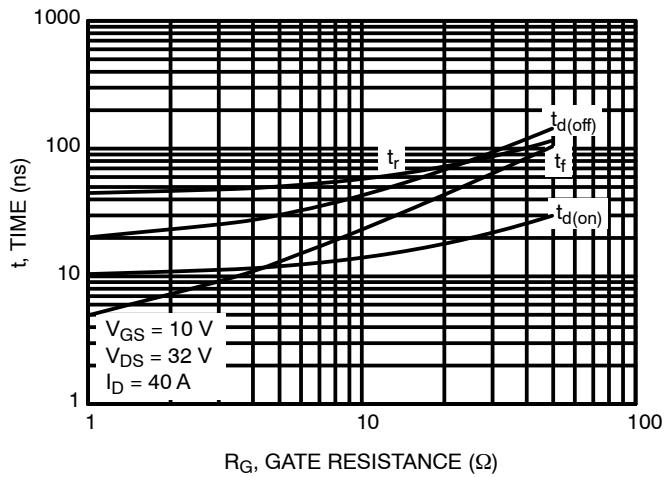


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

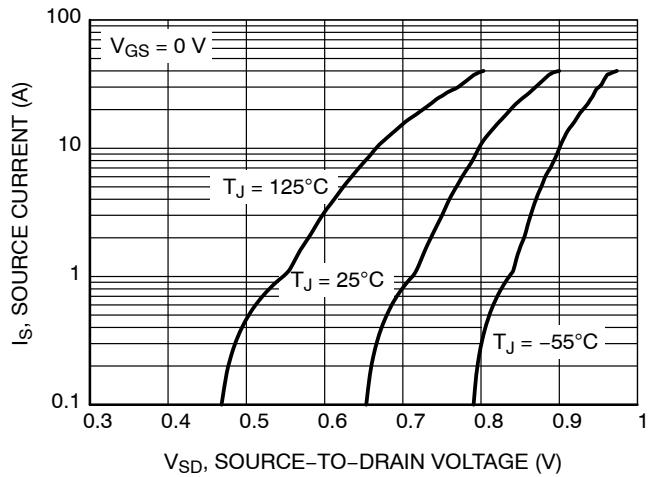


Figure 10. Diode Forward Voltage vs. Current

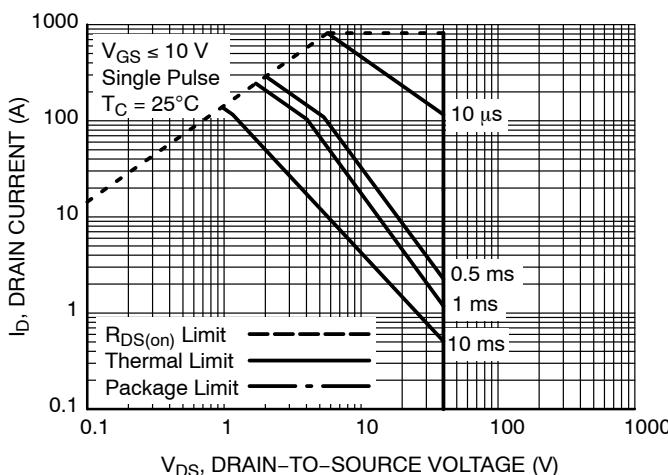


Figure 11. Maximum Rated Forward Biased Safe Operating Area

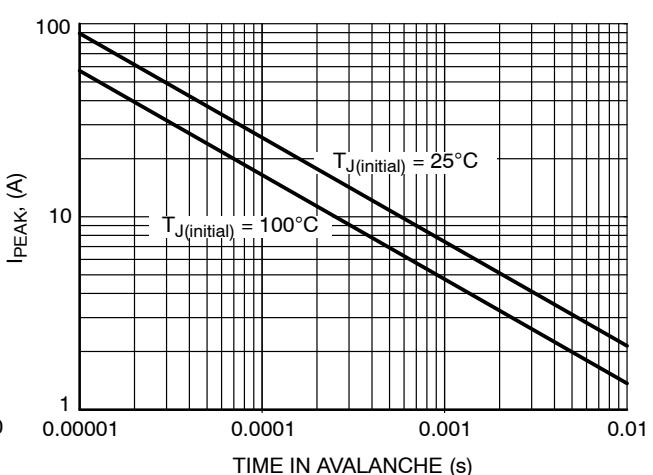
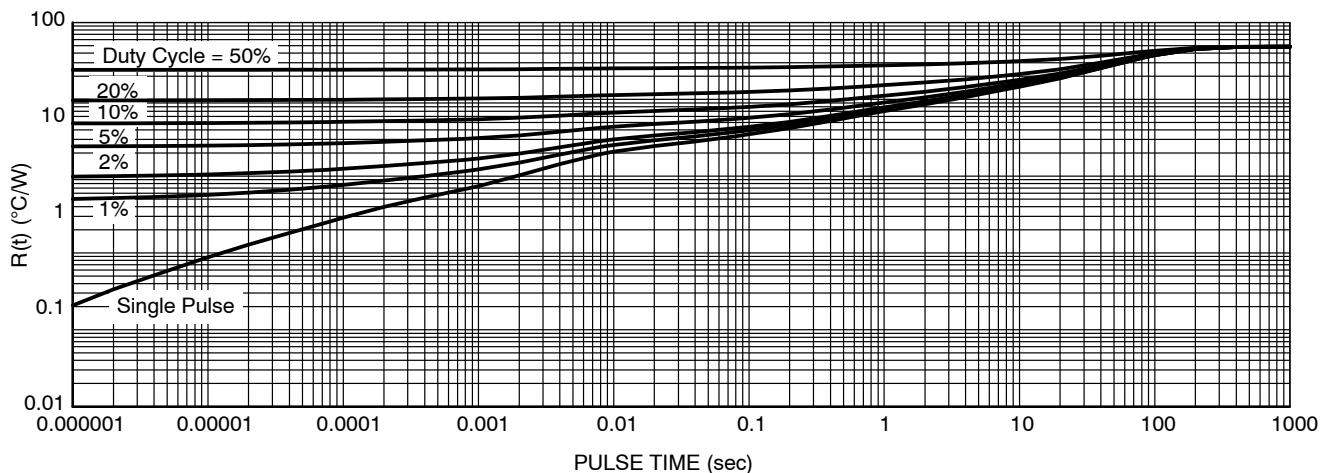
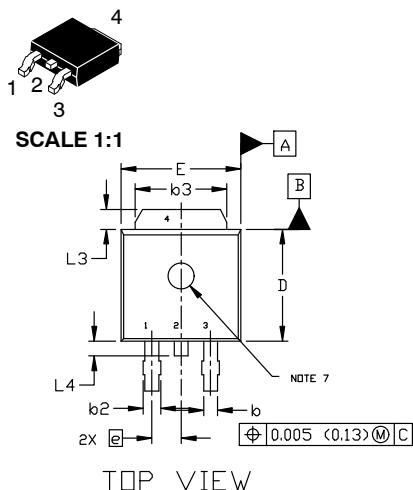


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)**Figure 13. Thermal Response****ORDERING INFORMATION**

| Order Number | Package | Shipping [†] |
|--------------|-------------------|-----------------------|
| NVD5C454NT4G | DPAK (Pb-Free) | 2,500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-----------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | 0.229 BSC | | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | 2.90 REF | | |
| L2 | 0.020 BSC | 0.51 BSC | | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | ---- | 0.040 | ---- | 1.01 |
| Z | 0.155 | ---- | 3.93 | ---- |

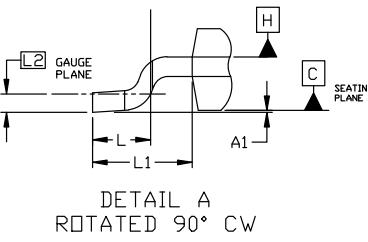
TOP VIEW

SIDE VIEW

BOTTOM VIEW

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. Emitter
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

**GENERIC
MARKING DIAGRAM***



IC

Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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