MPQ4487A

36V, Buck Converter with Programmable Frequency Dual USB Charging Ports Supporting EN, Fault Indication For Automotive, AEC-100 Qualified

DESCRIPTION

The MPQ4487A integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and Type-C 5V under 3A mode configuration channels for each port. The MPQ4487A achieves 6A of output current with excellent load and line regulation across a wide input supply range.

The output of each USB switch is current-limited. Both USB ports support USB Type-C 5V at 3A DFP mode, eliminating the need for outside user interaction.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4487A requires a minimal number of readily available, standard external components. It is available in a QFN-26 (5mmx5mm) package.

FEATURES

- Wide 6V to 36V Operating Input Voltage Range
- Passed Apple MFI R33 Certification Test
- Passed USB-IF Type-C Certification Test
- 135°C Load-Shedding Entry Temperature
- Selectable Output Voltage
- Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 18mΩ/15mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- 18mΩ/18mΩ Low $R_{DS(ON)}$ Internal USB1/USB2 Power MOSFETs
- Frequency Adjustable (250kHz to 2.2MHz)
- Frequency Spread Spectrum for MPQ4487AGU-FD-AEC1/MPQ4487AGU-FD2-AEC1
- Forced Continuous Conduction Mode (FCCM) Operation
- Hiccup Current Limit for Buck and USB
- EN Control for USB1 and USB2
- Fault Indication for USB1 and USB2
- Supports USB Type-C 5V at 3A Mode
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

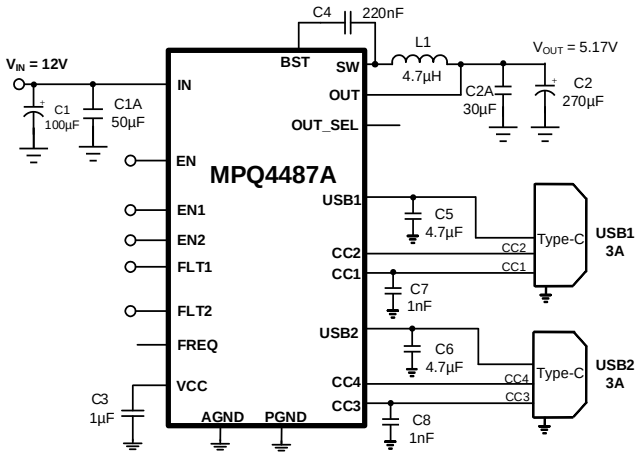
- USB Hubs
- USB Type-C Charging Ports

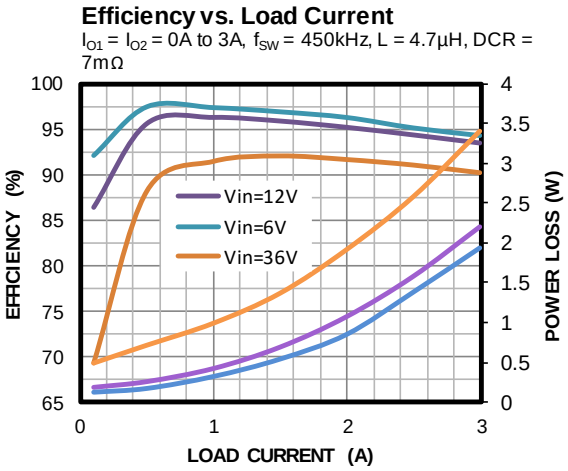
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4487AGU-AEC1	QFN-26 (5mmx5mm)	*See Below*	1
MPQ4487AGU-FD-AEC1			
MPQ4487AGU-FD2-AEC1			

* For Tape & Reel, add suffix -Z (e.g. MPQ4487AGU-AEC1-Z).

DEVICE COMPARISON INFORMATION

Part Number	Frequency Spread Spectrum
MPQ4487AGU-AEC1	No
MPQ4487AGU-FD-AEC1	Yes, fundamental f_{SW} is 420kHz
MPQ4487AGU-FD2-AEC1	Yes, fundamental f_{SW} is 250kHz

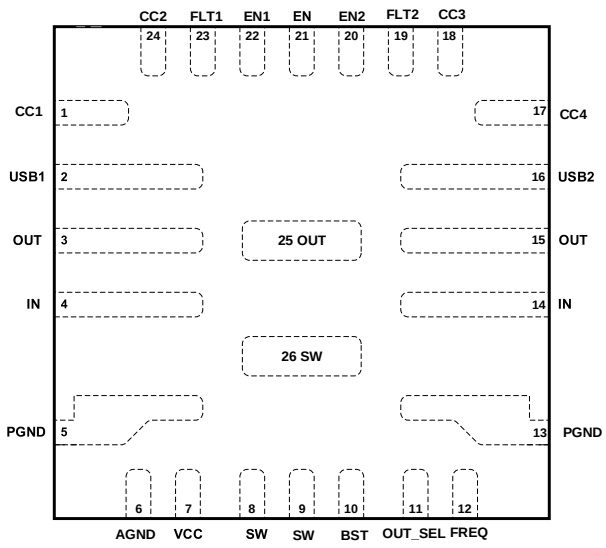
TOP MARKING

MPSYYWW
MP4487A
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4487A: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (5mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the power input for USB1 and USB2.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device, and provides power to the entire chip. The MPQ4487A operates from a 6V to 36V input voltage. A capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration when designing the PCB layout. Connect PGND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple VCC with a 1µF capacitor.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
10	BST	**Bootstrap.** A 0.22µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	OUT_SEL	**Buck output voltage setting.** Set OUT_SEL low for 5.1V, floating for 5.17V, or high for 5.3V.
12	FREQ	**Configurable switching frequency input.** Connect a resistor from FREQ to GND to set the switching frequency. Float FREQ or connect FREQ to VCC for the default 450kHz frequency. Connect FREQ to ground for a 250kHz internal frequency. For the MPQ4487AGU-FD-AEC1, float FREQ or connect FREQ to VCC to achieve a ±10% frequency spread spectrum based on 420kHz. Connect a resistor from FREQ to GND or pull FREQ to GND to set the switching frequency without frequency spread spectrum. For the MPQ4487AGU-FD2-AEC1, float FREQ or connect FREQ to VCC to achieve a ±10% frequency spread spectrum based on 250kHz. Connect a resistor from FREQ to GND or pull FREQ to GND to set the switching frequency without frequency spread spectrum.
16	USB2	**USB2 output.**
17	CC4	**Configuration channel.** CC4 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power over the VCONN pin of the plug.
18	CC3	**Configuration channel.** CC3 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power over the VCONN pin of the plug.
19	FLT2	**USB2 fault indication.** FLT2 indicates over-current or over-temperature conditions. FLT2 is an open drain in normal conditions. Pull FLT2 low during fault conditions.
20	EN2	**USB2 on/off control input.** By default, EN2 is pulled low by an internal 1MΩ resistor.
21	EN	**On/off control of the entire chip.** Pull EN down to ground internally with a 2MΩ resistor.
22	EN1	**USB1 on/off control input.** By default, EN1 is pulled low by an internal 1MΩ resistor.
23	FLT1	**USB1 fault indication.** FLT1 indicates over-current or over-temperature conditions. FLT1 is an open drain in normal conditions. Pull FLT1 low during fault conditions.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.4V to +40V
V_{SW} .....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{BST} .....V_{SW} + 5.5V
V_{EN} ..... -0.3V to +10V (2)
V_{OUT}, V_{USB} ..... -0.3V to +6.5V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-26 (5mmx5mm).....6.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (4)

Human body model (HBM)
CC1/CC2/CC3/CC4 (5).....±7.5kV
DP1/DP2/DM1/DM2/USB1/USB2 (5)…….. ..... ±8kV
All other pins…….....±1.8kV
Charged device model (CDM)
All pins..... ±1kV

Recommended Operating Conditions (6)

Operation input voltage range..... 6V to 36V
Output current.....3A for USB1, 3A for USB2
Operating junction temp (T_J)..-40°C to +125°C (7)

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-26 (5mmx5mm)			
JESD51-7 (8)	44	9	°C/W
50mmx50mm 4-layer PCB (9)	20	2	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, see the EN Control section on page 16.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) HBM, with regard to GND.
6) The device is not guaranteed to function outside of its operating conditions.
7) Operating devices at junction temperatures greater than 125°C is possible; contact MPS for details.
8) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
9) Measured on a 4-layer PCB (50mmx50mm).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		5	10	μA
Quiescent supply current	I_{Q1}	Type-C attached, V_{OUT} = 5.4V, buck not switching		1	2	mA
	I_{Q2}	Type-C unattached, V_{OUT} = 5.4V, buck not switching, T_J = 25°C		400	550	μA
EN rising threshold	V_{EN_RISING}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
EN pull-down resistor	R_{EN}			2		MΩ
Thermal shutdown (10)	T_{TSD}			165		°C
Thermal hysteresis (10)	T_{TSD_HYS}			20		°C
VCC regulator	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		4.6	5.0	5.4	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			800		mV
HS switch on resistance	R_{DSON_HS}			18	40	mΩ
LS switch on resistance	R_{DSON_LS}			15	30	mΩ
Output voltage	V_{OUT}	OUT_SEL = low	-2%	5.10	+2%	V
		OUT_SEL = float, T_J = 25°C	-1%	5.17	+1%	
		OUT_SEL = float, T_J = -40°C to +125°C	-2%	5.17	+2%	
		OUT_SEL = high	-2%	5.30	+2%	
Output over-voltage protection	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	V_{OVP_F}		5.3	5.7	6.1	V
Output to ground resistance	R_{FB}	EN = 0V, T_J = 25°C	100	160	220	kΩ
Low-side current limit	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT}	V_{OUT} = 0V	8	12	16	A
Oscillator frequency	f_{SW1}	Pull R_{FREQ} to GND	185	250	315	kHz
	f_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	
	f_{SW3}	R_{FREQ} = 9.53kΩ, refer to application note	1800	2200	2600	
	f_{SW4}	R_{FREQ} = float	360	450	540	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Frequency spread spectrum span (MPQ4487AGU-FD-AEC1)	f_{SS1}	FREQ = floating, based on 420kHz		±10		%
Frequency spread spectrum span (MPQ4487AGU-FD2-AEC1)	f_{SS2}	FREQ = floating, based on 250kHz		±10		%
Maximum duty cycle	D_{MAX}	FREQ = 450kHz	91	95	99	%
Minimum off time	t_{OFF_MIN}			110		ns
Minimum on time (10)	t_{ON_MIN}			130		ns
Soft-start time	t_{SS}	Output from 10% to 90%	1	2	3.4	ms
USB Switch (USB1 and USB2)						
Under-voltage lockout rising threshold	V_{USB_UVR}		3.7	4	4.3	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			18	35	mΩ
Output to ground resistance	R_{DIS_USB}	Apply 5V voltage on USB output, float CC	350	600	850	Ω
USB OVP clamp	V_{USB_OV}		5.5	5.8	6	V
Current limit	I_{LIMIT1}	V_{OUT} drops 10%, Type-C mode, T_J = 25°C	-6%	5	+6%	A
	I_{LIMIT2}	V_{OUT} drops 10%, Type-A mode, T_J = 25°C	3.6	3.9	4.2	A
Line drop compensation	V_{DROP_COM}	At 2.4A load, V_{OUT} = 5.17V	20	70	120	mV
V_{BUS} soft-start time	t_{SS}	Output from 10% to 90%	0.7	1.4	2.1	ms
V_{BUS} enter hiccup hold time	t_{HICP_ON1}	OC, hiccup on time, T_J = 25°C		3		ms
		OC, hiccup on time, T_J = -40°C to +125°C		3		
Hiccup mode off time	t_{HICP_OFF}	V_{OUT} connected to GND	1	2	3	s
EN1, EN2 logic high input	V_{ENSW_H}		1.2			V
EN1, EN2 logic low input	V_{ENSW_L}				0.8	V
FLT1, FLT2 output low voltage	V_{FLT_LOW}	Fault condition, sink 1mA			150	mV
FLT1, FLT2 leakage	I_{FLT_LKG}	V_{FAULT} = 5V			1	μA
FLT1, FLT2 deglitch time	t_{FLT_DEG}	Over-current		3		ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V at 3A Mode – CC1, CC2, CC3, and CC4						
CC resistor to disable Type-C mode	R_A	CC1 and CC3 pins; for Type-C mode applications, add a 1nF capacitor on CC1 and CC3	90		96	kΩ
CC voltage to enable VCONN	V_{RA}				0.75	V
CC voltage to enable V_{BUS}	V_{RD}		0.9		2.45	V
CC detach threshold	V_{OPEN}		2.65			V
CC voltage falling debounce timer	$t_{CC_DEBOUNCE}$	V_{BUS} enable deglitch	100	144	200	ms
CC voltage rising debounce timer	$t_{PD_DEBOUNCE}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	VCONN comes from the buck output with some series resistance, for applications without SuperSpeed data, T_J = 25°C	1			W

Notes:

10) Guaranteed by design and characterization test.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

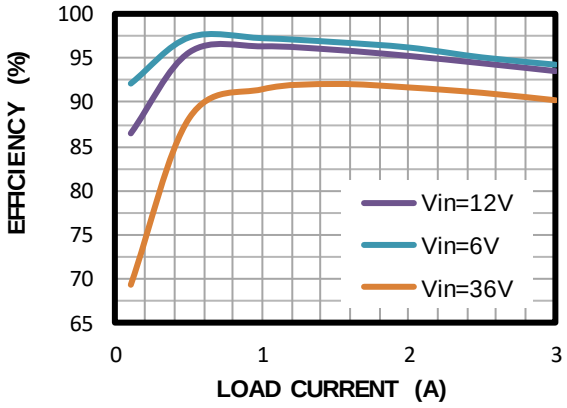
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS

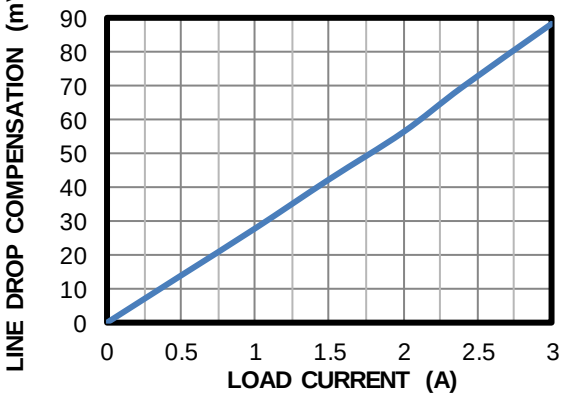
V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

I_{O1}= I_{O2} = 0A to 3A

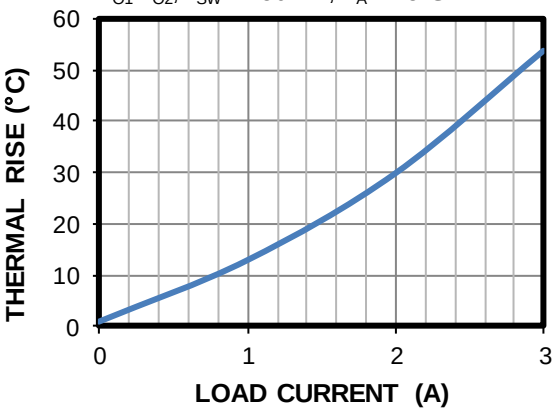


Line Drop Compensation vs. Load Current



Thermal Rise vs. Load Current

I_{O1}=I_{O2}, f_{SW} = 450kHz, T_A = 25℃



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

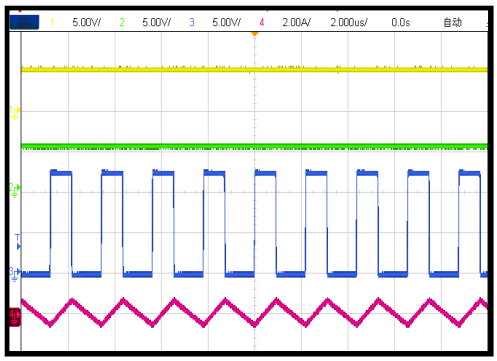
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

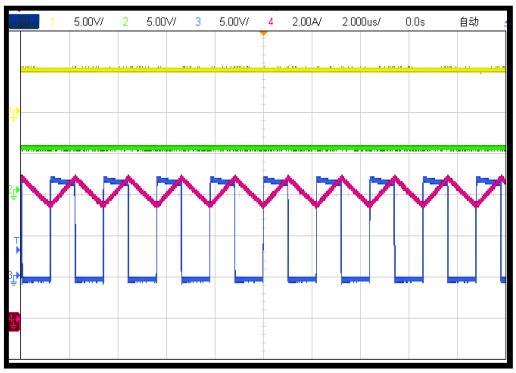
Steady State

I_{O1} = I_{O2} = 0A



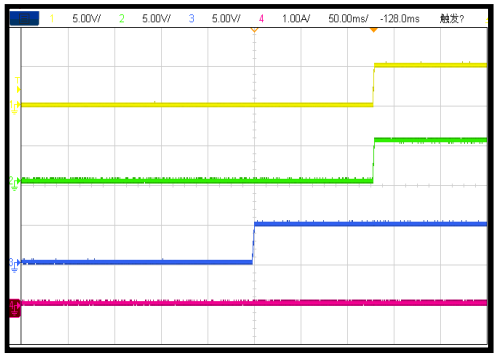
Steady State

I_{O1} = I_{O2} = 3A



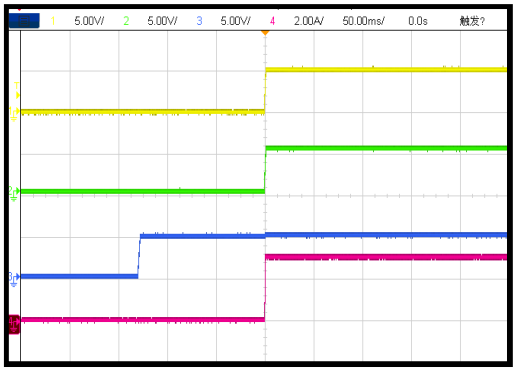
Power Start-Up

I_{O1} = I_{O2} = 0A



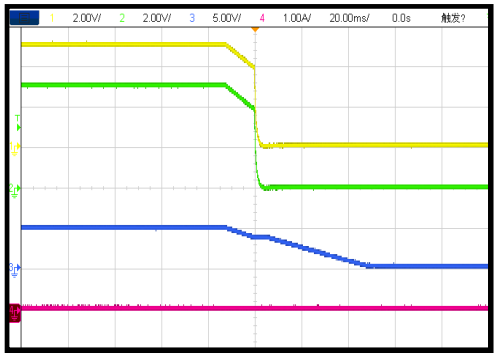
Power Start-Up

I_{O1} = I_{O2} = 3A



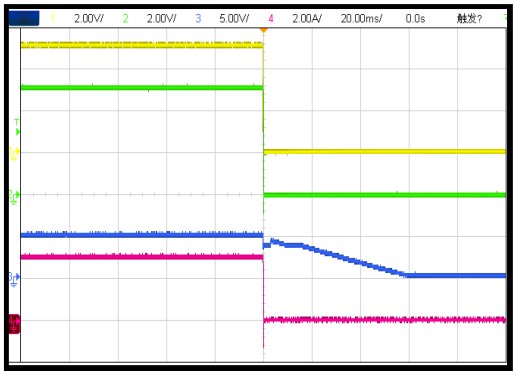
Power Shutdown

I_{O1} = I_{O2} = 0A



Power Shutdown

I_{O1} = I_{O2} = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

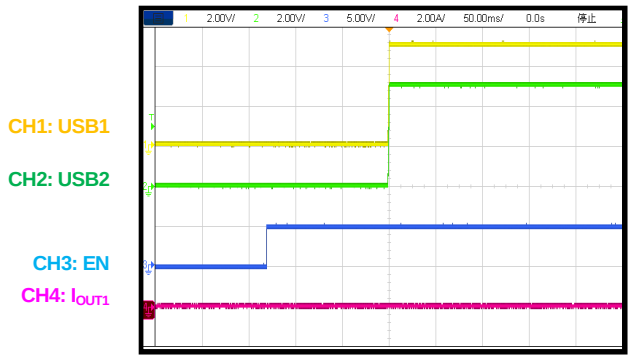
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

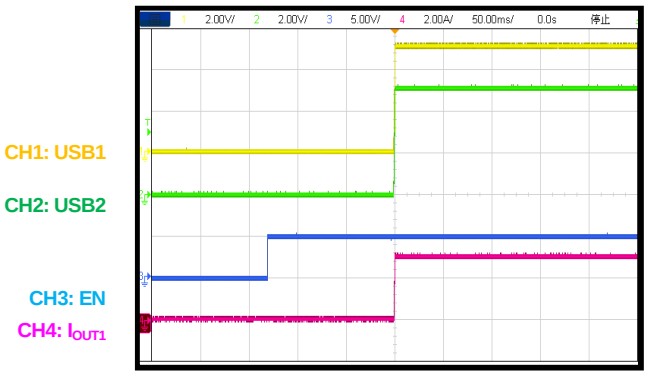
EN Start-Up

I_{O1} = I_{O2} = 0A



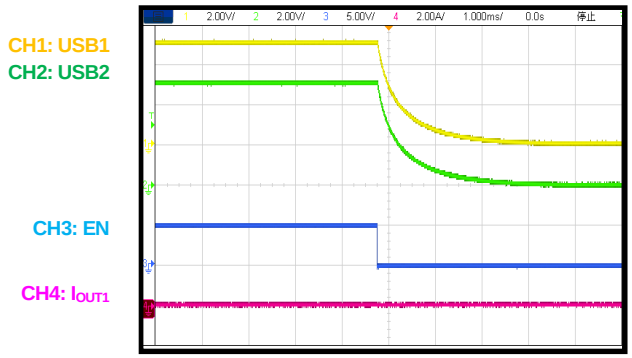
EN Start-Up

I_{O1} = I_{O2} = 3A



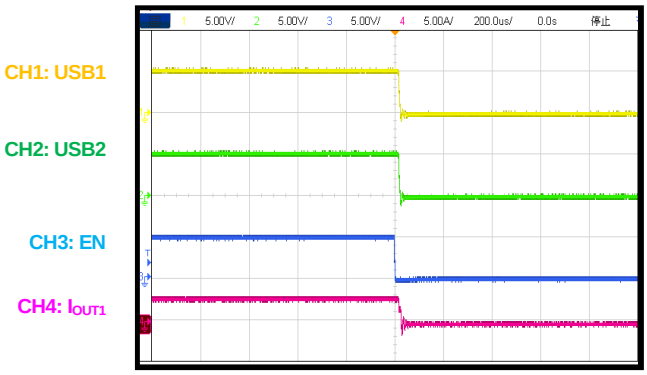
EN Shutdown

I_{O1} = I_{O2} = 0A



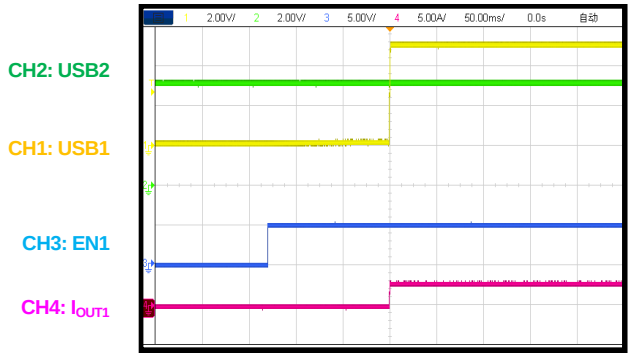
EN Shutdown

I_{O1} = I_{O2} = 3A



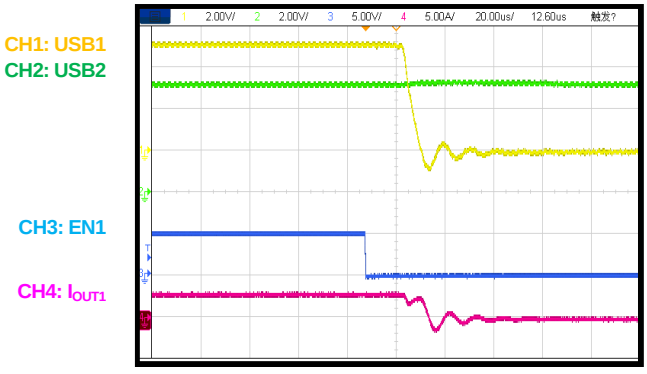
EN1 Start-Up

I_{O1} = I_{O2} = 3A



EN1 Shutdown

I_{O1} = I_{O2} = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

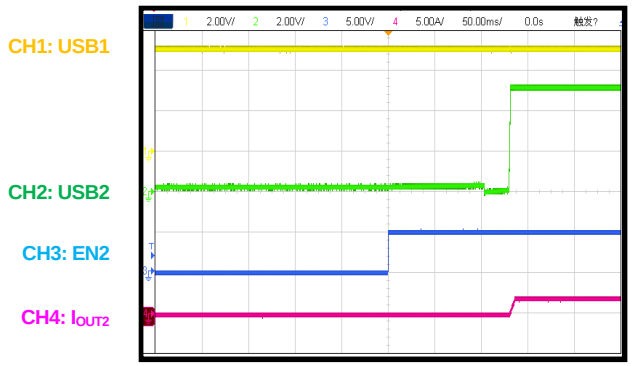
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

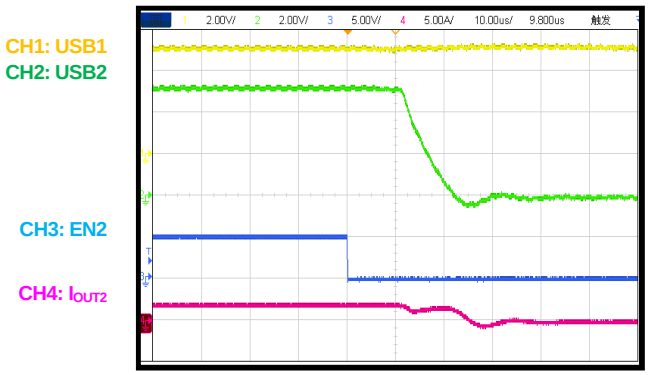
EN2 Start-Up

I_{O1} = I_{O2} = 3A



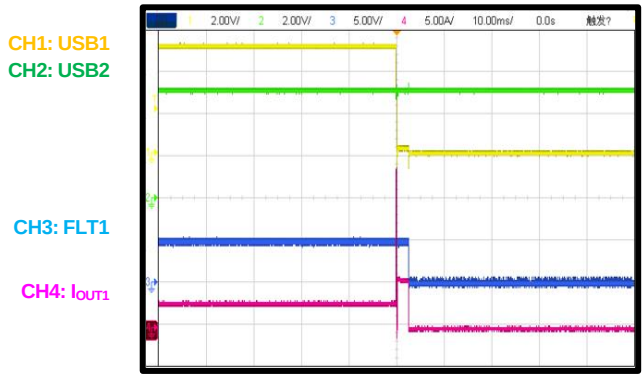
EN2 Shutdown

I_{O1} = I_{O2} = 3A



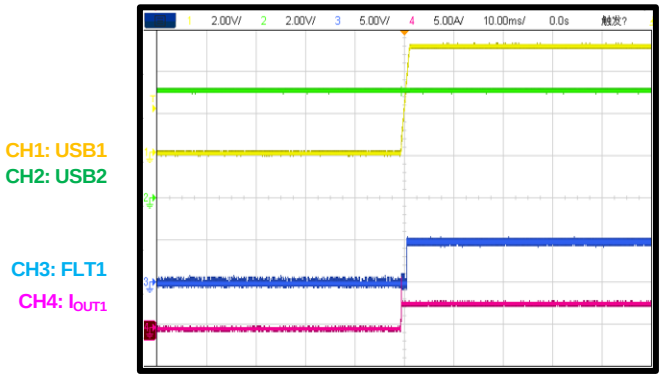
USB1 SCP Entry

I_{O1} = I_{O2} = 3A, load on USB output



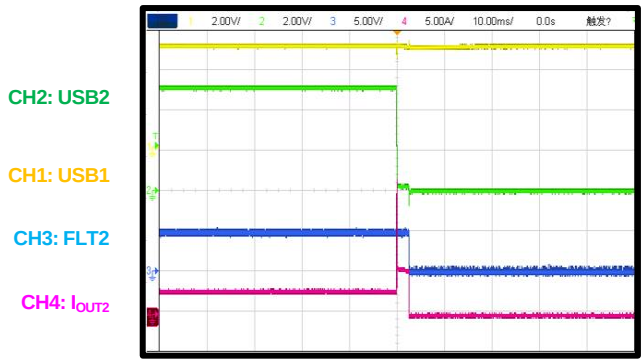
USB1 SCP Recovery

I_{O1} = I_{O2} = 3A, load on USB output



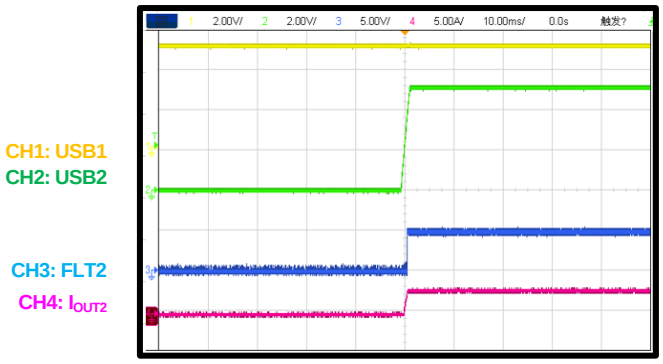
USB2 SCP Entry

I_{O1} = I_{O2} = 3A, load on USB output



USB2 SCP Recovery

I_{O1} = I_{O2} = 3A, load on USB output



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

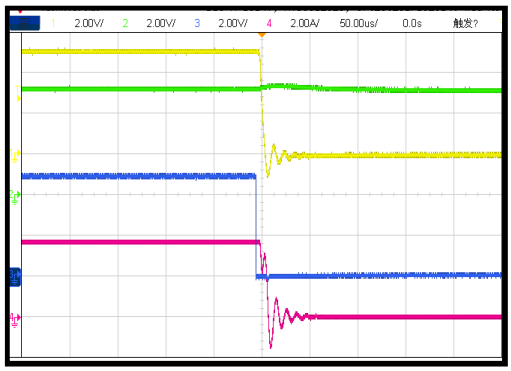
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

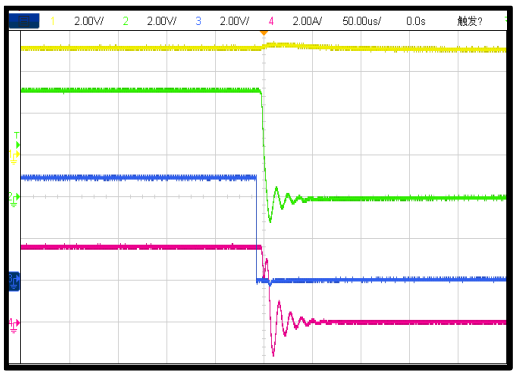
USB1 OCP

I_{O1} = I_{O2} = 0A, ramp up load current slowly



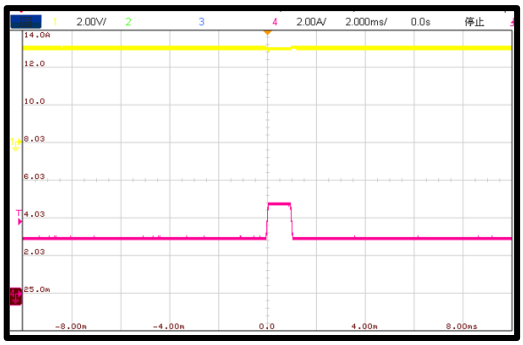
USB2 OCP

I_{O1} = I_{O2} = 0A, ramp up load current slowly



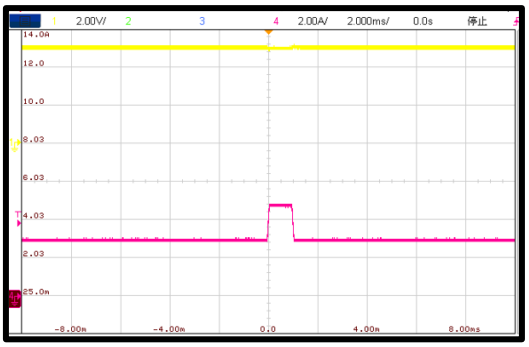
USB1 Load Transient

I_{OUT} = 3A to 4.8A, 500ms/1ms



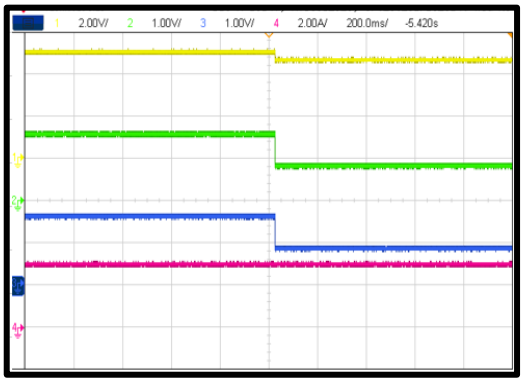
USB2 Load Transient

I_{OUT} = 3A to 4.8A, 500ms/1ms



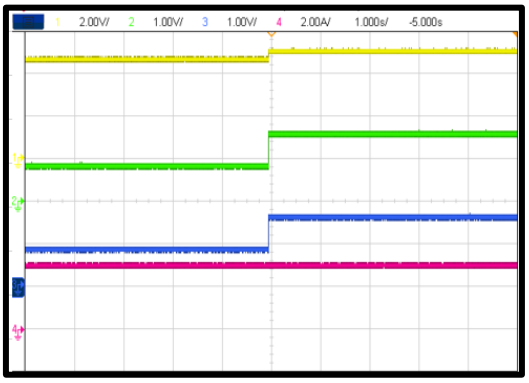
Load-Shedding Entry

I_{O1} = 3A



Load-Shedding Recovery

I_{O1} = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

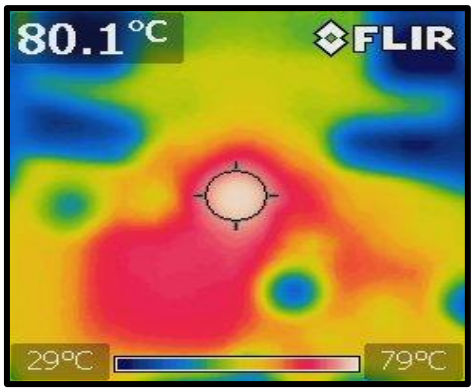
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Thermal Image

USB1 = USB2 = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

FUNCTIONAL BLOCK DIAGRAM

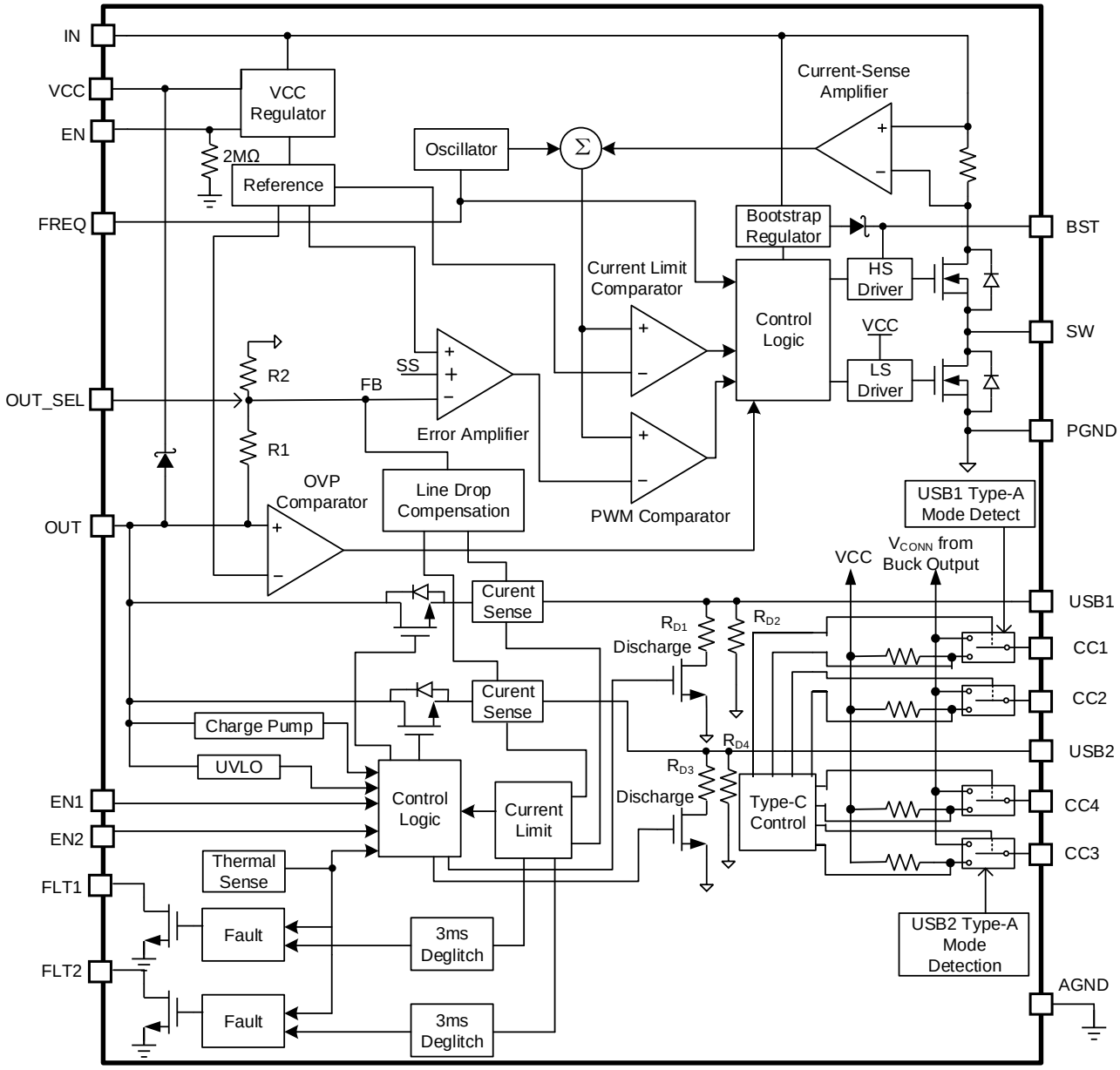


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

OPERATION

BUCK CONVERTER

The MPQ4487A integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current limit switches with charging port auto-detection. The MPQ4487A offers a compact solution that achieves 6A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ4487A operates in fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (450kHz switching frequency) in one PWM period, the current in the power MOSFET does not reach the current value set by COMP, and the power MOSFET turns off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 4.6V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.6V, the output of the regulator is in full regulation. If V_{IN} is below 4.6V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the buck output starts up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

Enable (EN) Control

The MPQ4487A has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC. Once EN is pulled high, the buck output is enabled, regardless of the statuses of EN1, EN2, or CC1 through CC4.

It is recommended to connect EN to VIN and GND through resistor dividers. When selecting a pull-up resistor, ensure that it can limit the current flowing into the EN pin below 100µA.

For example, if EN's pull-up resistor is 100kΩ, its pull-down resistor should be 34.8kΩ. Then the IC starts up when V_{IN} exceeds the under-voltage lockout (UVLO) threshold. The IC powers off when V_{IN} drops below the UVLO falling threshold.

Do not add a >1nF capacitor on the EN pin.

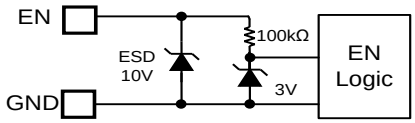


Figure 2: Zener Diode between EN and GND

Setting the Frequency

Connect a resistor from FREQ to ground to set the switching frequency (see Table 1).

Table 1: Recommended Resistor Values for Typical Switching Frequency

R_{FREQ} (kΩ)	f_{SW} (kHz)
0	250
66.5	350
NS	450
45.8	500
22.3	1000
14.6	1500
9.53	2200

The value of the frequency can be estimated with Equation (1):

$$FREQ(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(k\Omega) + 53.7} \quad (1)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Figure 3 shows the frequency vs. R_{FREQ} curve.

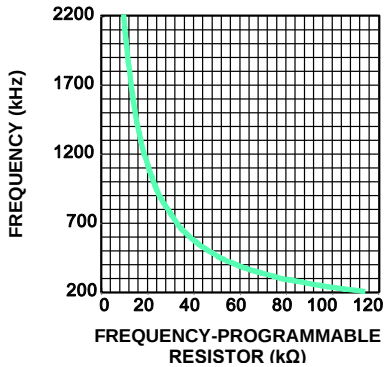


Figure 3: Switching Frequency vs. R_{FREQ}

If the part is being run at a high switching frequency (e.g. 2.2MHz), consider the minimum on time, minimum off time, and the maximum output current due to the thermal rise.

Two internal comparators monitor FREQ's logic voltage. These comparators enable FREQ to float, or short FREQ to GND. During start-up, there is another internal source current on FREQ. The frequency is locked at 450kHz when FREQ senses a voltage exceeding 2V for at least 8μs. The frequency is locked at 250kHz when a voltage below 0.1V is sensed on FREQ for at least 8μs. Leave FREQ floating or connect FREQ to VCC for a default switching frequency of 450kHz. Short FREQ to ground for a 250kHz frequency (see Figure 4).

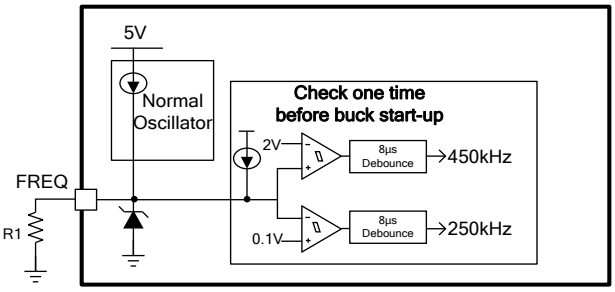


Figure 4: Switching Frequency Functional Block

Frequency Spread Spectrum

The purpose of frequency spread spectrum is to minimize the peak emissions at a specific frequency.

The MPQ4487AGU-FD-AEC1 and MPQ4487AGU-FD2-AEC1 use a 4kHz triangle wave (125μs rising, 125μs falling) to modulate the internal oscillator. The frequency span of the spread spectrum operation is ±10% (see Figure 5).

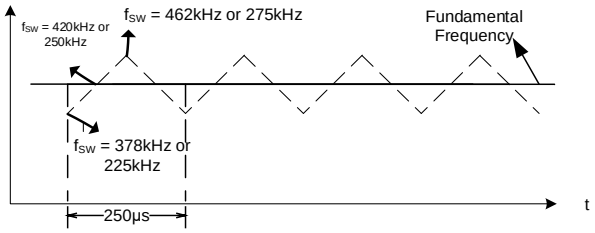


Figure 5: Frequency Spread Spectrum

FREQ must be floating or connected to VCC when using the spread spectrum function. The device can work without switching frequency spread spectrum when FREQ is connected to an external resistor or shorted to GND.

Pull FREQ to GND to set the fixed switching frequency at 250kHz without frequency spread spectrum. The frequency is determined by an external resistor when FREQ is connected to GND.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5V, and its falling threshold is 4.2V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 5V. When the SS voltage (V_{SS}) is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 2ms internally. If the output of the device is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Forced Continuous Conduction Mode (FCCM) Operation

The MPQ4487A can work in forced continuous conduction mode (FCCM). The MPQ4487A operates with a fixed switching frequency regardless of whether it is operating in light load or full load.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

The advantage of FCCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charge time. However, FCCM is less efficient under light-load conditions. A proper inductance should be selected to avoid triggering the LS-FET's negative current limit (typically 2A, from SW to GND). If the negative current limit is triggered, the LS-FET turns off, and the HS-FET turns on when the internal clock begins.

Buck Over-Current Protection (OCP)

The MPQ4487A has a cycle-by-cycle over-current limit when the inductor peak current exceeds the current limit threshold, and the FB voltage drops below the under-voltage (UV) threshold. Once UV is triggered, the MPQ4487A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4487A exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MPQ4487A has output over-voltage protection (OVP). If the output exceeds 5.85V, the HS-FET stops turning on. The LS-FET turns on to discharge the output voltage until the output decreases to 5.7V, and then the chip resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 6).

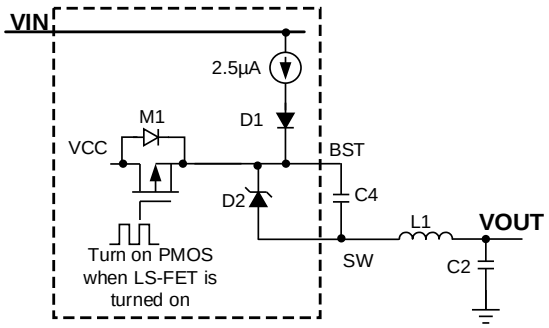


Figure 6: Internal Bootstrap Charging Circuit

The BST capacitor (C4) voltage is charged up quickly by turning on M1 when the LS-FET is turned on. The 2.5µA input to the BST current source can also charge the BST capacitor when the LS-FET does not turn on.

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, IN low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Impedance

The buck does not involve an output discharge function during EN shutdown. After EN shuts down, there are only two feedback resistors connected to OUT, which have a typical resistance of 160kΩ.

USB CURRENT LIMIT SWITCH

Current Limit Switch

The MPQ4487A integrates two USB current limit switches. The MPQ4487A provides built-in soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges. When the load current reaches the current limit threshold, the USB power MOSFET works in constant current limit mode (see Figure 7).

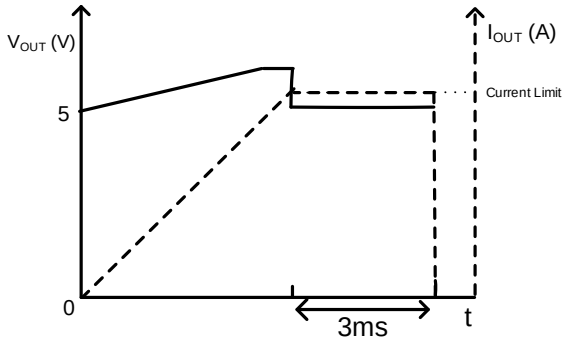


Figure 7: Over-Current Limit

If the over-current limit condition lasts for longer than 3ms, the corresponding USB channel enters hiccup mode with 3ms of on time and 2s

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

of off time. The other USB channel still works normally.

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 10.5A secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This can help limit the peak current through the switch, keeping the buck output voltage from dropping too much and affecting another USB channel. The total short-circuit response time is shorter than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. If the short remains during the restart process, the MPQ4487A regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4487A can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches, and uses the larger current-sense output voltage to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. It also has an upper limitation. The line drop compensation is 70mV at 2.4A output current.

USB Output Over-Voltage Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage exceeds the OVP threshold, the output voltage is clamped to its OVP threshold value.

USB Output Discharge and Impedance

Each USB switch has a fast discharge path that can discharge the external output capacitor's energy quickly during a power shutdown. This function is active when the CC pins are released or the part is disabled (input voltage is under UVLO or EN is off). The discharge path is turned off when the USB output voltage is discharged below 50mV. After the fast discharge path turns off, there is only a high-impedance resistor (typically 500kΩ) from USB1 or USB2 to ground.

USB Enable On/Off Control (EN1, EN2)

EN1 and EN2 are the on/off control input pins for USB1 and USB2, respectively. The USB switch is active when EN is pulled high. Float or pull the EN voltage to logic low to shut down the USB switch with an output discharge. EN1 and EN2 are pulled low by an internal 1MΩ resistor to ground. Connect EN1 and EN2 to VCC through a 100kΩ resistor for automatic start-up, or to control them by an external on/off signal.

Fault Indication (FLT1, FLT2)

FLT1 and FLT2 are the fault indication pins for USB1 and USB2, respectively. FLT is in an open-drain state during shutdown, start-up, or normal operation. If the USB switch enters hiccup mode, or over-temperature protection (OTP) is triggered, FLT is pulled low.

FLT asserts (logic low) on an individual USB switch during an over-current or over-temperature condition. FLT switches high after the fault condition is removed, and the USB output voltage goes high again.

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins (CC1, CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To help define the functional behavior of CC, a pull-up (R_P) and pull-down (R_D, 5.1kΩ) termination model is used based on the pull-up resistor and pull-down resistor (see Figure 8).

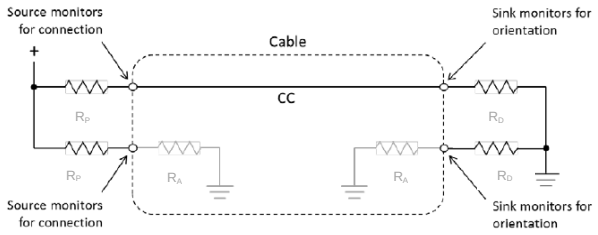


Figure 8: Current Source/Pull-Down CC Model

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The source-to-sink circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage below its unterminated voltage. The choice of R_P is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes R_A (typically 1kΩ) on its VCONN pin. R_A represents the load on VCONN, plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it may simply be the load.

The source must be able to differentiate between the presence of R_D and R_A to detect whether there is a sink attached and where to apply VCONN. The source is not required to source VCONN unless R_A is detected. VCONN quickly discharges when exiting VCONN mode.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: R_A / R_A for audio adapter mode, and R_D / R_D for debugging mode (see Figure 9 and Table 2).

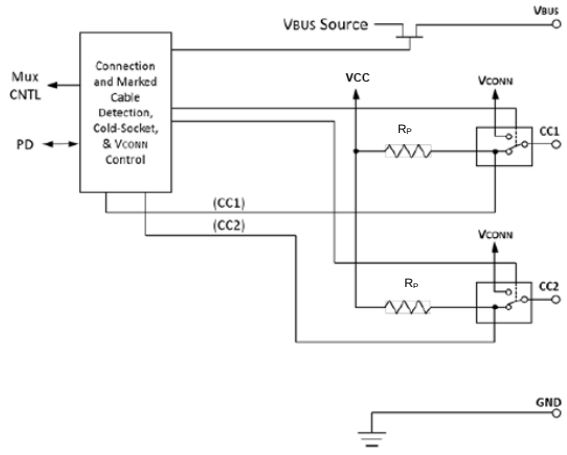


Figure 9: CC Functional Block

A port that behaves as a source has the following functional characteristics:

- The source uses a MOSFET to enable or disable the power delivery across V_{BUS}. Initially, the source is disabled.
- The source supplies pull-up resistors (R_P) on CC1 and CC2, and monitors both to detect a sink. The presence of an R_D pull-down resistor on either CC1 or CC2 indicates that a sink is being attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4487A's default R_P is 10kΩ, which represents a 3A current level.
- The source uses the CC pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when R_A is detected).
- Once a sink is detected, the source enables V_{BUS} and VCONN.
- The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures, the MPQ4487A changes R_P to 22kΩ to indicate a 1.5A current ability.
- The source monitors the continued presence of R_D to detect a sink detachment. When a detach event is detected, the source is removed, and V_{BUS} and VCONN return to point 2 (see above).

Disable Type-C Mode (Type-A Mode)

During the MPQ4487A's initial start-up, the IC sources current on CC1 for a certain time. If the CC1 voltage falls to a certain voltage range, USB1 latches in Type-A mode unless the part is re-enabled. Type-C mode is disabled, so CC1's attach and detach logic is disabled, and V_{BUS} is always enabled. The current limit changes to a Type-A specification. The same logic is implemented on CC3 for USB2.

To trigger Type-A mode, the external pull-down resistor should be 95.3kΩ. Do not connect extra capacitors on CC1 and CC3.

In normal Type-C mode applications, a 1nF capacitor should be added on CC1 and CC3 to avoid falsely triggering Type-A mode. If two R_A resistors pull down CC1 and CC2, or two R_D resistors pull down CC1 and CC2, there is no IC action (V_{BUS} is not enabled) (see Table 2 on page 22).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Load-Shedding vs. Temperature

The MPQ4487A monitors the die temperature and changes its output current capability with this value.

If the die temperature exceeds 135°C, the USB port's CC pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A. Meanwhile, V_{BUS} changes to 4.77V.

If the die temperature recovers and drops below 100°C for 16 seconds, V_{BUS} reverts back to the normal voltage set by OUT_SEL. Meanwhile, the USB Type-C current capability changes back to 3A (R_P = 10kΩ). The current-limit threshold remains at 5A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 145°C), the chip is enabled.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Table 2: CC Logic Truth Table

EN	EN1	EN2	CC of USB1 (11)	CC of USB2 (11)	Buck	VCONN (USB1)	USB1	VCONN (USB2)	USB2
0	X	X	X	X	Disabled	Disabled	Disabled	Disabled	Disabled
1	0	0	X	X	Enabled	Disabled	Disabled	Disabled	Disabled
1	1	0	AUDIO	X	Enabled	Disabled	Disabled	Disabled	Disabled
			DEBUG	X	Enabled	Disabled	Disabled	Disabled	Disabled
			A (12)	X	Enabled	Disabled	Enabled	Disabled	Disabled
			R_D, R_A	X	Enabled	Enabled	Enabled	Disabled	Disabled
			Open	X	Enabled	Disabled	Disabled	Disabled	Disabled
1	0	1	X	AUDIO	Enabled	Disabled	Disabled	Disabled	Disabled
			X	DEBUG	Enabled	Disabled	Disabled	Disabled	Disabled
			X	A	Enabled	Disabled	Disabled	Disabled	Enabled
			X	R_D, R_A	Enabled	Disabled	Disabled	Enabled	Enabled
			X	Open	Enabled	Disabled	Disabled	Disabled	Disabled
1	1	1	AUDIO	X	Enabled	Disabled	Disabled	X	X
			DEBUG	X	Enabled	Disabled	Disabled	X	X
			A	X	Enabled	Disabled	Enabled	X	X
			R_D, R_A	X	Enabled	Enabled	Enabled	X	X
			Open	X	Enabled	Disabled	Disabled	X	X
			X	AUDIO	Enabled	X	X	Disabled	Disabled
			X	DEBUG	Enabled	X	X	Disabled	Disabled
			X	A	Enabled	X	X	Disabled	Enabled
			X	R_D, R_A	Enabled	X	X	Enabled	Enabled
			X	Open	Enabled	X	X	Disabled	Disabled
1	1	1	AUDIO	R_D, R_A	Enabled	Disabled	Disabled	Enabled	Enabled
			DEBUG		Enabled	Disabled	Disabled	Enabled	Enabled
			A		Enabled	Disabled	Enabled	Enabled	Enabled
			Open		Enabled	Disabled	Disabled	Enabled	Enabled
			R_D, R_A	AUDIO	Enabled	Enabled	Enabled	Disabled	Disabled
				DEBUG	Enabled	Enabled	Enabled	Disabled	Disabled
				A	Enabled	Enabled	Enabled	Disabled	Enabled
				R_D, R_A	Enabled	Enabled	Enabled	Enabled	Enabled
				Open	Enabled	Enabled	Enabled	Disabled	Disabled
			A	A	Enabled	Disabled	Enabled	Disabled	Enabled
			Open	A	Enabled	Disabled	Disabled	Disabled	Enabled
			A	Open	Enabled	Disabled	Enabled	Disabled	Disabled
			Open	Open	Enabled	Disabled	Disabled	Disabled	Disabled

Notes:

11) USB1 and USB2 are symmetrical to one other.
12) "A" means Type-A mode. CC1 (CC3 for USB2) must be pulled down by a 95.3kΩ resistor to enter this mode.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating that exceeds the maximum load current by at least 25%. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductor value can be calculated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 100µF electrolytic and 50µF ceramic capacitors are recommended in automotive applications with a 450kHz switching frequency.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

A 100µF to 270µF capacitor with an ESR below 50mΩ (e.g. polymer or tantalum capacitors) and three 10µF ceramic capacitors are recommended in the application (see Table 3).

Table 3: Recommended External Components

Switching Frequency	Inductor	Input Capacitor	Buck Output Capacitor
250kHz	8µH	50µF ceramic capacitor and 100µF e-capacitor	30µF ceramic capacitor and 270µF polymer capacitor
450kHz	4.7µH	50µF ceramic capacitor and 100µF e-capacitor	30µF ceramic capacitor and 270µF polymer capacitor

ESD Protection for I/O Pins

Consider higher ESD levels for all USB I/O pins. The ESD structures can withstand high ESD during both normal operation and when the device is off. To further extend CC's ESD level for complicated application environments, additional ESD diodes can be added on CC.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

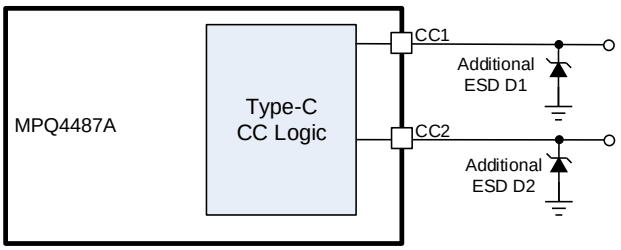


Figure 10: Recommended CC Pins ESD Enhancing

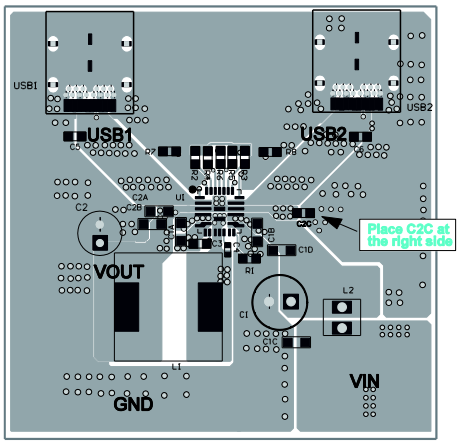
PCB Layout Guidelines [13]

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 11 and follow the guidelines below:

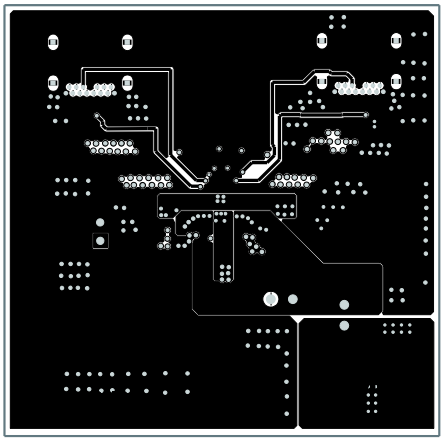
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place the buck output ceramic capacitors (C2A and C2B) on the left side, and place C2C on the right side.
5. Add a large copper plane for PGND.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Place a large copper plane for SW, USB, and USB2.
9. Route the USB1 and USB2 traces on both PCB layers.
10. Place two ceramic input decoupling capacitors as close to IN and PGND as possible to improve EMI performance.
11. Place the symmetric C_{IN} capacitors on each side of the IC.
12. Place the BST capacitor close to BST and SW.
13. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

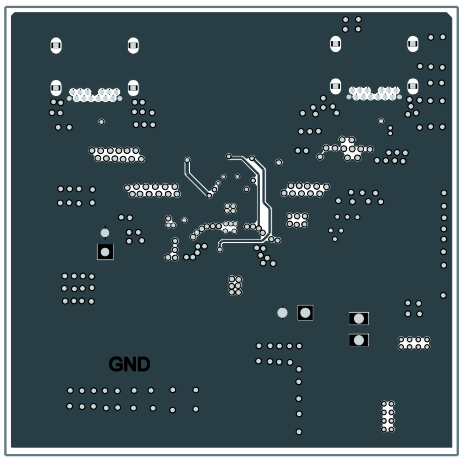
13) The recommended layout is based on the Typical Application Circuits (see Figure 12, Figure 13, and Figure 14 on page 25 and page 26).



Top Layer



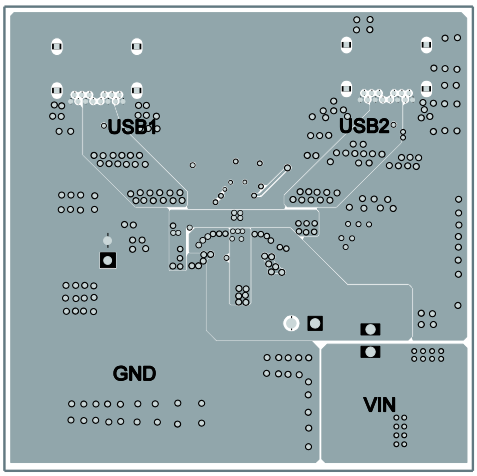
Middle Layer 1



Middle Layer 2

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.



Bottom Layer

Figure 11: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

TYPICAL APPLICATION CIRCUITS

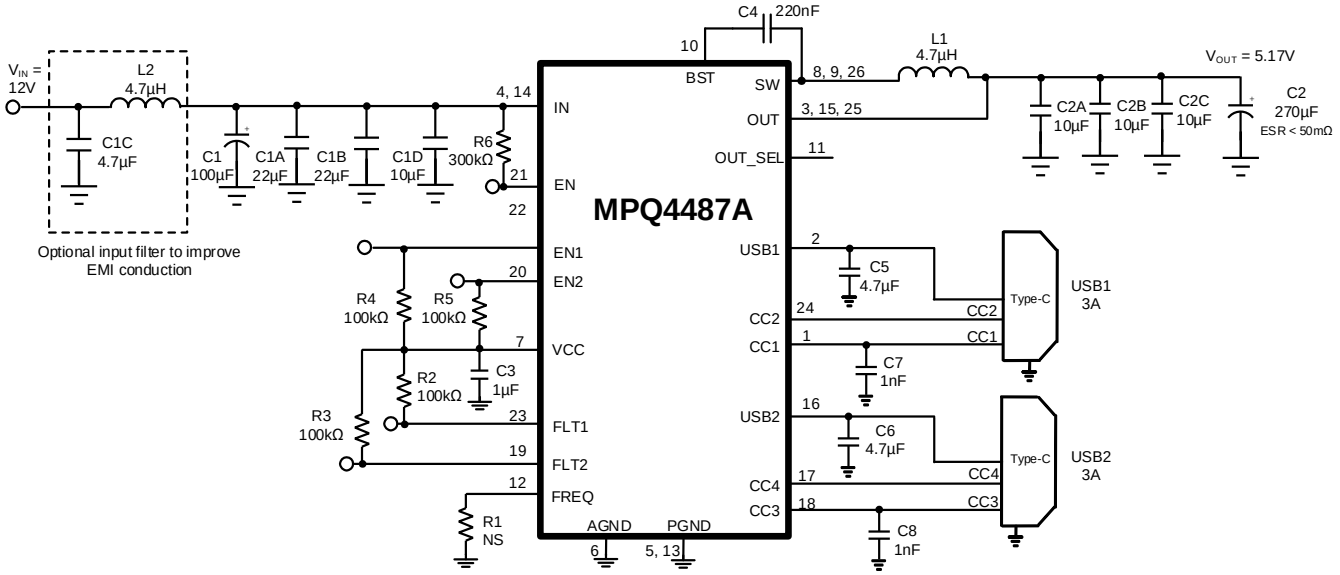


Figure 12: Dual USB Type-C 5V/3A DFP Ports (14)

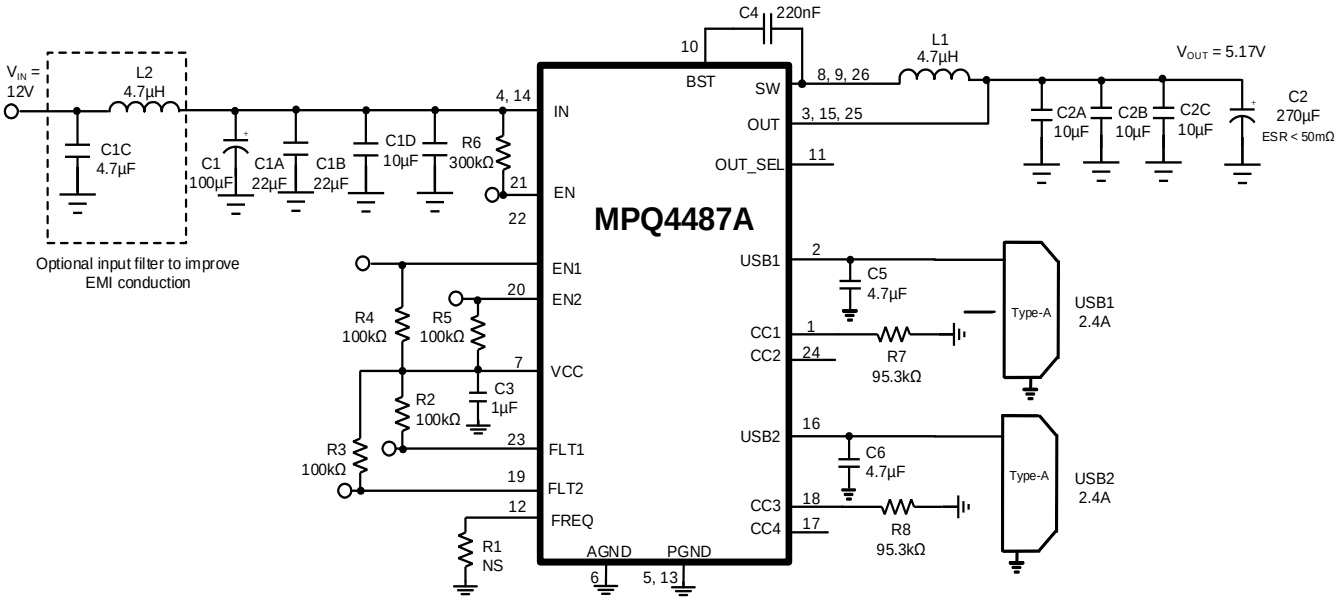


Figure 13: Dual USB Type-A 5V/2.4A Ports (14)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

TYPICAL APPLICATION CIRCUITS *(continued)*

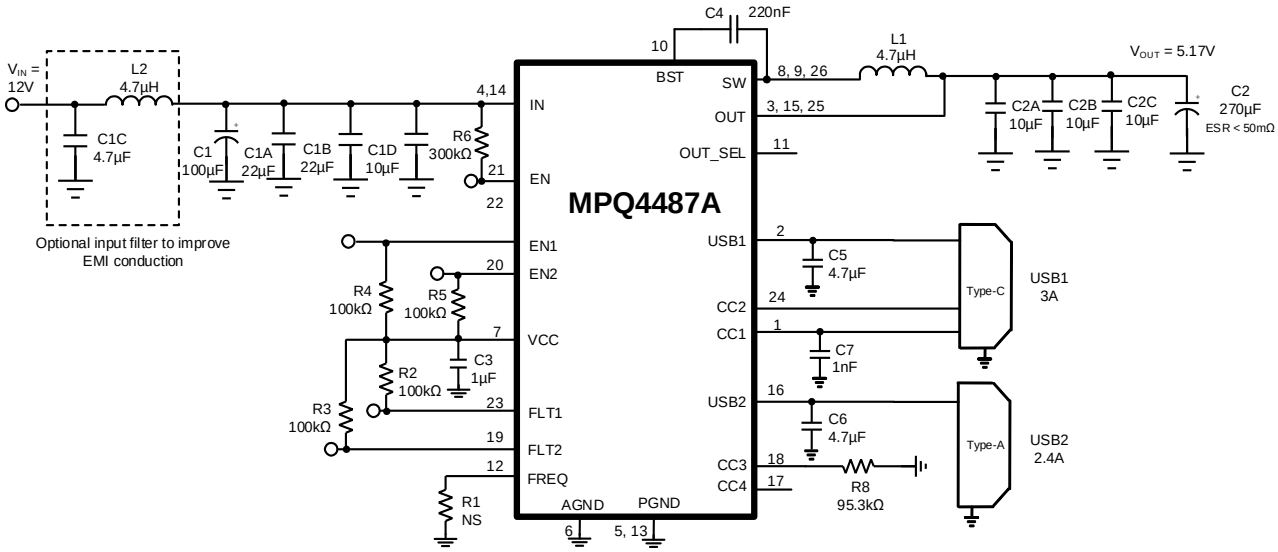


Figure 14: One Type-C 5V/3A DFP Port, One USB2 Type-A 5V/2.4A Port (14)

Note:

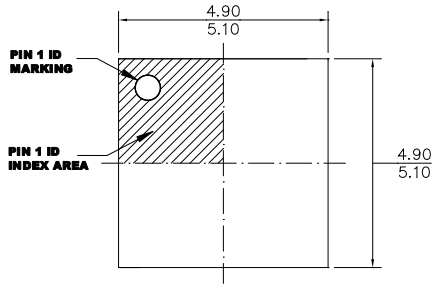
14) See Figure 10 on page 24 for the CC pins' ESD protection enhancing details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

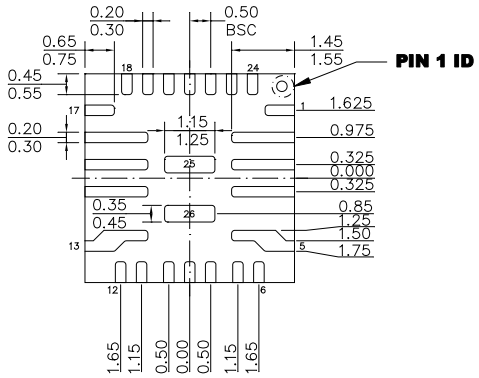
Downloaded from Arrow.com.

PACKAGE INFORMATION

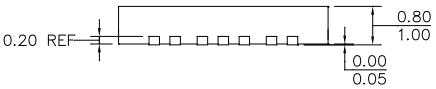
QFN-26 (5mmx5mm)



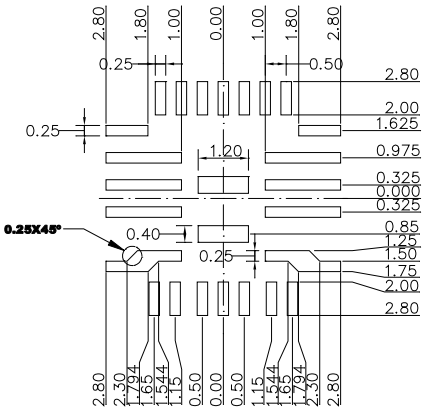
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

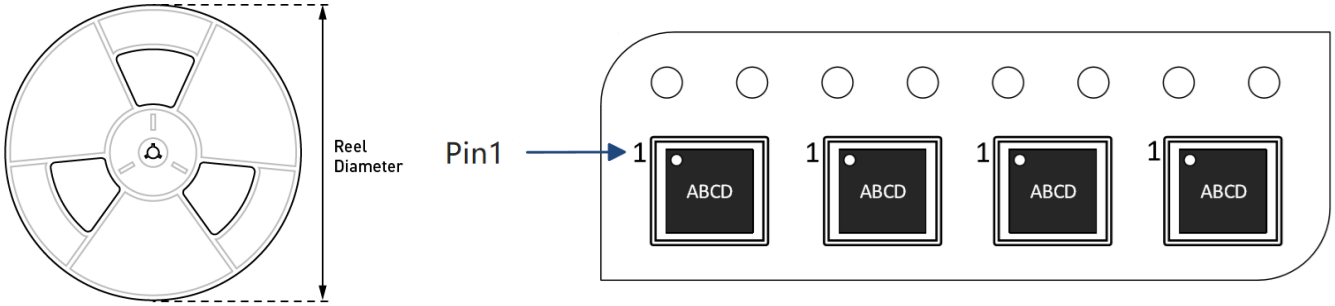
NOTE:

1) LAND PATTERNS OF PINS 2, 3, AND 4, AS WELL AS 14, 15, AND 16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4487AGU-AEC1-Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4487AGU-FD-AEC1-Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4487AGU-FD2-AEC1-Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/23/2020	Initial Release	-
1.1	12/7/2021	Added MPQ4487-FD2 PN to the figure and ordering information	1, 3
		Updated the FREQ pin description	5
		Added f_{SS2} to the Electrical Characteristics section	8
		Updated the Frequency Spread Spectrum section	17
		Added FD2 carrier information	30
		Minor formatting updates	All

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Downloaded from Arrow.com.