



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

8-Mbit (512K × 16-bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
 - Typical standby current: 1.4 μ A
 - Maximum standby current: 6.5 μ A
- High speed: 45 ns
- Voltage range: 1.65 V to 3.6 V
- Embedded Error-Correcting Code (ECC) for single-bit error correction
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA, 44-TSOP II and 48-pin TSOP I packages

Functional Description

CY62157G and CY62157GE are high-performance CMOS low-power (MoBL®) SRAM device with Embedded Error-Correcting Code. ECC logic can detect and correct single bit error in accessed location.

This device is offered in dual chip enable option. Dual chip enable devices are accessed by asserting both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable input ($\overline{WE}$ LOW), and providing the data and address on device data (I/O_0 through I/O_{15}) and address (A_0 through A_{18}) pins respectively. The Byte High/Low Enable ($\overline{BHE}$, BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and BLE controls I/O_0 through I/O_7 .

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$, BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH/ CE_2 LOW for dual chip enable device), or control signals are de-asserted ($\overline{OE}$, BLE, $\overline{BHE}$).

These devices also have a unique “Byte Power down” feature, where, if both the Byte Enables ($\overline{BHE}$ and BLE) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62157G and CY62157GE devices are available in a Pb-free 48-ball VFBGA, 44-TSOP II and 48-pin TSOP I packages. See the [Logic Block Diagram – CY62157G on page 2](#).

The device in the 48-pin TSOP I package can also be configured to function as a 1M × 8-bit device. See the [Pin Configurations on page 5](#).

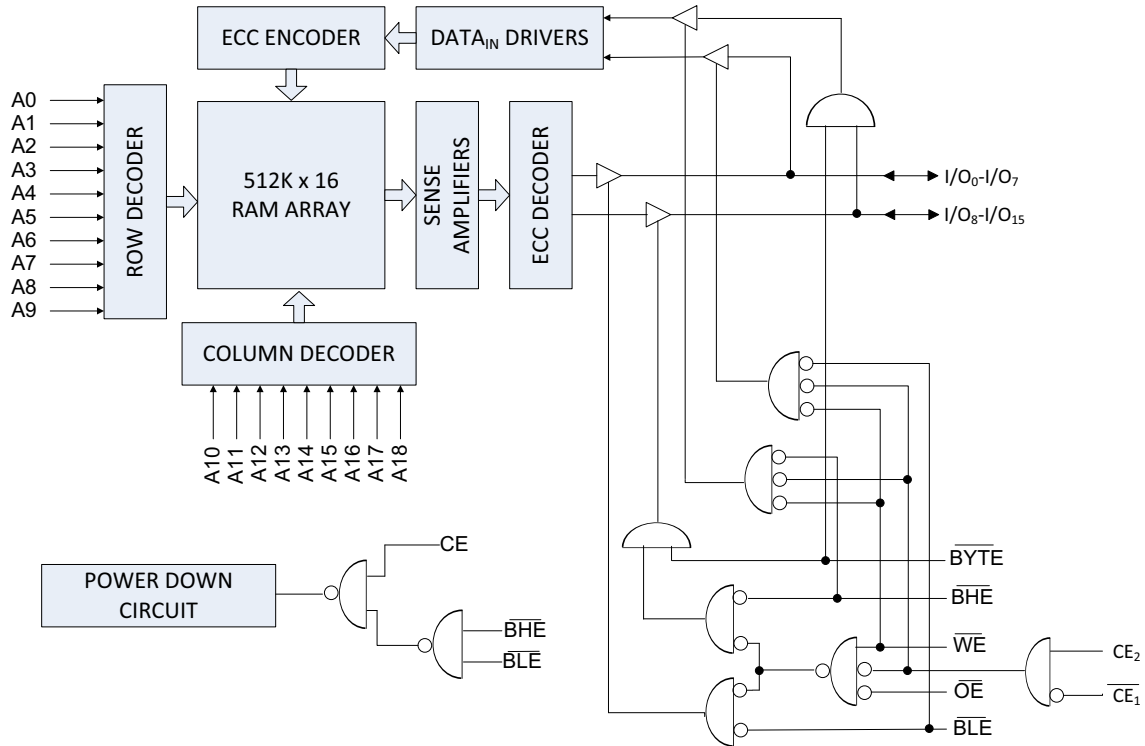
Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I _{CC} : (mA)		Standby, I _{SB2} (μA)	
				f = f _{max}			
				Typ ^[1]	Max	Typ ^[1]	Max
CY62157G18	Industrial	1.65 V–2.2 V	55	18	22	2.0	8
CY62157G30	Industrial	2.2 V–3.6 V	45	18	25	1.4	6.5

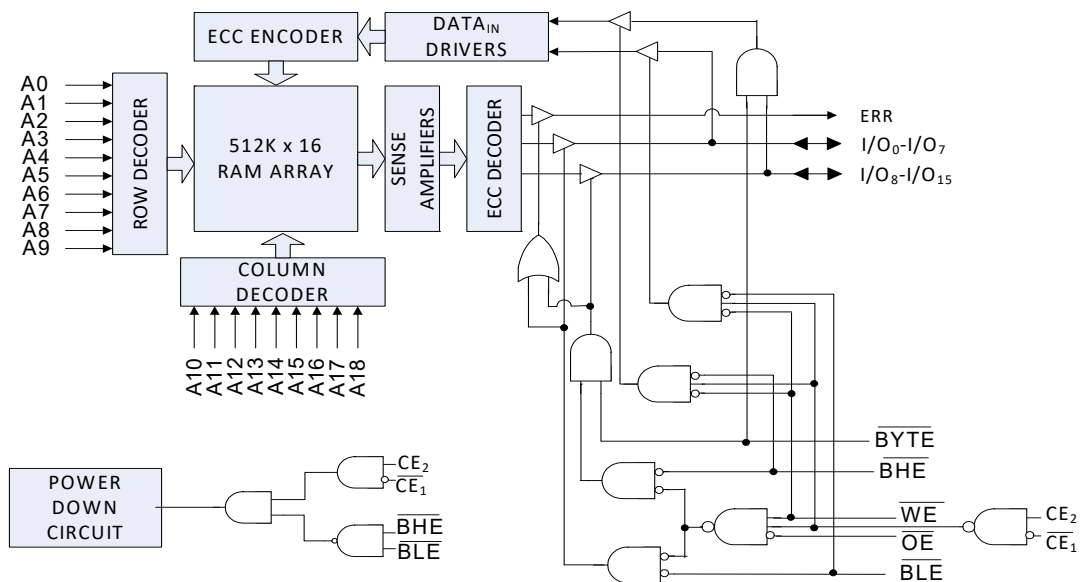
Note

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3$ V (for V_{CC} range of 2.2 V–3.6 V) and $V_{CC} = 1.8$ V (for V_{CC} range of 1.65 V–2.2 V), $T_A = 25$ °C.

Logic Block Diagram – CY62157G



Logic Block Diagram – CY62157GE



Contents

Pin Configurations	4	Ordering Information	17
Maximum Ratings	6	Ordering Code Definitions	17
Operating Range	6	Package Diagrams	18
DC Electrical Characteristics	6	Acronyms	21
Capacitance	7	Document Conventions	21
Thermal Resistance	7	Units of Measure	21
AC Test Loads and Waveforms	8	Document History Page	22
Data Retention Characteristics	8	Sales, Solutions, and Legal Information	23
Data Retention Waveform	9	Worldwide Sales and Design Support	23
Switching Characteristics	10	Products	23
Switching Waveforms	11	PSoC® Solutions	23
Truth Table – CY62157G/CY62157GE	16	Cypress Developer Community	23
ERR Output – CY62157GE	16	Technical Support	23

Pin Configurations

Figure 1. 48-ball VFBGA Pinout (Top View)^[2]

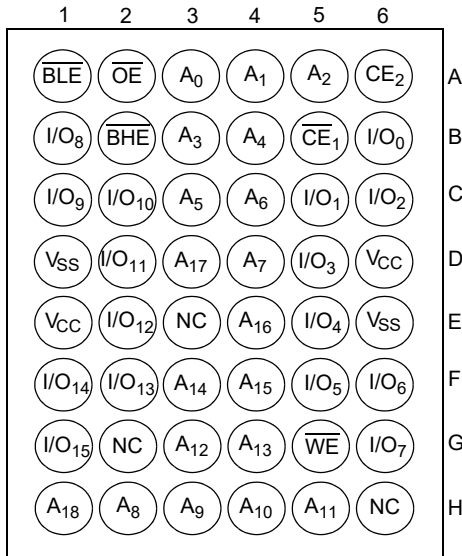


Figure 2. 48-ball VFBGA Pinout (with ERR (Top View))^[2]

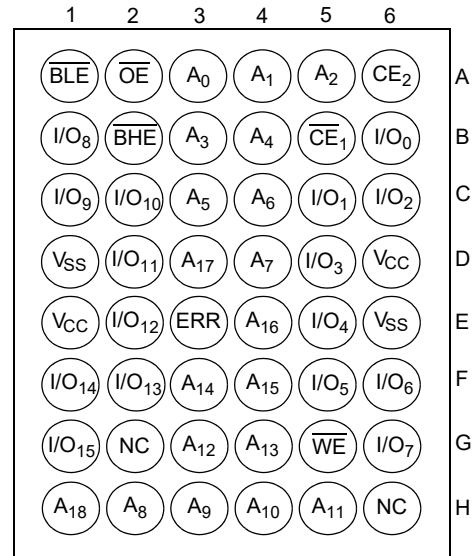
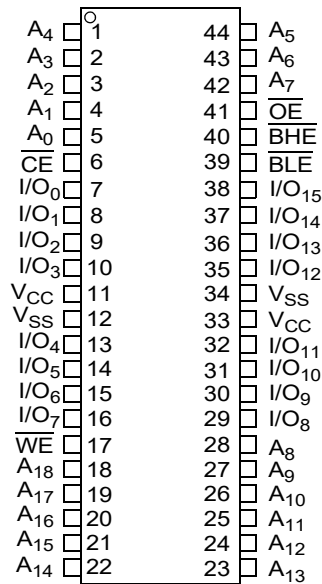


Figure 3. 44-pin TSOP II Pinout (Top View)^[2]



Note

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configurations (continued)

Figure 4. 48-pin TSOP I Pinout (Top View)^[3, 4]

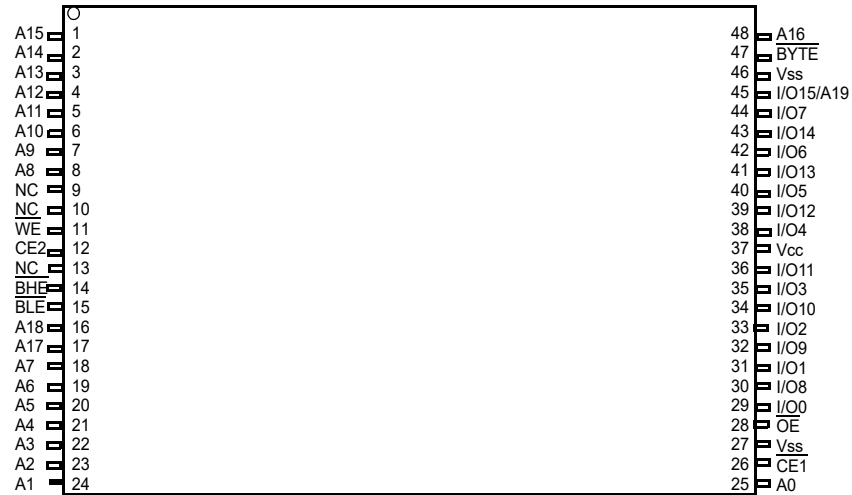
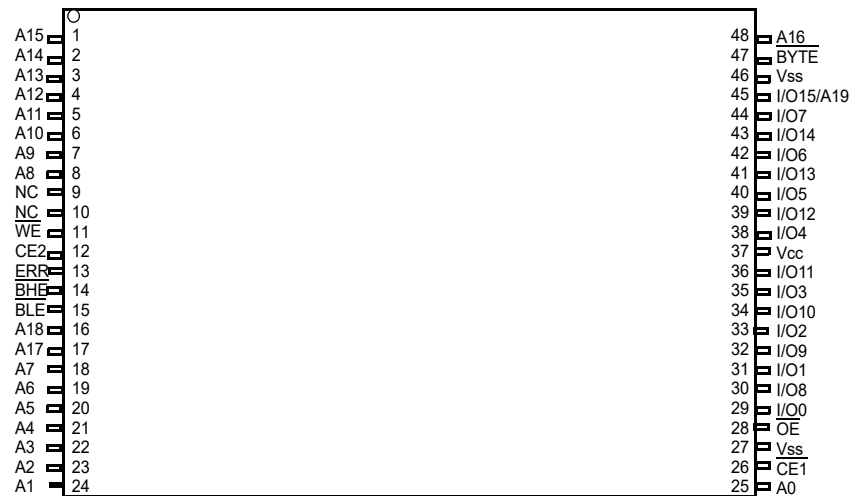


Figure 5. 48-pin TSOP I Pinout (with ERR (Top View))^[3, 4]



Notes

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- Tie the **BYTE** pin in the 48-pin TSOP I package to V_{CC} to use the device as a 512K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the **BYTE** signal to V_{SS} . In the 1M × 8 configuration, Pin 45 is the extra address line A19, while **BHE**, **BLE**, and **I/O₈** to **I/O₁₄** pins are not used and can be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage
to ground potential -0.2 V to $V_{CC} + 0.3$ V

DC voltage applied to outputs
in High Z state^[5] -0.2 V to $V_{CC} + 0.3$ V

DC input voltage^[5] -0.2 V to $V_{CC} + 0.3$ V

Output current into outputs (LOW) 20 mA

Static discharge voltage (HBM)
(MIL-STD-883, Method 3015) >2001 V

Latch-up current >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V 2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description		Test Conditions		45/55 ns			Unit
					Min	Typ ^[6]	Max	
V _{OH}	Output HIGH voltage	1.65 V to 2.2 V	V _{CC} = Min, I _{OH} = −0.1 mA	1.4	–	–	V	
		2.2 V to 2.7 V	V _{CC} = Min, I _{OH} = −0.1 mA	2	–	–		
		2.7 V to 3.6 V	V _{CC} = Min, I _{OH} = −1.0 mA	2.4	–	–		
V _{OL}	Output LOW voltage	1.65 V to 2.2 V	V _{CC} = Min, I _{OL} = 0.1 mA	–	–	0.2	V	
		2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 0.1 mA	–	–	0.4		
		2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 2.1 mA	–	–	0.4		
V _{IH}	Input HIGH voltage	1.65 V to 2.2 V	–	1.4	–	V _{CC} + 0.2	V	
		2.2 V to 2.7 V	–	1.8	–	V _{CC} + 0.3		
		2.7 V to 3.6 V	–	2	–	V _{CC} + 0.3		
V _{IL}	Input LOW voltage ^[6]	1.65 V to 2.2 V	–	−0.2	–	0.4	V	
		2.2 V to 2.7 V	–	−0.3	–	0.6		
		2.7 V to 3.6 V	–	−0.3	–	0.8		
I _{IX}	Input leakage current		GND ≤ V _{IN} ≤ V _{CC}	−1	–	+1	μA	
I _{OZ}	Output leakage current		GND ≤ V _{OUT} ≤ V _{CC} , Output disabled	−1	–	+1		
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	18	25	mA	
			f = 18.18 MHz (55 ns)	–	18	22		
			f = 1 MHz	–	6	7		
I _{SB1} ^[7]	Automatic power down current – CMOS inputs; V _{CC} = 2.2 to 3.6 V	CE ₁ ≥ V _{CC} − 0.2 V or CE ₂ ≤ 0.2 V, (BHE and BLE) ≥ V _{CC} − 0.2 V, V _{IN} ≥ V _{CC} − 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE, and WE), V _{CC} = V _{CC(max)}		–	1.4	6.5	μA	
	Automatic power down current – CMOS inputs; V _{CC} = 1.65 to 2.2 V			–	2.0	8.0		

Notes

- $V_{IL(\text{min})} = -2.0$ V and $V_{IH(\text{max})} = V_{CC} + 2$ V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3$ V (for V_{CC} range of 2.2 V–3.6 V) and $V_{CC} = 1.8$ V (for V_{CC} range of 1.65 V–2.2 V), $T_A = 25$ °C.
- Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
- The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

DC Electrical Characteristics (continued)

Over the Operating Range of -40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns			Unit
				Min	Typ ^[6]	Max	
$I_{SB2}^{[7]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2$ to 3.6 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, (BHE and BLE) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = V_{CC(max)}$	$25^\circ\text{C}^{[8]}$	–	1.4	2.8	μA
			$40^\circ\text{C}^{[8]}$	–	–	3.5	
			$70^\circ\text{C}^{[8]}$	–	–	5.5	
			85°C	–	–	6.5	
	Automatic power down current – CMOS inputs $V_{CC} = 1.65$ to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, (BHE and BLE) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = V_{CC(max)}$		–	2.0	8.0	μA

Notes

- $V_{IL(min)} = -2.0$ V and $V_{IH(max)} = V_{CC} + 2$ V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3$ V (for V_{CC} range of 2.2 V–3.6 V) and $V_{CC} = 1.8$ V (for V_{CC} range of 1.65 V–2.2 V), $T_A = 25$ °C.
- Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
- The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

Parameter ^[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25$ °C, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	

Thermal Resistance

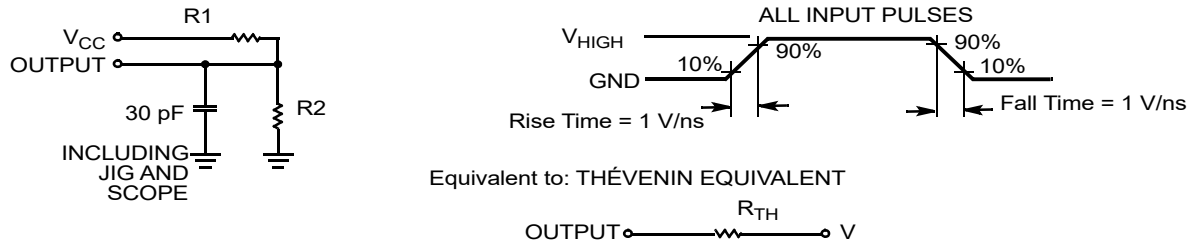
Parameter ^[9]	Description	Test Conditions	48-pin TSOP I	48-ball VFBGA	44-TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	60.07	36.92	65.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		9.73	13.55	13.96	

Note

- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms



Parameters	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	Ω
R2	10800	15385	1554	
R_{TH}	6000	8000	645	
V_{TH}	0.8	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

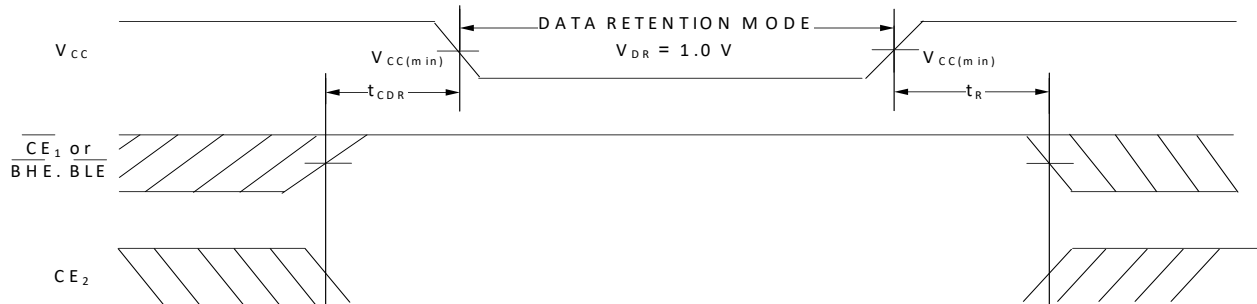
Parameter	Description	Conditions	Min	Typ ^[15]	Max	Unit
V_{DR}	V_{CC} for data retention		1	—	—	V
$I_{CCDR}^{[11, 12]}$	Data retention current (For 3.3V Typical Device)	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ $V_{CC} = 1.2 \text{ V}$	—	4.0	9.0	μA
		$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ $V_{CC} = 1.5 \text{ V}$	—	3.2	8.0	
		$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ $2.2 \text{ V} < V_{CC} \leq 3.6 \text{ V}$	—	1.4	6.5	
$I_{CCDR}^{[11, 12]}$	Data retention current (For 1.8V Typical Device)	$1.2 \text{ V} < V_{CC} \leq 2.2 \text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	—	5.0	9.0	
$t_{CDR}^{[13]}$	Chip deselect to data retention time	—	0	—	—	—
$t_R^{[14]}$	Operation recovery time	—	45/55	—	—	ns

Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25^\circ\text{C}$.
- Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
- I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC}(\text{min})$ and then brought down to V_{DR} .
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\text{min}) \geq 100 \mu\text{s}$ or stable at $V_{CC}(\text{min}) \geq 100 \mu\text{s}$.

Data Retention Waveform

Figure 7. Data Retention Waveform^[15]



Note

15. $\overline{BHE.BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

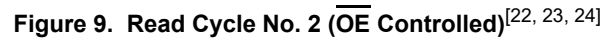
Switching Characteristics

Parameter ^[16]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read cycle time	45	–	55	–	ns
t _{AA}	Address to data valid/Address LOW to ERR valid	–	45	–	55	
t _{OHA}	Data hold from address change	10	–	10	–	
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to data valid/ $\overline{CE}$ LOW to ERR valid	–	45	–	55	
t _{DOE}	$\overline{OE}$ LOW to data valid/ $\overline{OE}$ LOW to ERR valid	–	22	–	25	
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[17]	5	–	5	–	
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[17, 18]	–	18	–	18	
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Low-Z ^[17]	10	–	10	–	
t _{HZCE}	$\overline{CE}_1$ HIGH and CE ₂ LOW to High-Z ^[17, 18]	–	18	–	18	
t _{PU}	$\overline{CE}_1$ LOW and CE ₂ HIGH to power-up	0	–	0	–	
t _{PD}	$\overline{CE}_1$ HIGH and CE ₂ LOW to power-down	–	45	–	55	
t _{DBE}	BLE / BHE LOW to data valid	–	45	–	55	
t _{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z ^[17]	5	–	5	–	
t _{HZBE}	BLE / $\overline{BHE}$ HIGH to High-Z ^[17, 18]	–	18	–	18	
Write Cycle ^[19, 20]						
t _{WC}	Write cycle time	45	–	55	–	ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to write end	35	–	40	–	
t _{AW}	Address setup to write end	35	–	40	–	
t _{HA}	Address hold from write end	0	–	0	–	
t _{SA}	Address setup to write start	0	–	0	–	
t _{PWE}	$\overline{WE}$ pulse width	35	–	40	–	
t _{BW}	BLE / $\overline{BHE}$ LOW to write end	35	–	40	–	
t _{SD}	Data setup to write end	25	–	25	–	
t _{HD}	Data hold from write end	0	–	0	–	
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[17, 18]	–	18	–	20	
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[17]	10	–	10	–	

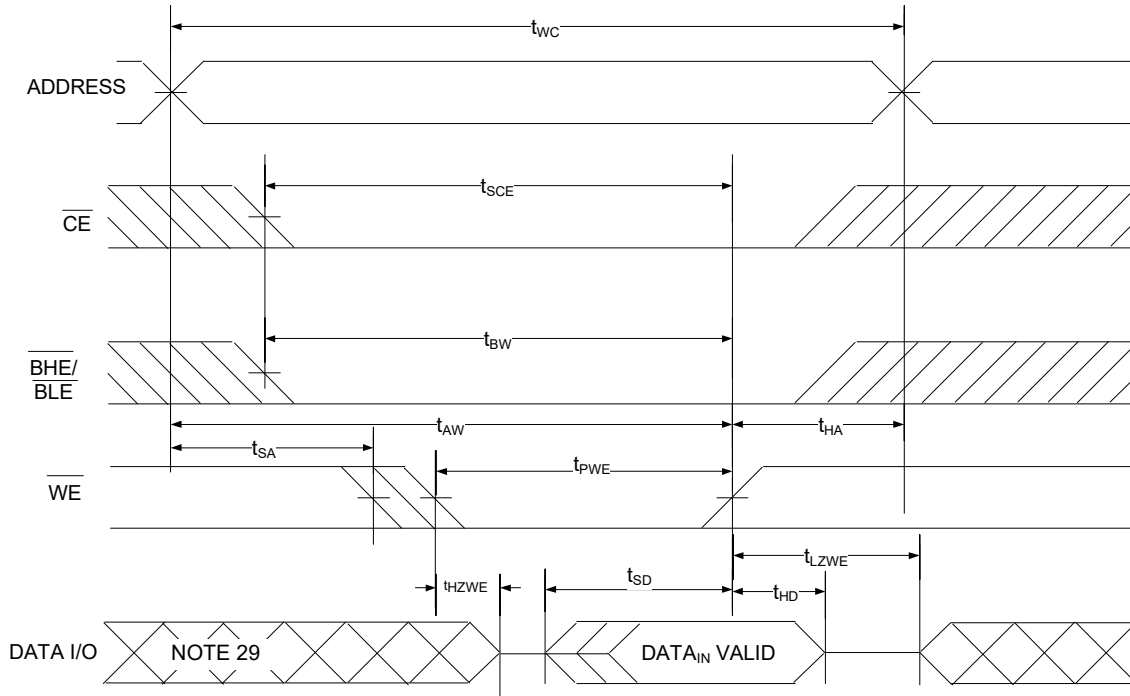
Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Figure 8. Read Cycle No. 1 of CY62157G (Address Transition Controlled)^[21, 22]

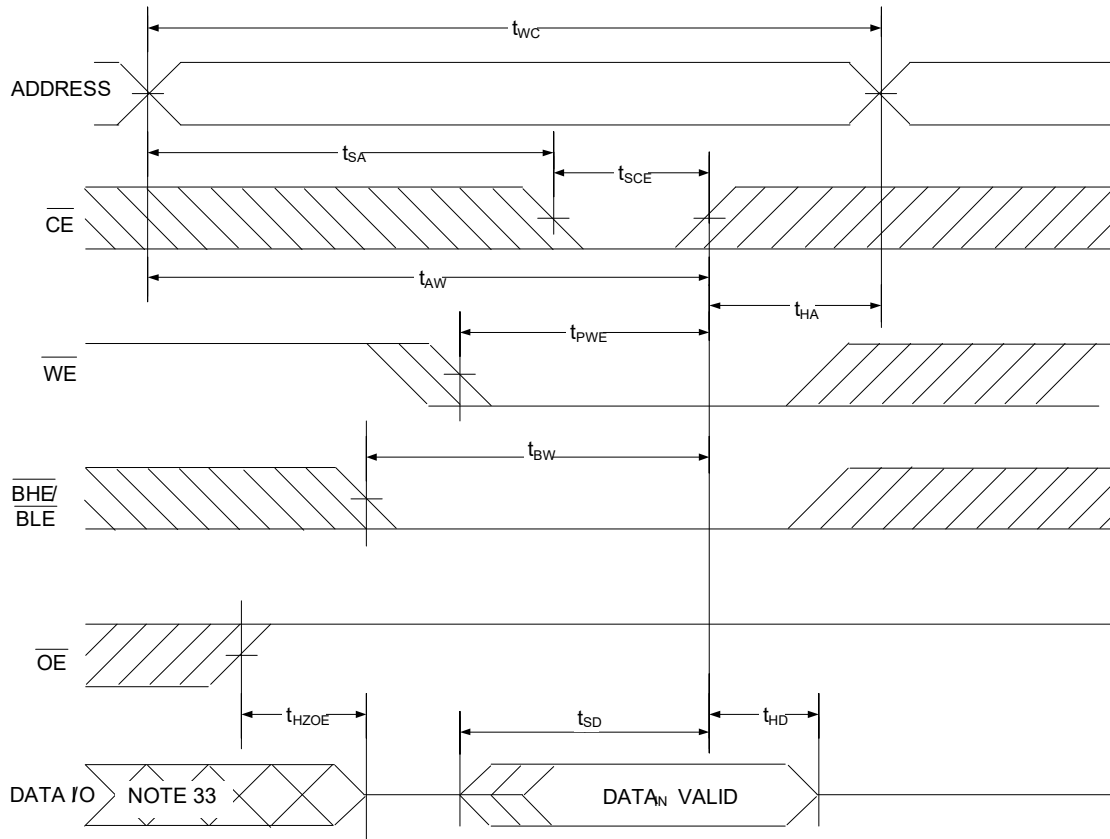


Switching Waveforms (continued)

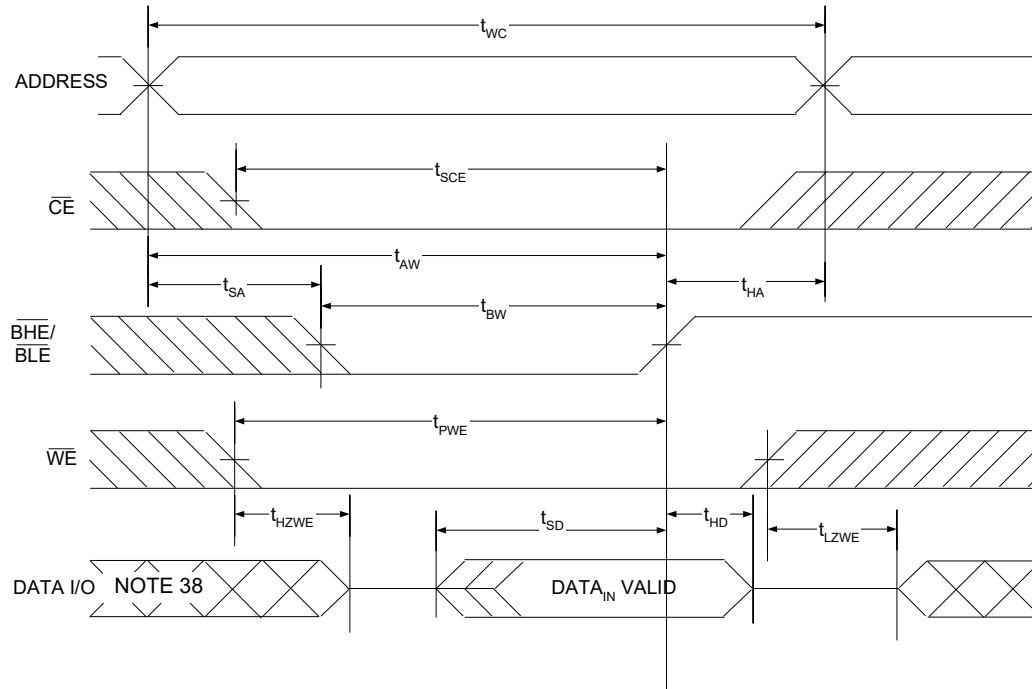
Figure 10. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [25, 26, 27, 28]

Notes

25. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
26. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
28. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

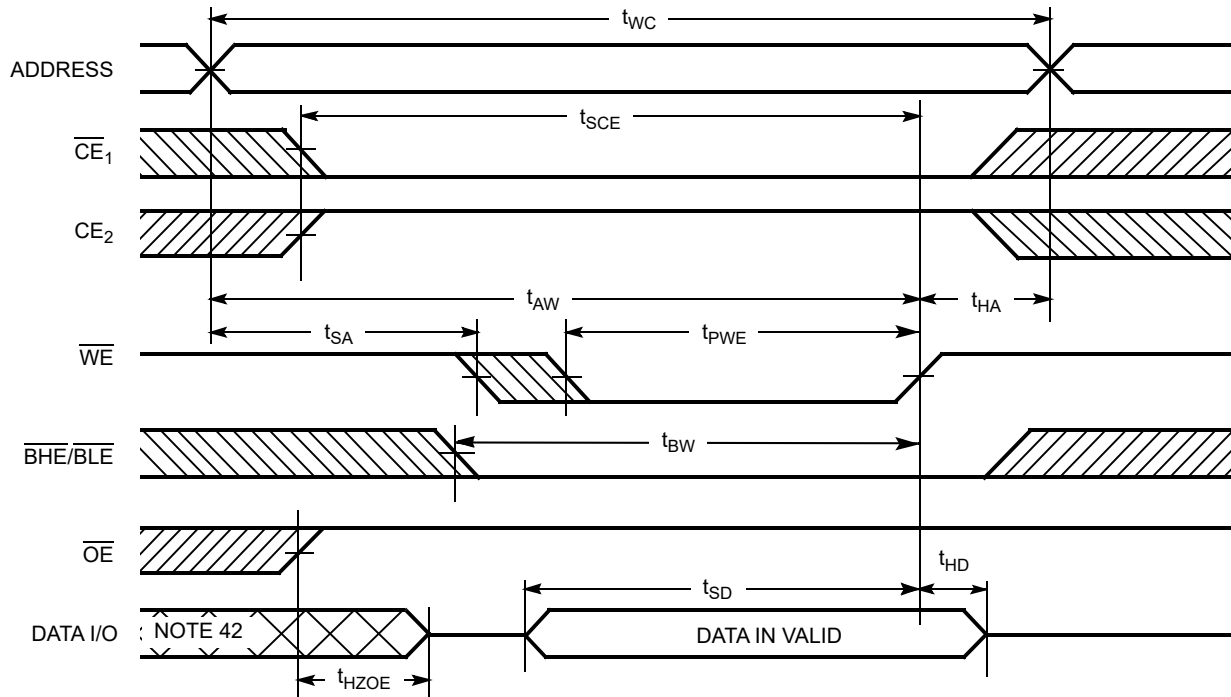
Figure 11. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[30, 31, 32]

Notes

30. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
31. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Figure 12. Write Cycle No. 3 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) [34, 35, 36, 37]

Notes

34. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
35. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
36. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
37. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .
38. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 4 ($\overline{WE}$ Controlled)^[39, 40, 41]

Notes

39. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

40. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

41. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

42. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table – CY62157G/CY62157GE

BYTE ^[43]	CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power	Configuration
X ^[44]	H	X ^[44]	X	X	X	X	High-Z	Deselect/Power-down	Standby (I _{SB})	1M × 8/512K × 16
X	X ^[44]	L	X	X	X	X	High-Z	Deselect/Power-down	Standby (I _{SB})	1M × 8/512K × 16
X	X ^[44]	X ^[44]	X	X	H	H	High-Z	Deselect/Power-down	Standby (I _{SB})	512K × 16
H	L	H	H	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})	512K × 16
H	L	H	H	L	H	L	Data Out (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})	512K × 16
H	L	H	H	L	L	H	High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})	512K × 16
H	L	H	H	H	L	H	High-Z	Output disabled	Active (I _{CC})	512K × 16
H	L	H	H	H	H	L	High-Z	Output disabled	Active (I _{CC})	512K × 16
H	L	H	H	H	L	L	High-Z	Output disabled	Active (I _{CC})	512K × 16
H	L	H	L	X	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})	512K × 16
H	L	H	L	X	H	L	Data In (I/O ₀ –I/O ₇); High-Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})	512K × 16
H	L	H	L	X	L	H	High-Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})	512K × 16
L	L	H	H	L	X	X	Data Out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})	1M × 8
L	L	H	H	H	X	X	High-Z	Output disabled	Active (I _{CC})	1M × 8
L	L	H	L	X	X	X	Data In (I/O ₀ –I/O ₇)	Write	Active (I _{CC})	1M × 8

ERR Output – CY62157GE

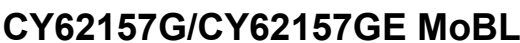
Output ^[45]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

Notes

43. This pin is available only in the 48-pin TSOP I package. Tie the $\overline{\text{BYTE}}$ to V_{CC} to configure the device in the 512K × 16 option. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the $\overline{\text{BYTE}}$ signal to V_{SS}.

44. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

45. ERR is an Output pin. If not used, this pin should be left floating.



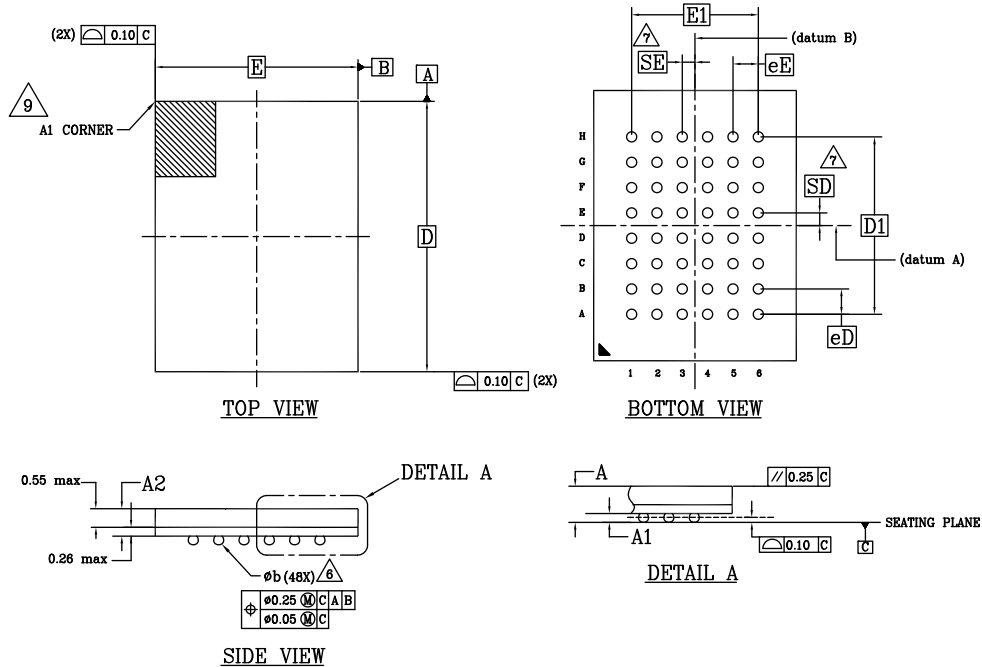
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157G30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Industrial
	CY62157G30-45BVXIT			
	CY62157GE30-45BVXI			
	CY62157G30-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
	CY62157G30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free)	
	CY62157GE30-45ZXI			
55	CY62157G18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62157G18-55BVXIT			

Diagram illustrating the structure of the MoBL SRAM part number, showing the relationship between the part number fields and their corresponding specifications:

- CY**: Company ID: CY = Cypress
- 621**: Family Code: 621 = MoBL SRAM family
- 5**: Density: 5 = 8-Mbit
- 7**: Bus Width: 7 = x 16
- G**: Process Technology: G = 65 nm
- E**: ERR Output: Single-bit error correction indicator
- XX**: Voltage Range: XX = 30 or 18
30 = 3 V typ; 18 = 1.8 V typ
- XX**: Speed Grade: XX = 45 or 55
45 = 45 ns; 55 = 55 ns
- XX**: Package Type: XX = BV or ZS or Z
BV = 48-ball VFBGA; ZS = 44-pin TSOP II; Z = 48-pin TSOP I
- X**: Pb-free
- I**: Temperature Grade: I = Industrial
- X**: blank or T
blank = Bulk; T = Tape and Reel

Package Diagrams

Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

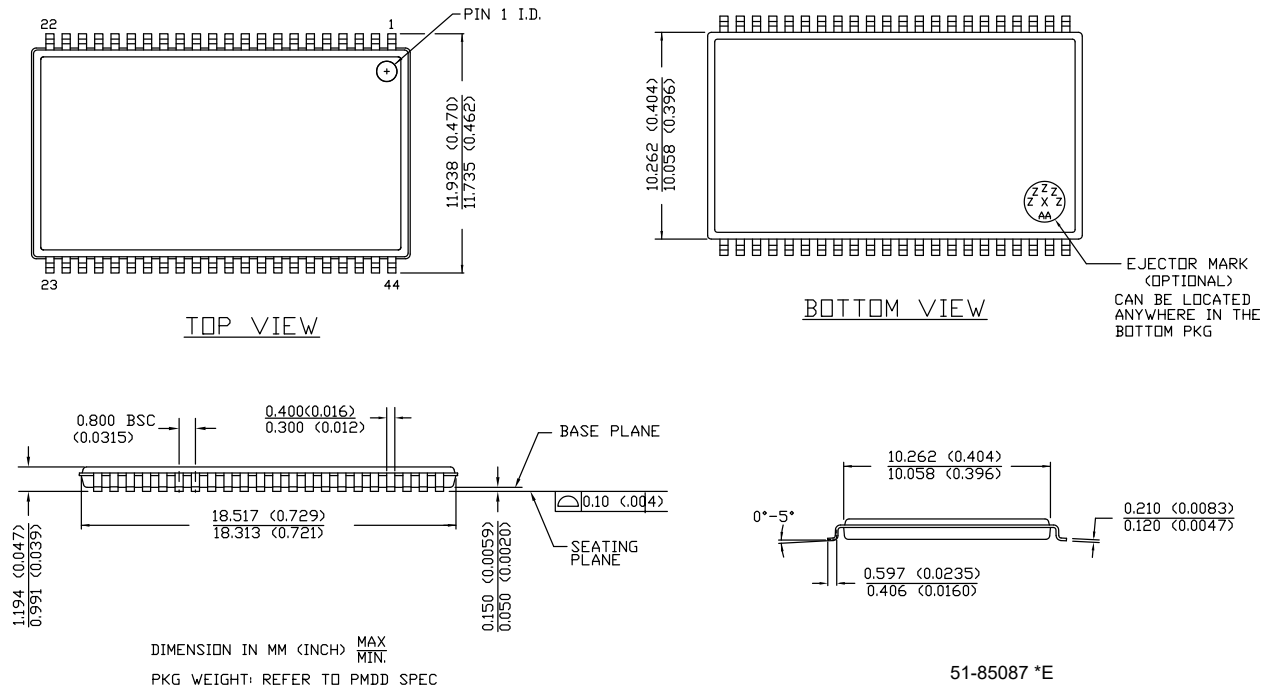
NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- Ø b REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- ** INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *1

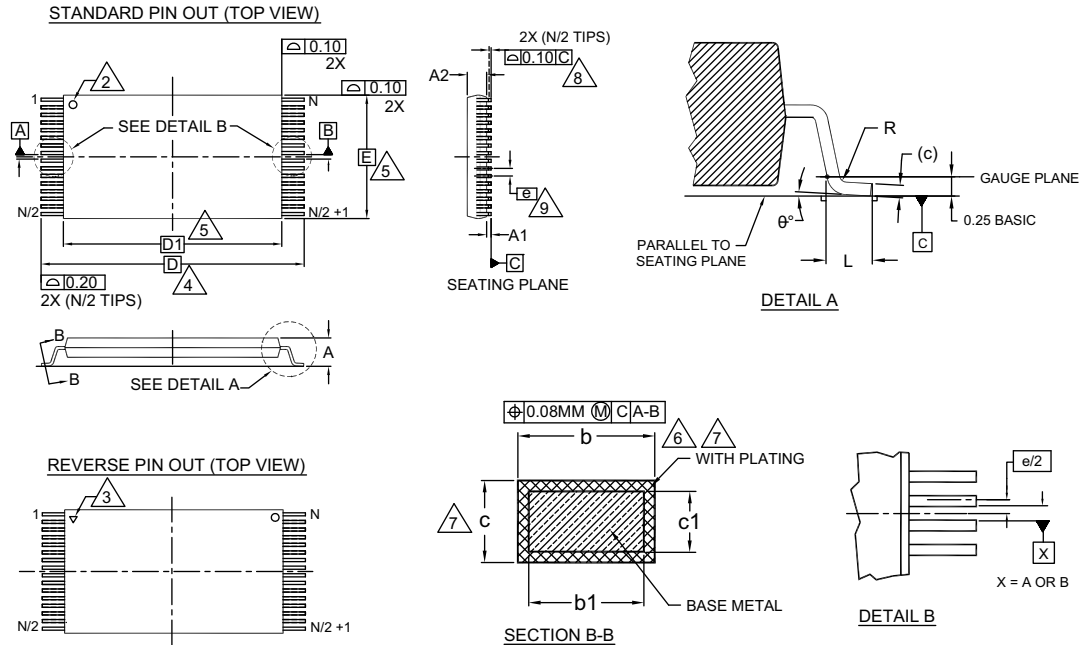
Package Diagrams (continued)

Figure 15. 44-pin TSOP II Package Outline, 51-85087



Package Diagrams (continued)

Figure 16. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE $\square C$. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Table 1. Acronyms used in this Document

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
ECC	error-correcting code
I/O	input/output
OE	output enable
SRAM	static random access memory
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
WE	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62157G/CY62157GE MoBL, 8-Mbit (512K × 16-bits) Static RAM with Error-Correcting Code (ECC)
Document Number: 002-27323

Rev.	ECN No.	Submission Date	Description of Change
*C	6814364	02/28/2020	Release to web.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2019-2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.