

CMPA1D1J001S

12.7 – 18 GHz, 1 W GaN HPA

Description

The CMPA1D1J001S is a 1W package MMIC HPA utilizing the high performance, 0.15um GaN on SiC production process. The CMPA1D1J001S operates from 12.7-18 GHz and supports both radar and communication applications within both military and commercial markets. The CMPA1D1J001S achieves 1 W of saturated output power with 23 dB of large signal gain and typically 30% power-added efficiency under CW operation.

Packaged in a 4x3 mm plastic overmold QFN, the CMPA1D1J001S provides superior broadband performance and environmental robustness in a small form factor allowing customers to improve SWaP-C benchmarks in their next-generation systems.

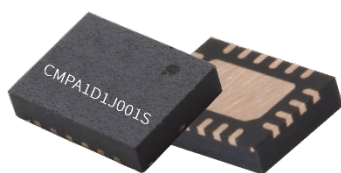


Figure 1. CMPA1D1J001S

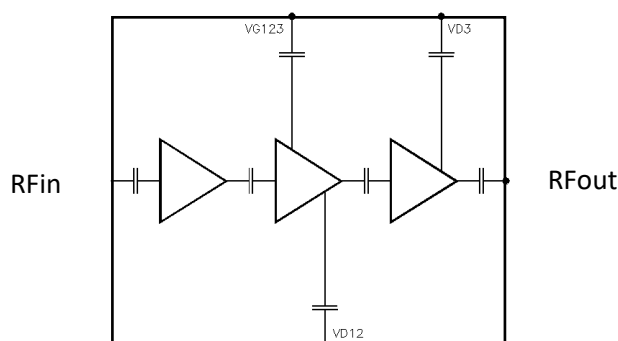


Figure 2. Functional Block Diagram

Features

- Psat: 1 W
- PAE: 30 %
- LSG: 23 dB
- S21: 27 dB
- S11: -10 dB
- S22: -8 dB
- CW operation
- Small 4 x 3 mm footprint

Note: Features are typical performance across frequency under 25C operation. Please reference performance charts for additional information.

Applications

- Military and Commercial Radar and Communications
- General Purpose Broadband Amplifier



Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	84	
Drain Voltage	V_D	V	28	
Gate Voltage	V_G	V	-8, +2	
Drain Current	I_D	A	0.8	
Gate Current	I_G	mA	1.0	
Input Power	P_{in}	dBm	10	
Dissipated Power	P_{diss}	W	4.4	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	260	30 seconds
Junction Temperature	T_J	°C	225	
Output Mismatch Stress	VSWR	Ψ	5:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	V_d	V	22	
Gate Voltage	V_g	V	-2.0	
Drain Current	I_{dq}	mA	30	
Input Power	P_{in}	dBm	8	
Case Temperature	T_{case}	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: $V_d=22$ V, $I_{dq}=30$ mA, CW, $P_{in} = 8$ dBm, $T_{base}=25$ °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		13		18	
Output Power	dBm	12.7		30.5		
		15.5		31.5		
		18		30.5		
Power-added Efficiency	%	12.7		28		
		15.5		35		
		18		34		
LSG	dB	12.7		22.5		
		15.5		23.5		
		18		22.5		
Small-Signal Gain	dB	12.7		27		Pin = -20 dBm
		15.5		30		
		18		24		
Input Return Loss	dB			-10		Pin = -20 dBm
Output Return Loss	dB			-8		Pin = -20 dBm

Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25\text{ }^{\circ}\text{C}$, Frequency: 15.5GHz

Figure 3: Pout v. Frequency v. Temperature

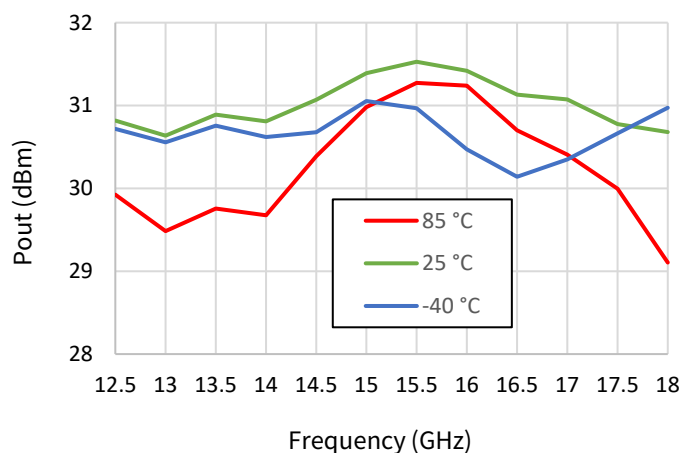


Figure 4: PAE v. Frequency v. Temperature

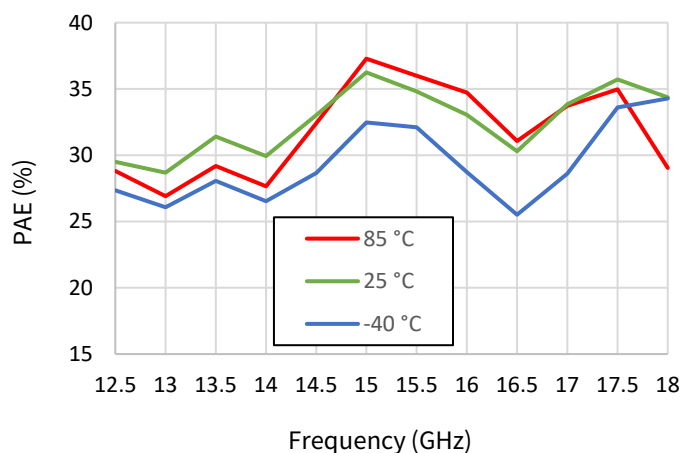


Figure 5: Id v. Frequency v. Temperature

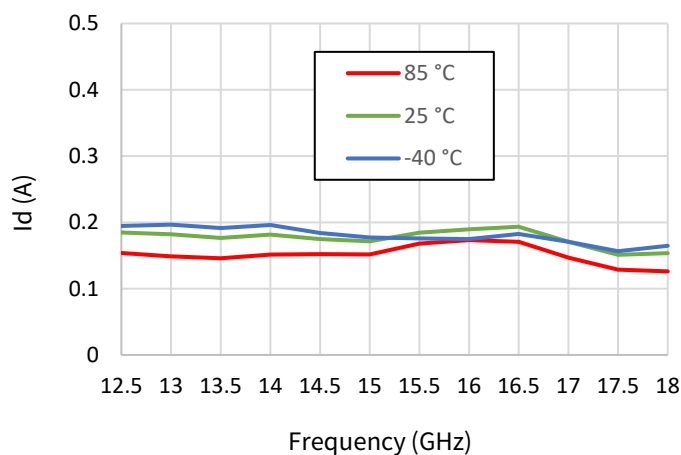


Figure 6: Ig v. Frequency v. Temperature

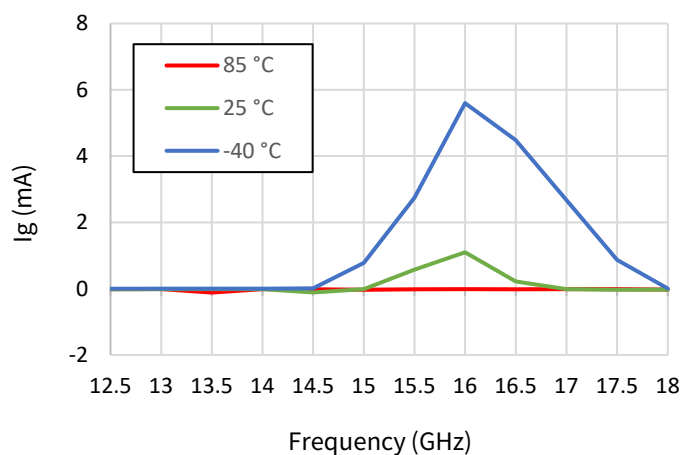
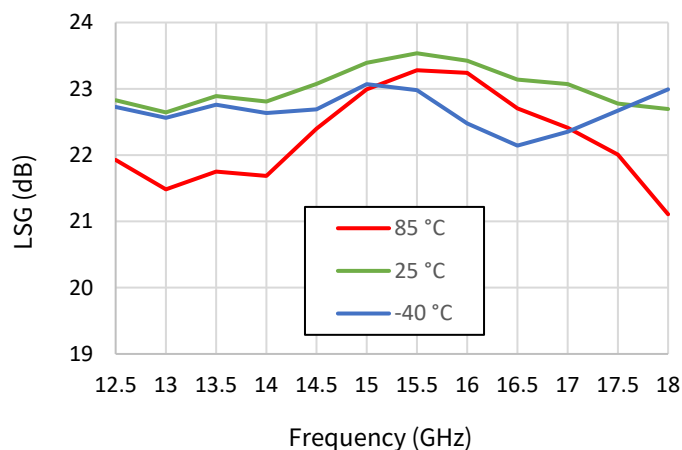


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=22 V, Idq=30mA, CW, Pin = 8 dBm, T_{base}=25°C, Frequency: 15.5GHz

Figure 8: Pout v. Frequency v. Vd

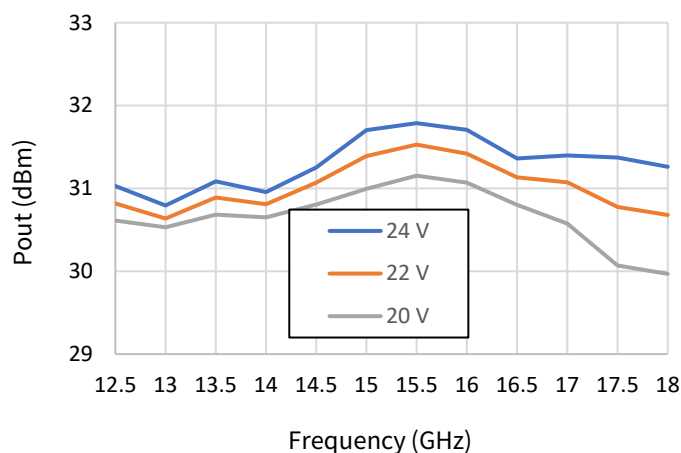


Figure 9: PAE v. Frequency v. Vd

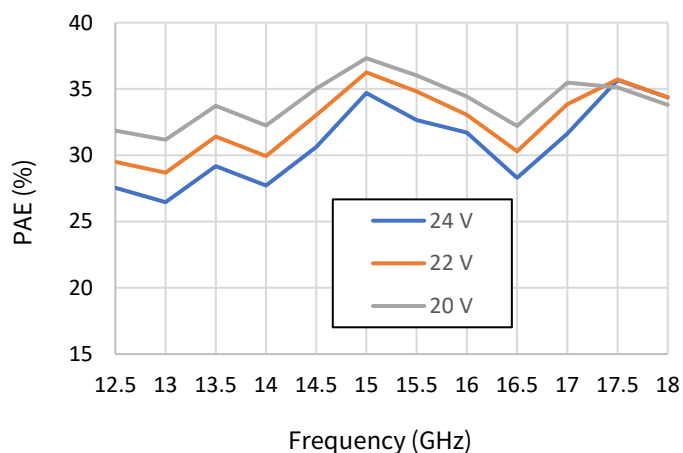


Figure 10: Id v. Frequency v. Vd

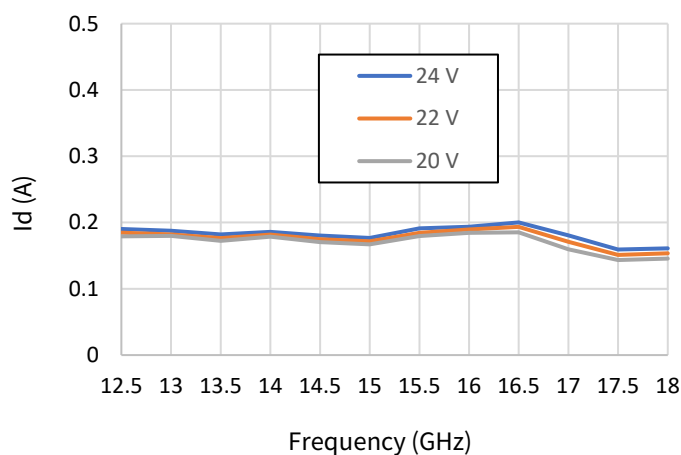


Figure 11: Ig v. Frequency v. Vd

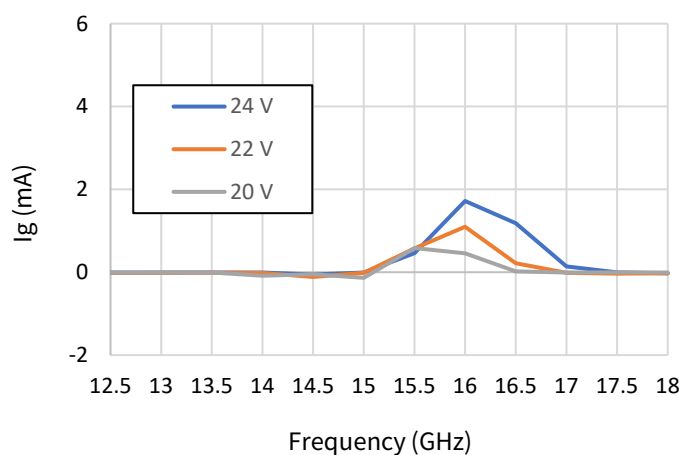
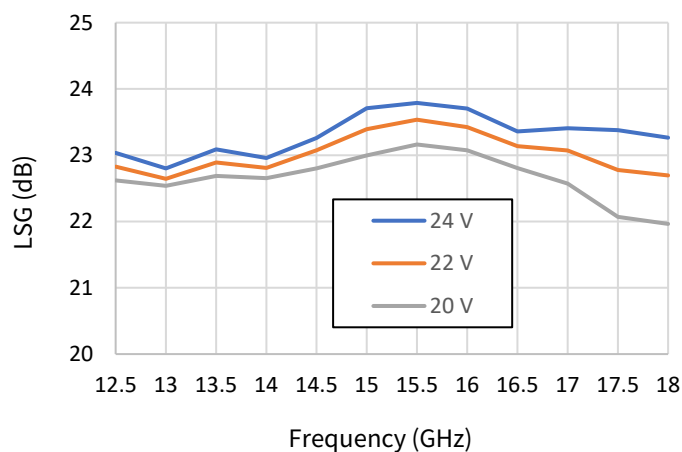


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in}=8\text{ dBm}$, $T_{base}=25^\circ\text{C}$, Frequency: 15.5GHz

Figure 13: Pout v. Frequency v. Idq

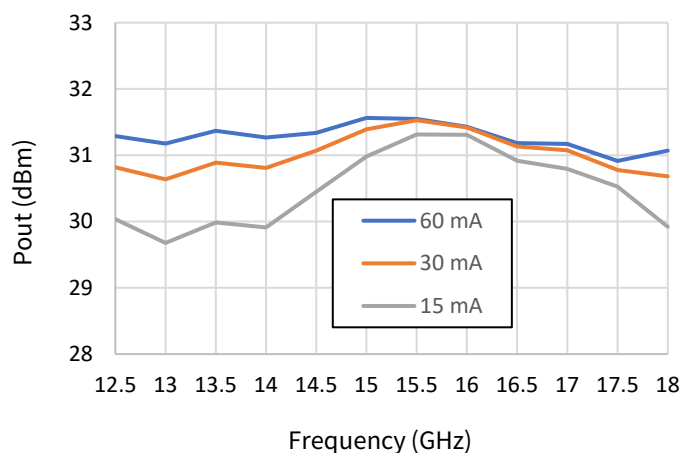


Figure 14: PAE v. Frequency v. Idq

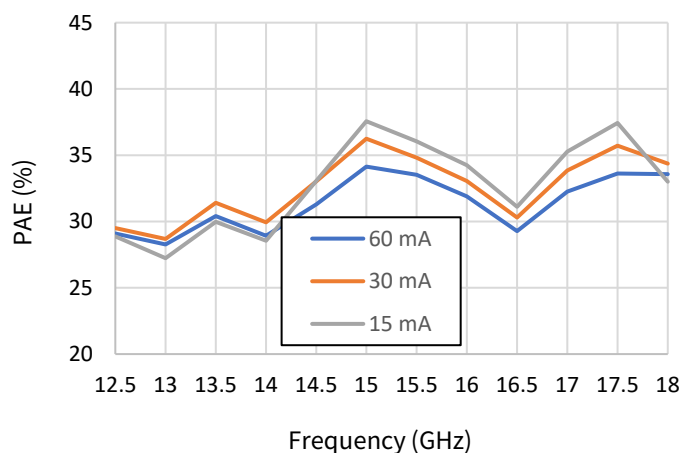


Figure 15: Id v. Frequency v. Idq

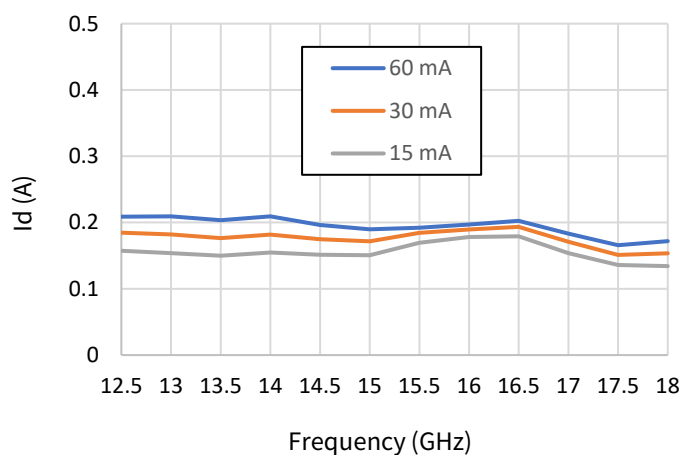


Figure 16: Ig v. Frequency v. Idq

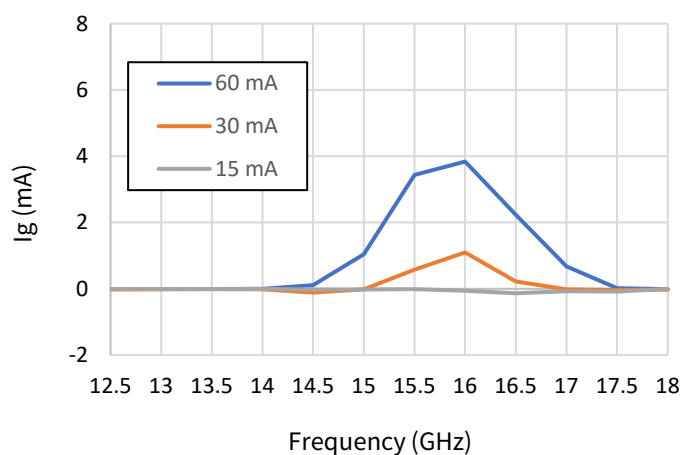
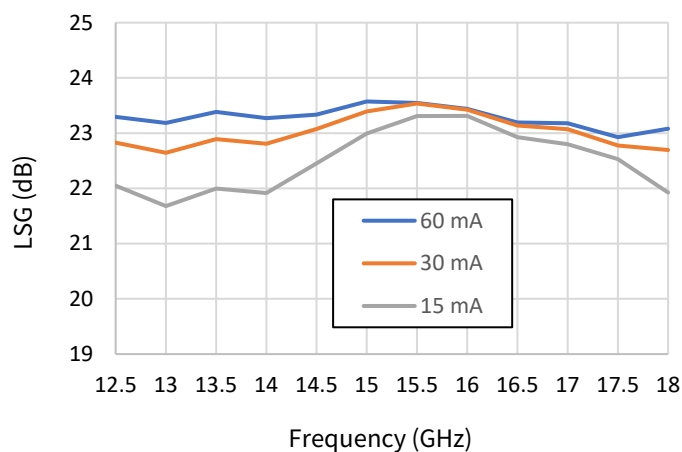


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in}=8\text{ dBm}$, $T_{base}=25^\circ\text{C}$, Frequency: 15.5GHz

Figure 18: Pout v. Pin v. Frequency

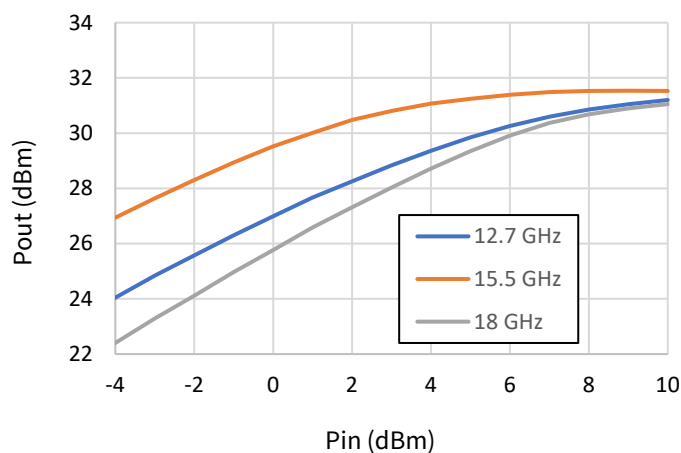


Figure 19: PAE v. Pin v. Frequency

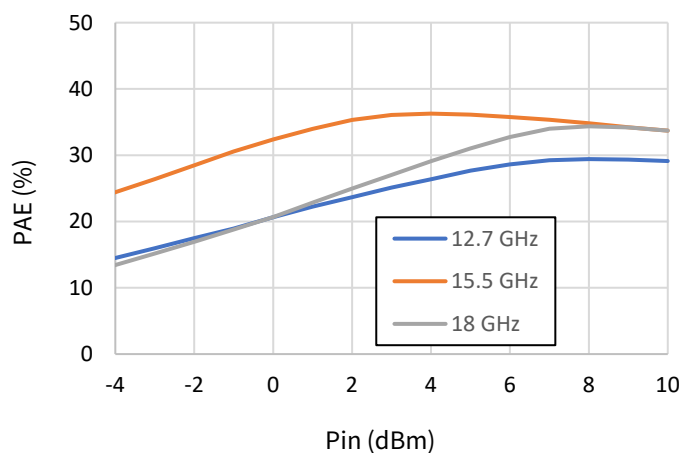


Figure 20: Id v. Pin v. Frequency

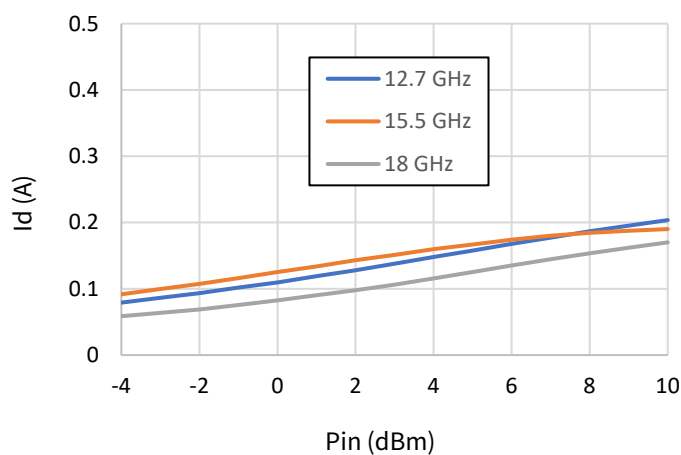


Figure 21: Ig v. Pin v. Frequency

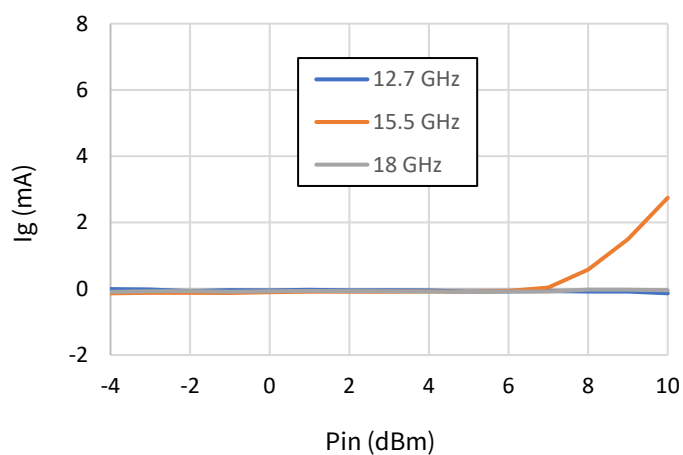
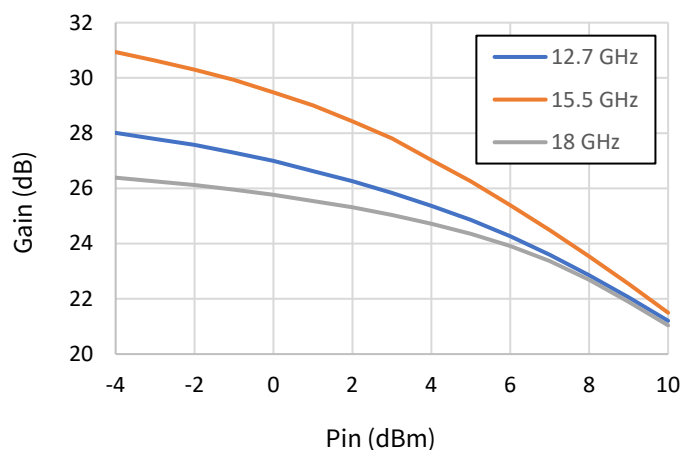


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25\text{ }^{\circ}\text{C}$, Frequency: 15.5GHz

Figure 23: Pout v. Pin v. Temperature

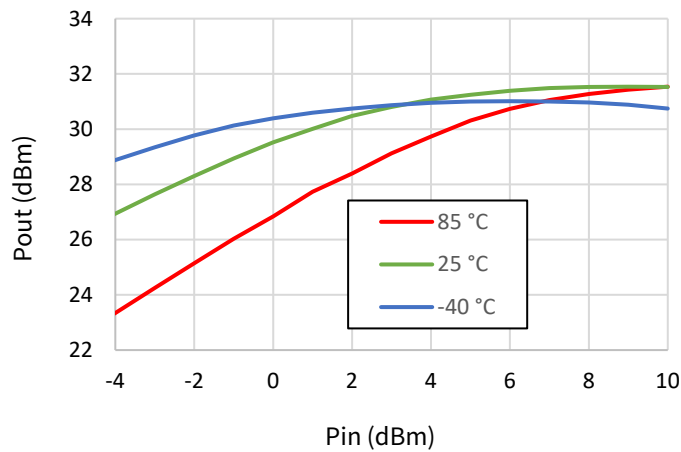


Figure 24: PAE v. Pin v. Temperature

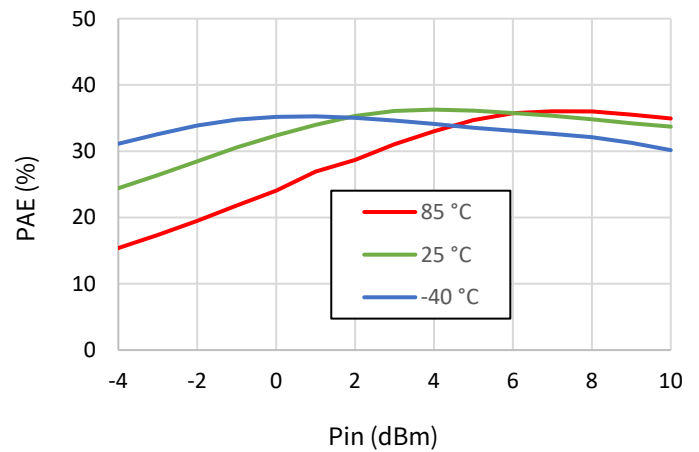


Figure 25: Id v. Pin v. Temperature

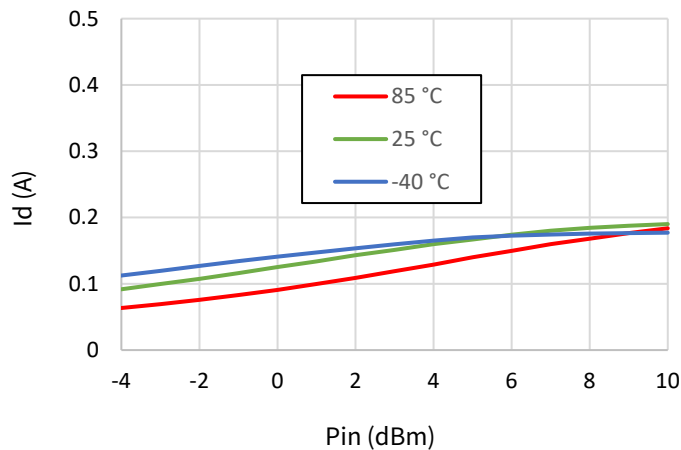


Figure 26: Ig v. Pin v. Temperature

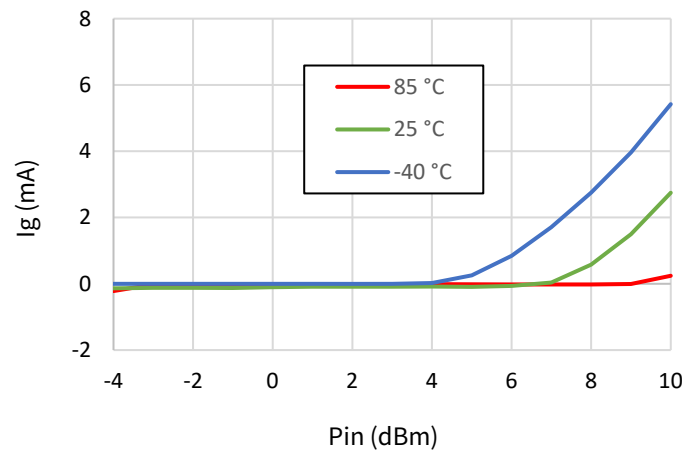
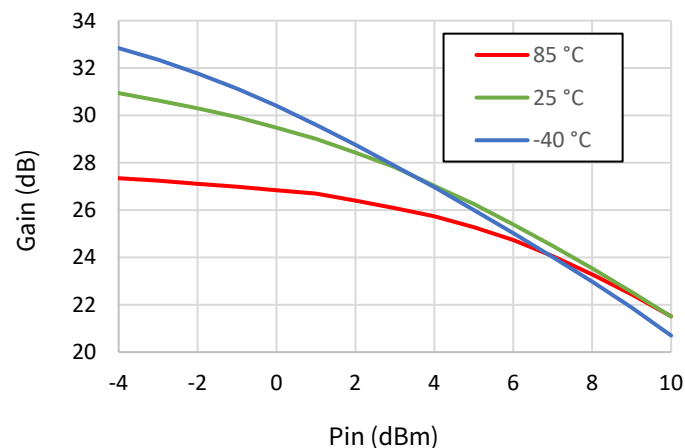


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=22 V, Idq=30mA, CW, Pin = 8 dBm, T_{base}=25 °C, Frequency: 15.5GHz

Figure 28: Pout v. Pin v. Vd

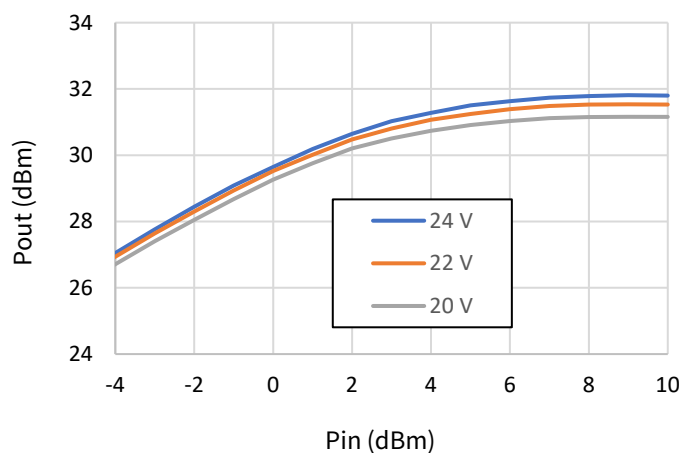


Figure 29: PAE v. Pin v. Vd

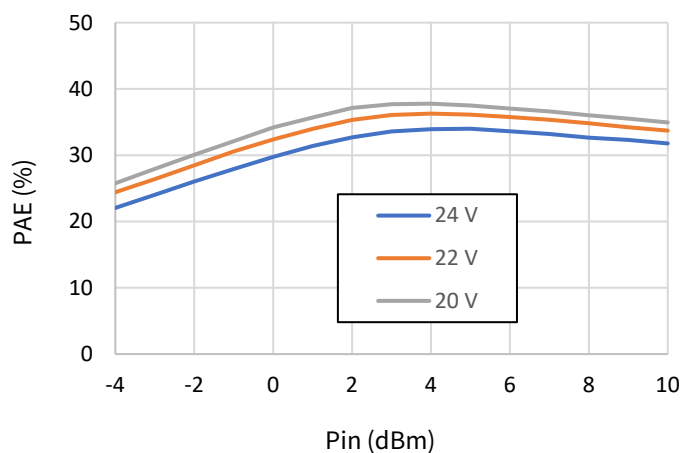


Figure 30: Id v. Pin v. Vd

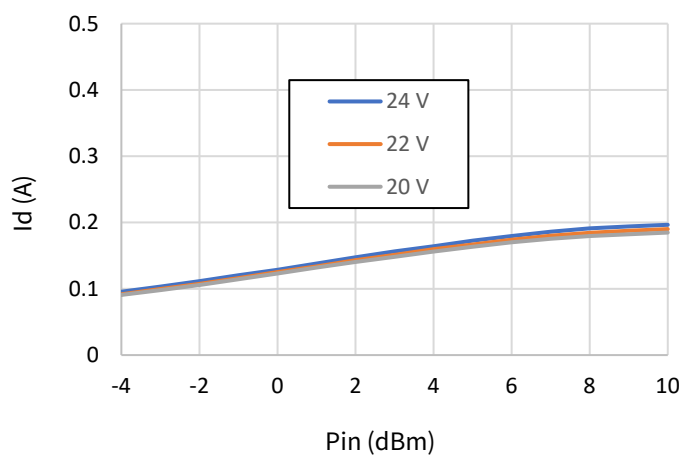


Figure 31: Ig v. Pin v. Vd

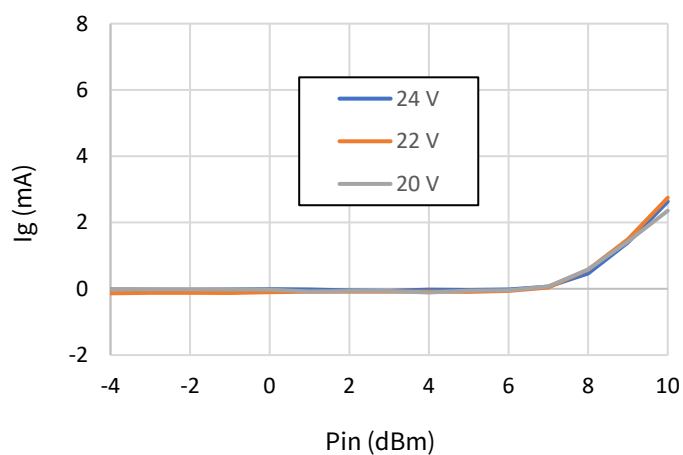
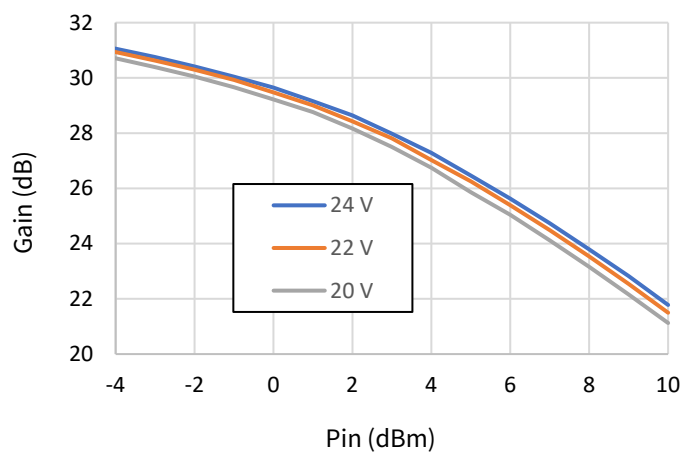
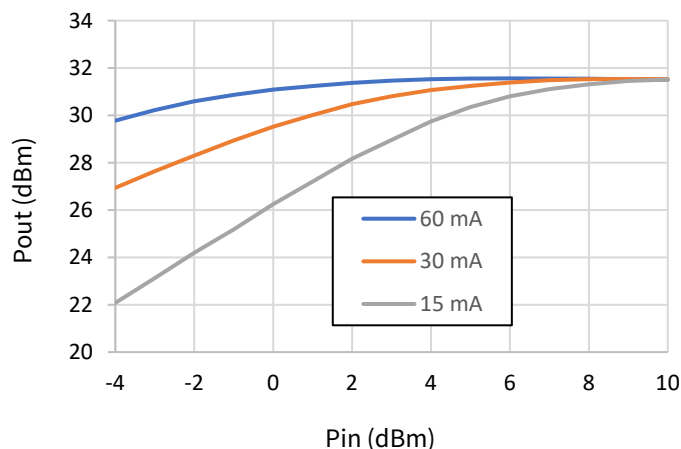
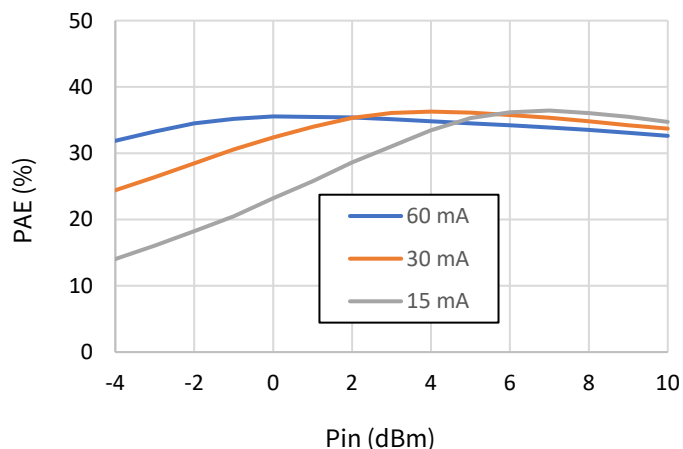
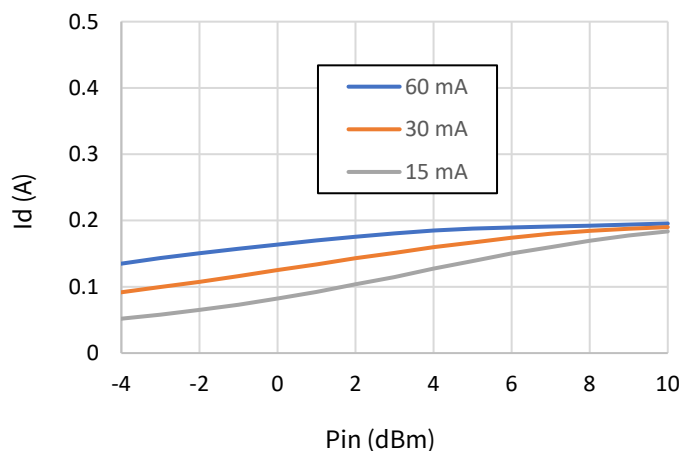
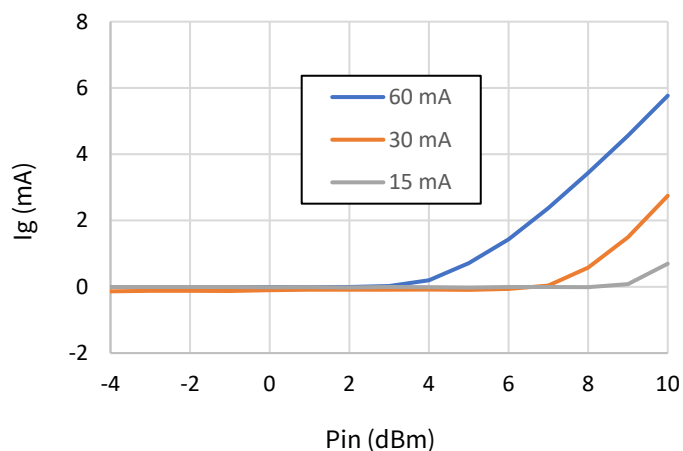
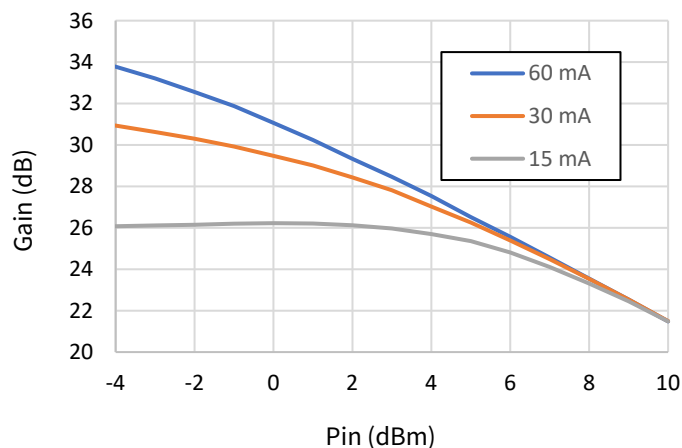


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25^\circ\text{C}$, Frequency: 15.5GHz

Figure 33: P_{out} v. P_{in} v. I_{dq} **Figure 34: PAE v. P_{in} v. I_{dq}** **Figure 35: I_d v. P_{in} v. I_{dq}** **Figure 36: I_g v. P_{in} v. I_{dq}** **Figure 37: Gain v. P_{in} v. I_{dq}** 

Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25^\circ\text{C}$, Frequency: 15.5GHz

Figure 38: S21 v. Frequency v. Temperature

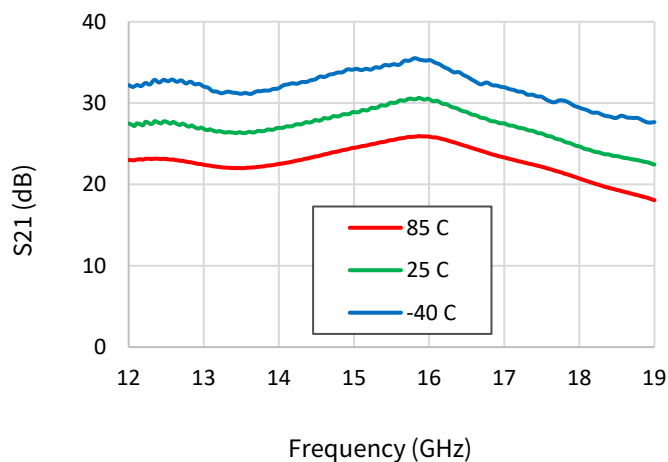


Figure 39: S21 v. Frequency v. Vd

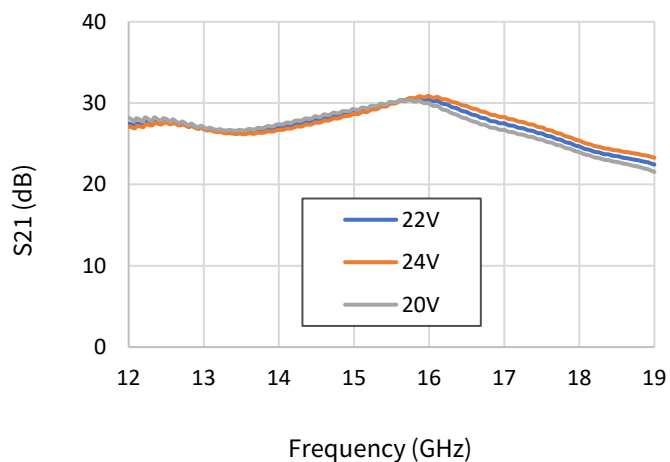


Figure 40: S11 v. Frequency v. Temperature

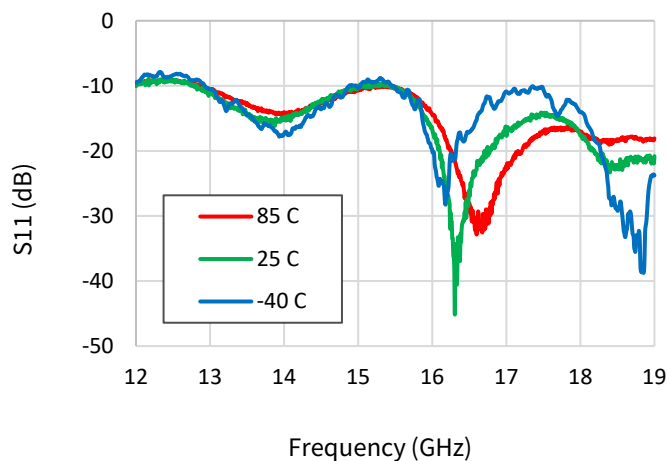


Figure 41: S11 v. Frequency v. Vd

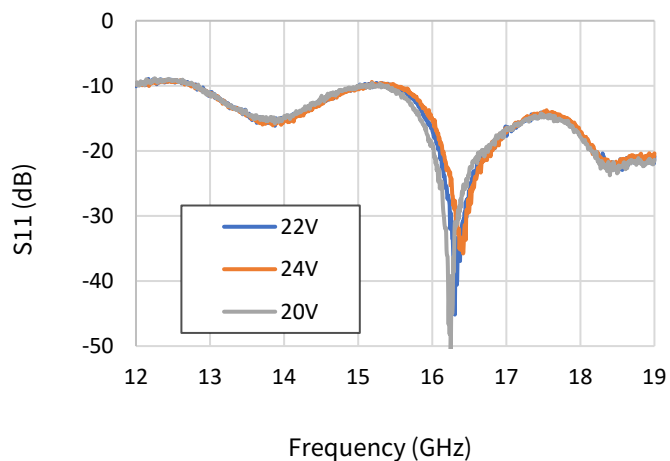


Figure 42: S22 v. Frequency v. Temperature

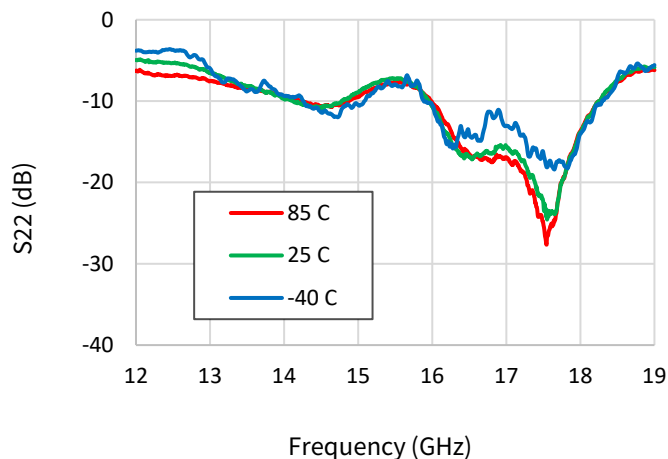
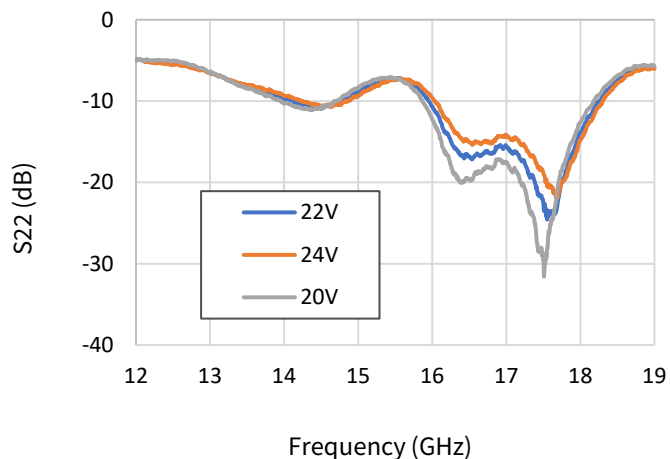


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25^\circ\text{C}$, Frequency: 15.5GHz

Figure 44: S21 v. Frequency v. Idq

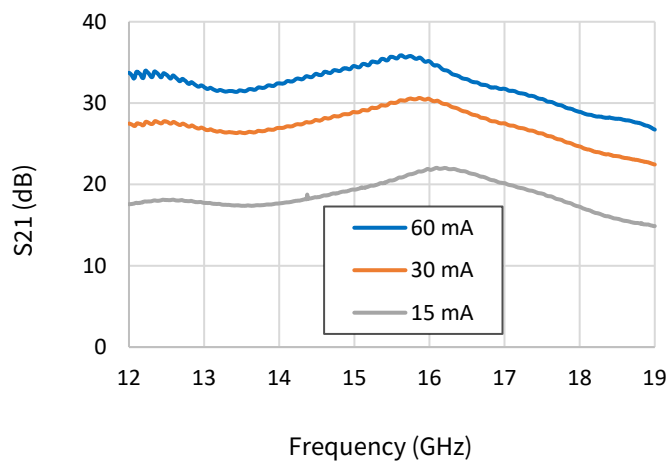


Figure 45: S11 v. Frequency v. Idq

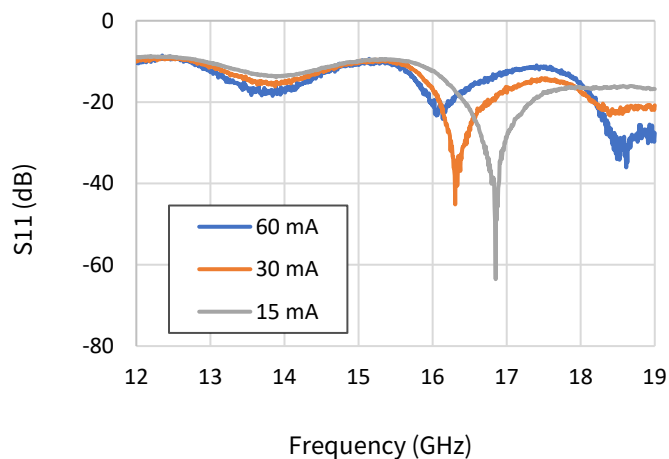
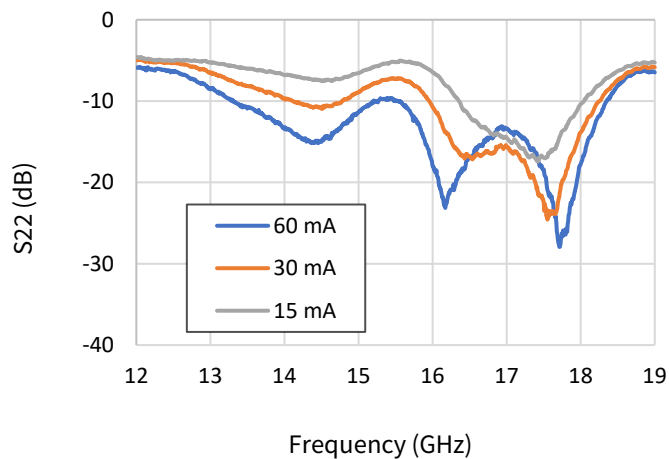


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: $V_d=22\text{ V}$, $I_{dq}=30\text{ mA}$, CW, $P_{in} = 8\text{ dBm}$, $T_{base}=25\text{ }^{\circ}\text{C}$, Frequency: 15.5GHz, Tone Spacing = 10 MHz, $T_{base}=25\text{ }^{\circ}\text{C}$

Figure 47: IM3 v. Pout/tone v. Frequency

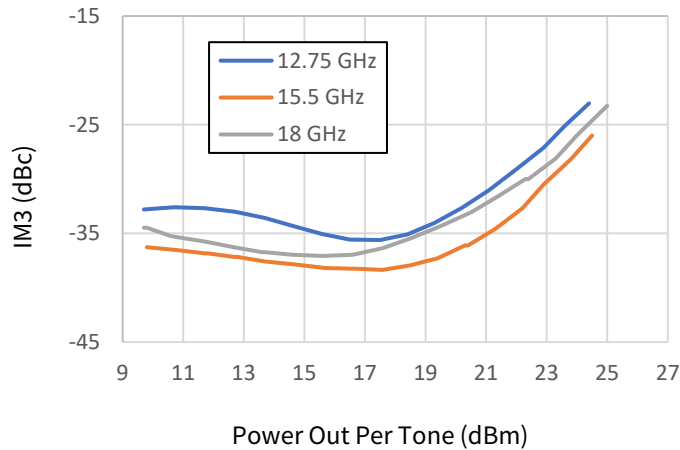


Figure 48: IM5 v. Pout/tone v. Frequency

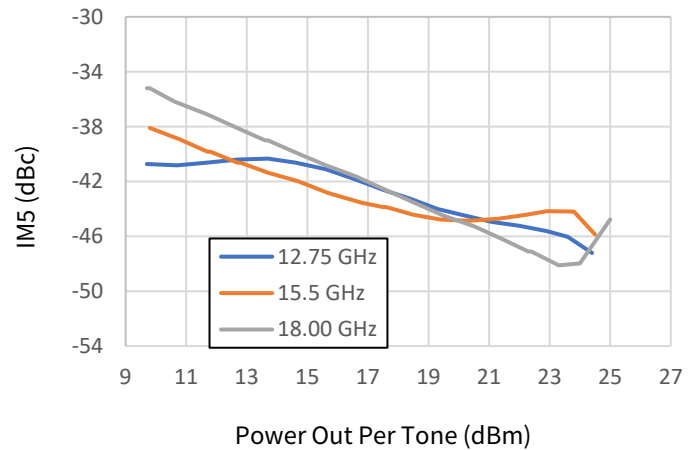


Figure 49: IM3 v. Pout/tone v. Temperature

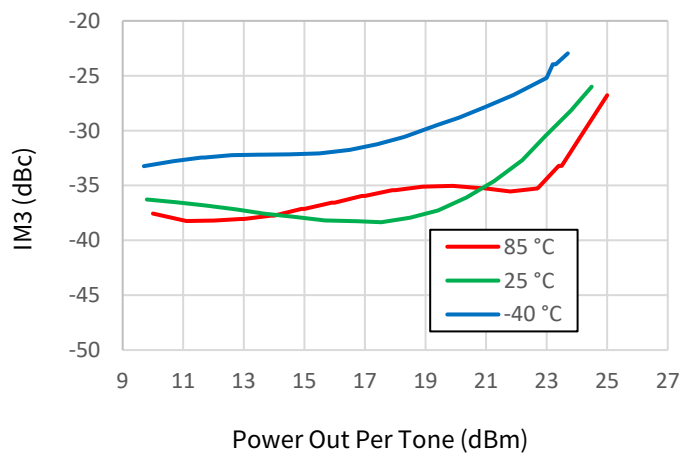


Figure 50: IM5 v. Pout/tone v. Temperature

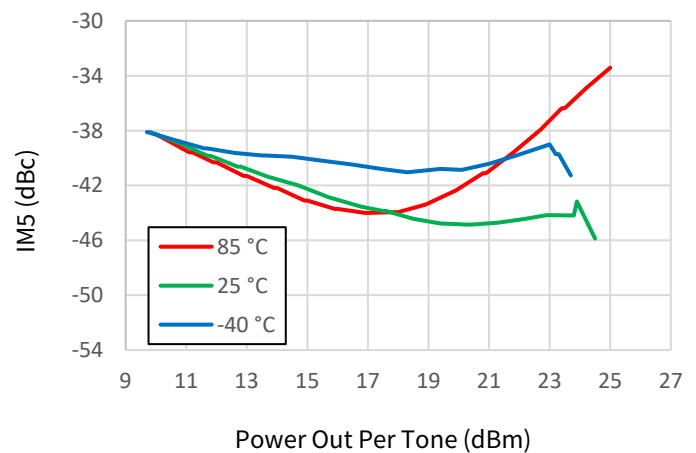


Figure 51: IM3 v. Pout/tone v. Idq

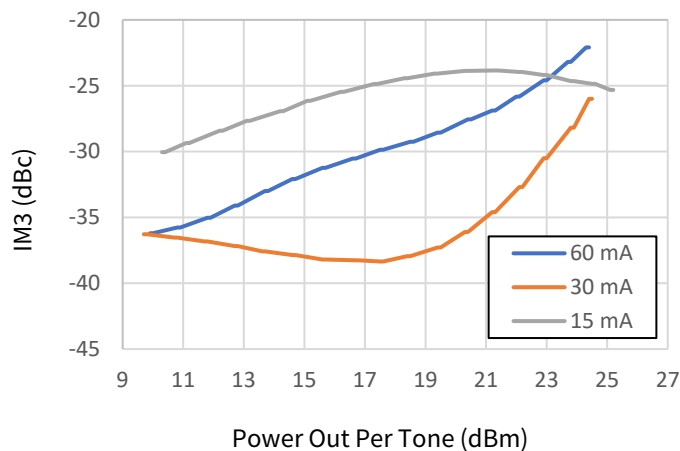
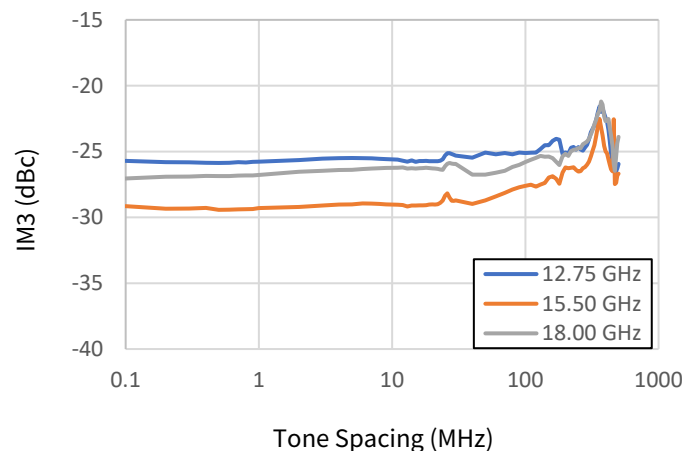


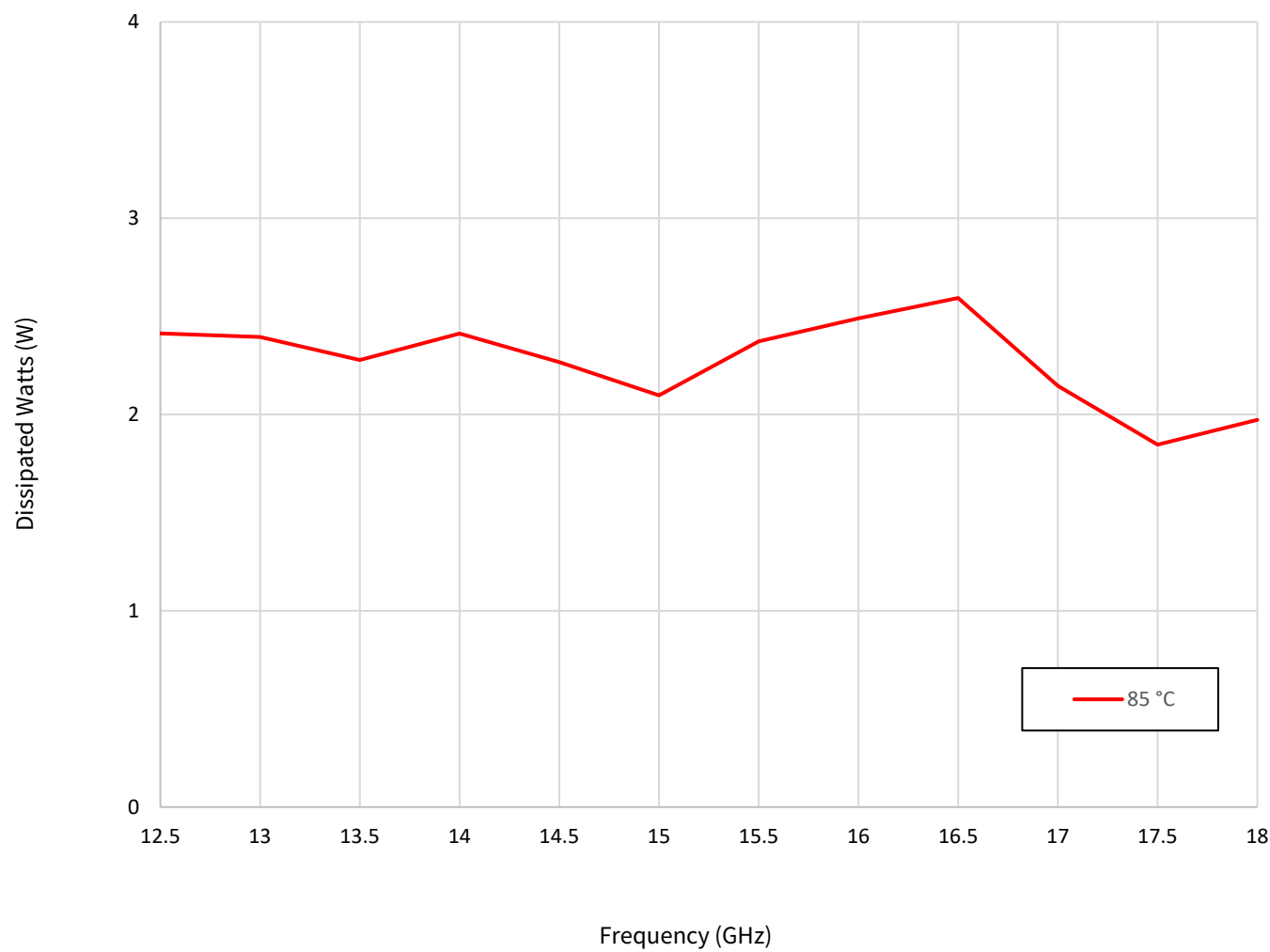
Figure 52: IM3 v. Tone Spacing v. Frequency



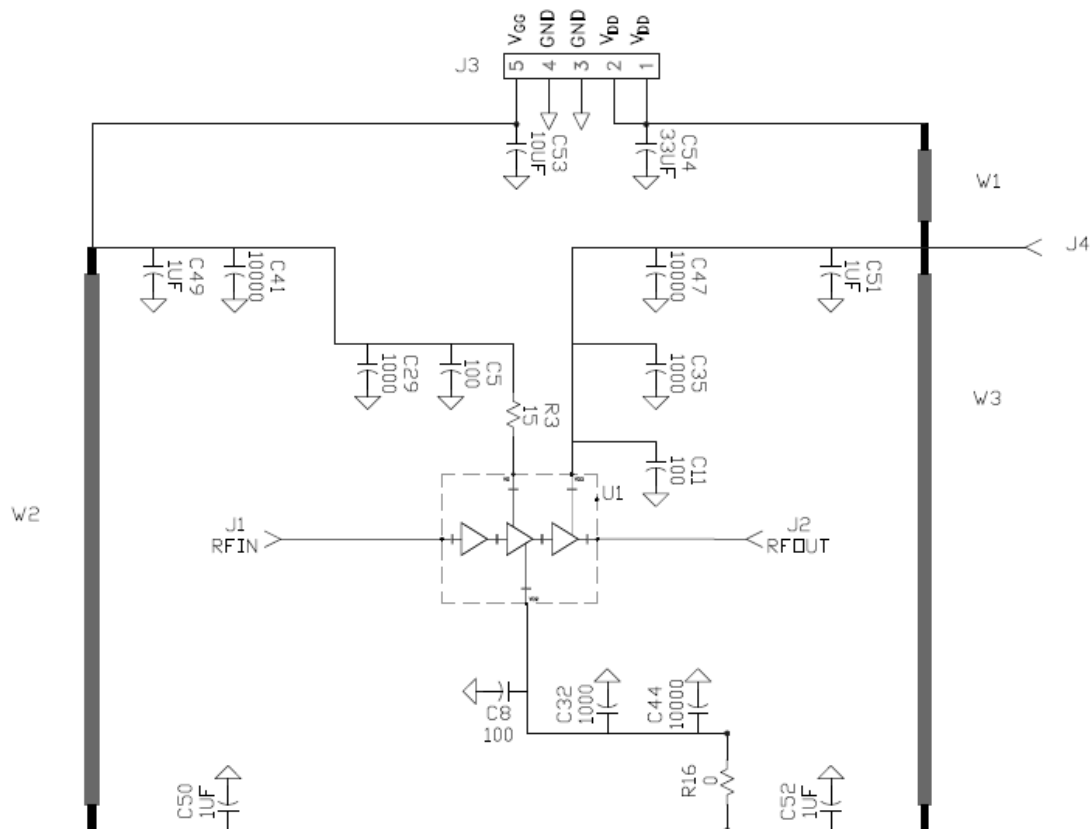
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	161.3	Freq = 15.5 GHz, V_d = 22 V, I_{dq} = 30 mA, I_{drive} = 190 mA, P_{in} = 8 dBm, P_{out} = 31 dBm, P_{diss} = 2.4 W, T_{case} = 85°C, CW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	31.8	

Power Dissipation v. Frequency (Tcase = 85°C)



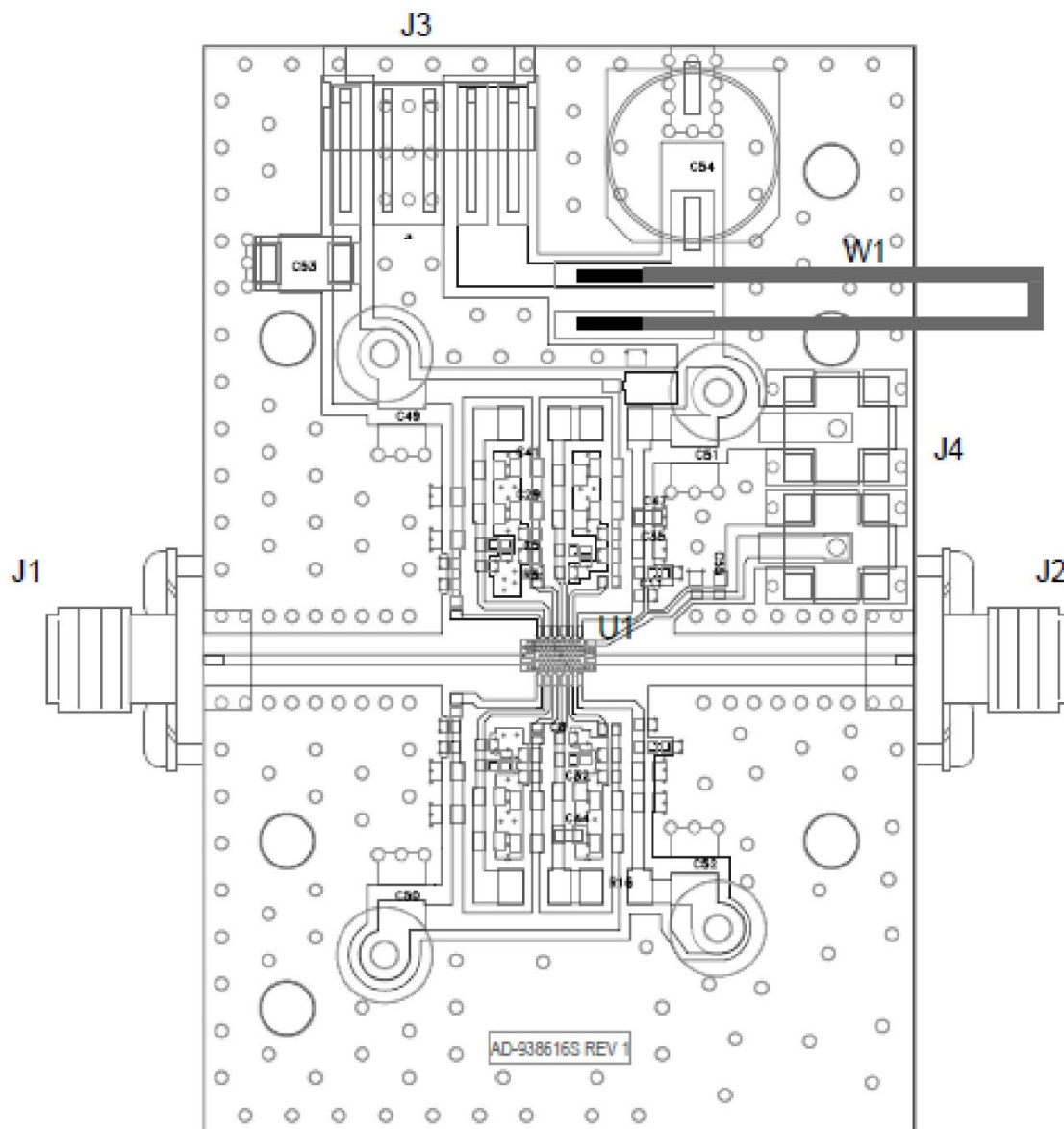
CMPA1D1J001S-AMP1 Evaluation Board Schematic Drawing



CMPA1D1J001S-AMP1 Evaluation Board Bill of Materials

Reference Designator	Description	Qty
C47, C41, C44	C0G, 10nF, +/-5%, 100V, 0603	3
C54	CAP, 33 UF, 20%, G CASE	1
C53	CAP, 10UF, 16V, TANTALUM	1
C11, C55, C5, C8	CAP, 100pF, +/-5%, 50V, 0402	4
R3	RES 15 OHM, +/-1%, 1/16W, 0402	1
C35, C29, C32	CAP, 1000PF, +/-5%, 100V, 0603	3
C49, C50, C51, C52	CAP, 1UF, 100V	4
R16	RES 0.0 OHM 1/16W 1206 SMD	1
-	PCB, RF-35, .010 THK, 3X4, 3-STAGE, QFN, CMPA1D1J001S	1
-	BASEPLATE 2.6"x1.7"x0.25" AL 3x4 QFN	1
-	2-56 SOC HD SCREW 3/16 SS	4
-	#2 SPLIT LOCKWASHER SS	4
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	1
J3	HEADER RT>PLZ .1CEN LK 5POS	1
W2, W3	WIRE, BLACK, 20 AWG	1
W1	WIRE, BLACK, 22 AWG	3
U1	CMPA1D1J001S	1

CMPA1D1J001S-AMP1 Evaluation Board Assembly Drawing



Note: W2 and W3 are connected on backside

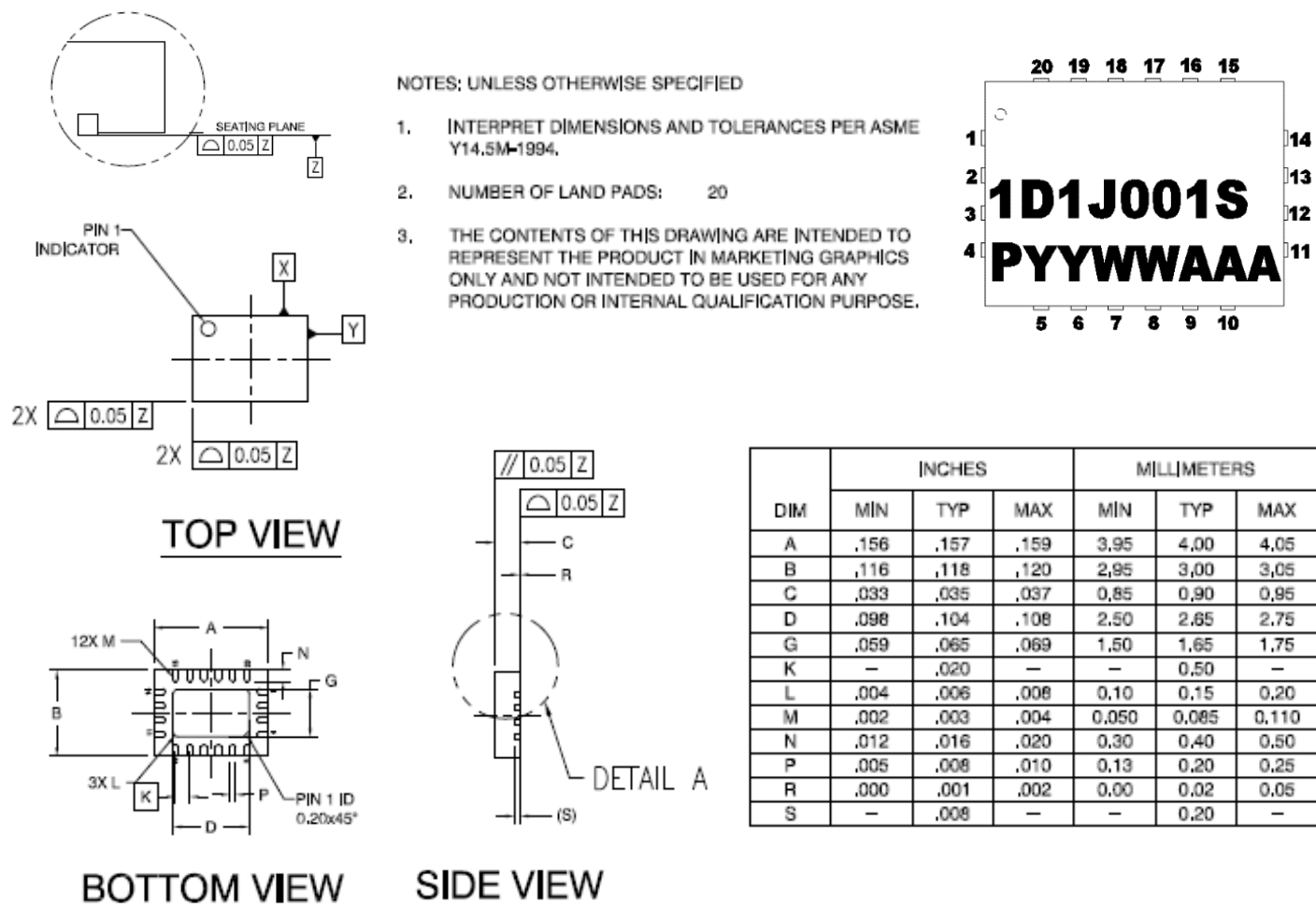
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_g)
3. Apply nominal drain voltage (V_d)
4. Adjust V_g to obtain desired quiescent drain current (I_{dq})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate ($V_g = -5V$)
3. Turn off drain voltage (V_d)
4. Turn off gate voltage (V_g)

Product Dimensions

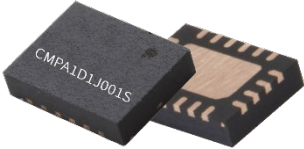
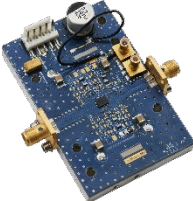


PIN	DESC	PIN	DESC
1	NC	11	RFGND
2	RFGND	12	RFGND
3	RFIN	13	RFGND
4	RFGND	14	NC
5	NC	15	VD3
6	NC	16	NC
7	NC	17	NC
8	VD1,VD2	18	VG
9	NC	19	NC
10	NC	20	NC

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA1D1J001S	12.7 – 18 GHz, 1W GaN MMIC		
CMPA1D1J001S-AMP1	Evaluation Board w/ PA	1 Each	

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