

MOSFET – N-Channel, POWERTRENCH[®], Shielded Gate

100 V, 16.5 A, 56 mΩ

FDMS8622, FDMS8622-NC

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWETRENCH process that incorporates Shielded Gate technology. This process has been optimized for $R_{DS(on)}$, switching performance and ruggedness.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 56 mΩ at V_{GS} = 10 V, I_D = 4.8 A
- Max $R_{DS(on)}$ = 88 mΩ at V_{GS} = 6 V, I_D = 3.9 A
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

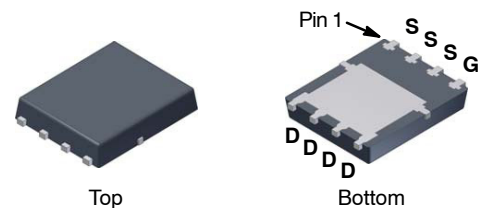
- POE Protection Switch
- DC-DC Switch

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous $T_C = 25\text{ °C}$ – Continuous $T_A = 25\text{ °C}$ (Note 1a) – Pulsed	16.5 4.8 30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	12	mJ
P_D	Power Dissipation: $T_C = 25\text{ °C}$ $T_A = 25\text{ °C}$ (Note 1a)	31 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

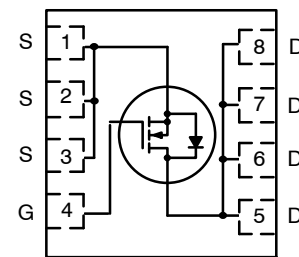
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	56 mΩ @ 10 V	16.5 A
	88 mΩ @ 6 V	

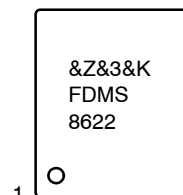


PQFN8 5 × 6, 1.27P
(Power 56)
CASE 483AE

ELECTRICAL CONNECTION



MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = 3-Digit Date Code
 (Year and Week)
 &K = 2-Digit Lot Run Code
 FDMS8622 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMS8622	PQFN8	3000 / Tape & Reel
FDMS8622-NC		

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^{\circ}\text{C}$	–	69	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^{\circ}\text{C}$	–	–8	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.8\text{ A}$	–	45	56	m Ω
		$V_{GS} = 6\text{ V}$, $I_D = 3.9\text{ A}$	–	62	88	
		$V_{GS} = 10\text{ V}$, $I_D = 4.8\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	–	78	97	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 4.8\text{ A}$	–	9	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	–	301	400	pF
C_{oss}	Output Capacitance		–	70	95	pF
C_{rss}	Reverse Transfer Capacitance		–	3.6	5	pF
R_g	Gate Resistance		–	1.0	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 4.8\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	–	5.7	11	ns
t_r	Rise Time		–	1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	10.2	18	ns
t_f	Fall Time		–	2.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$, $V_{DD} = 50\text{ V}$, $I_D = 4.8\text{ A}$	–	5	7	nC
		$V_{GS} = 0\text{ V to }5\text{ V}$, $V_{DD} = 50\text{ V}$, $I_D = 4.8\text{ A}$	–	2.8	4	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 50\text{ V}$, $I_D = 4.8\text{ A}$	–	1.4	2.8	nC
Q_{gd}	Gate to Drain “Miller” Charge	$V_{DD} = 50\text{ V}$, $I_D = 4.8\text{ A}$	–	1.3	2.6	nC

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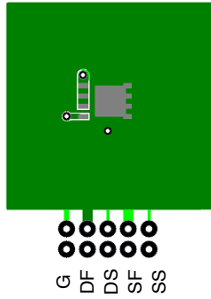
ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 4.8\text{ A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = 1.9\text{ A}$ (Note 2)	–	0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 4.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	–	38	60	ns
Q_{rr}	Reverse Recovery Charge		–	30	48	nC

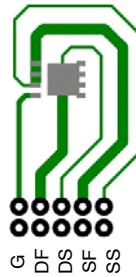
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Starting $T_J = 25\text{ }^{\circ}\text{C}$; N-ch: $L = 0.1\text{ mH}$, $I_{AS} = 16\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$.

TYPICAL CHARACTERISTICS

($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

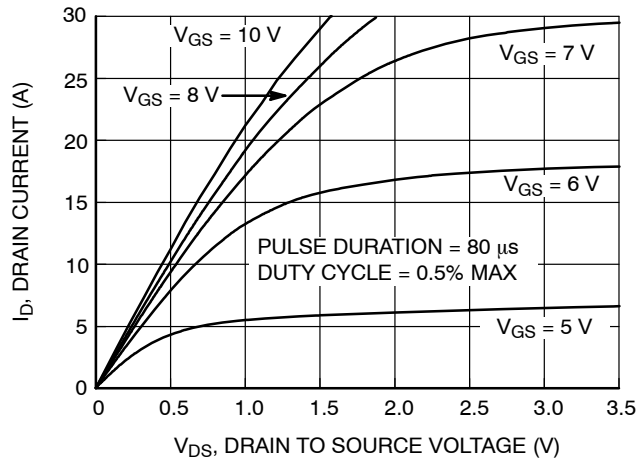


Figure 1. On Region Characteristics

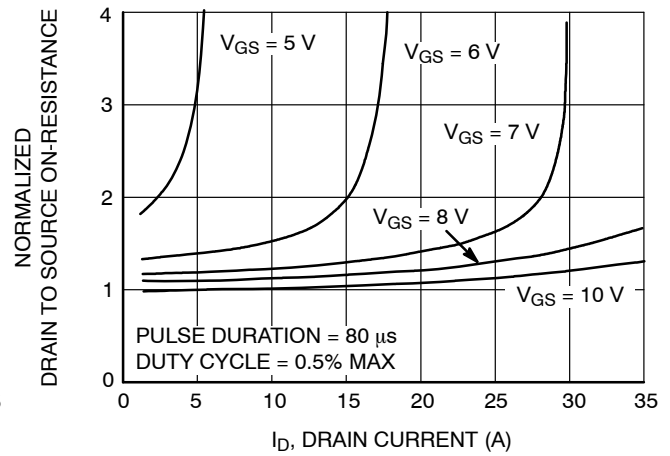


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

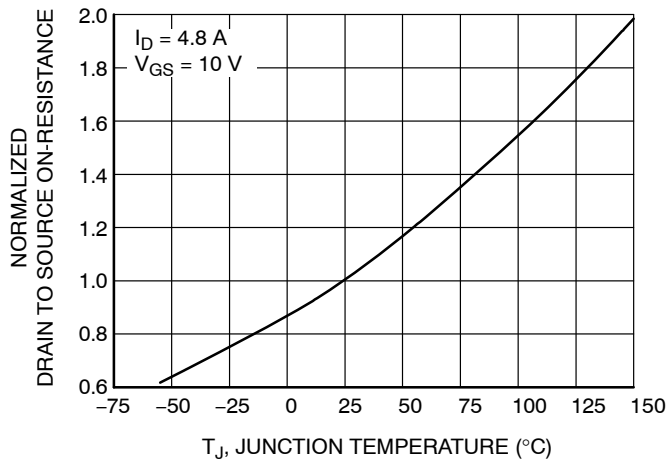


Figure 3. Normalized On-Resistance vs. Junction Temperature

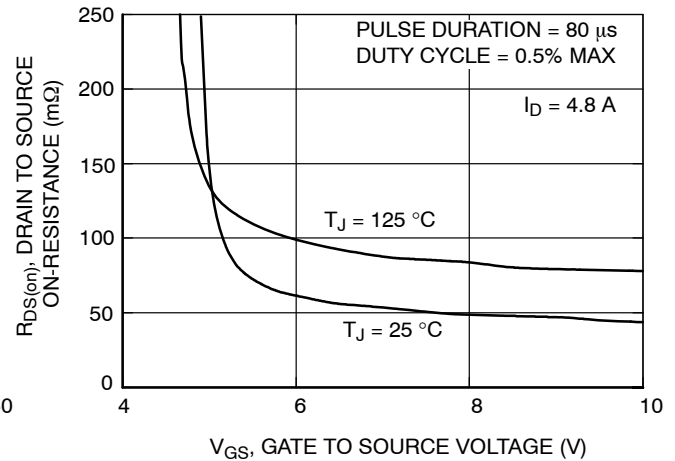


Figure 4. On-Resistance vs. Gate to Source Voltage

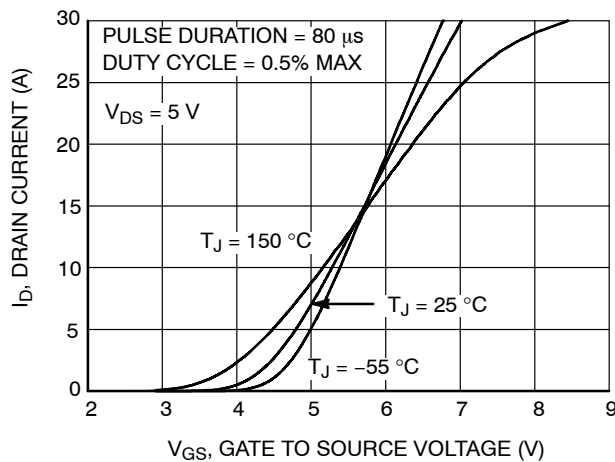


Figure 5. Transfer Characteristics

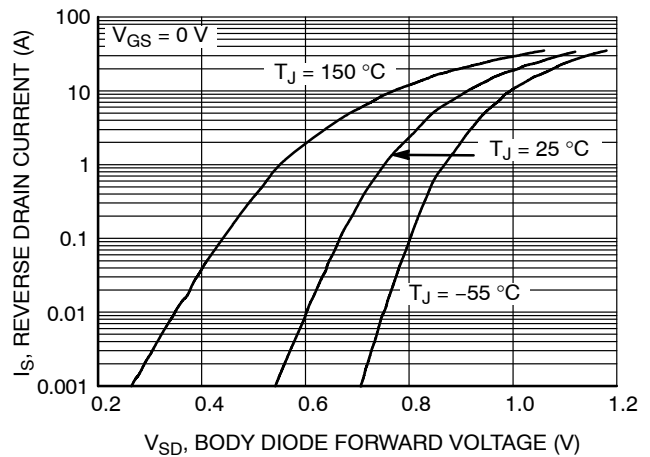


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

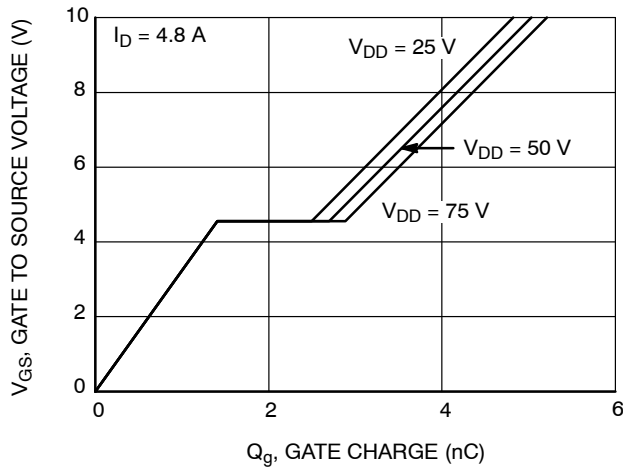


Figure 7. Gate Charge Characteristics

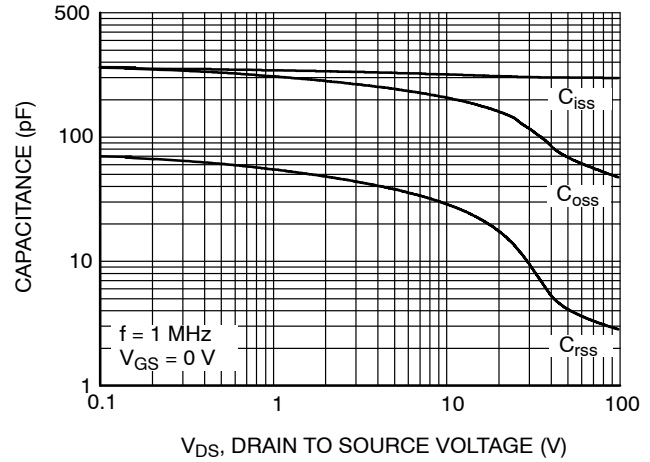


Figure 8. Capacitance vs. Drain to Source Voltage

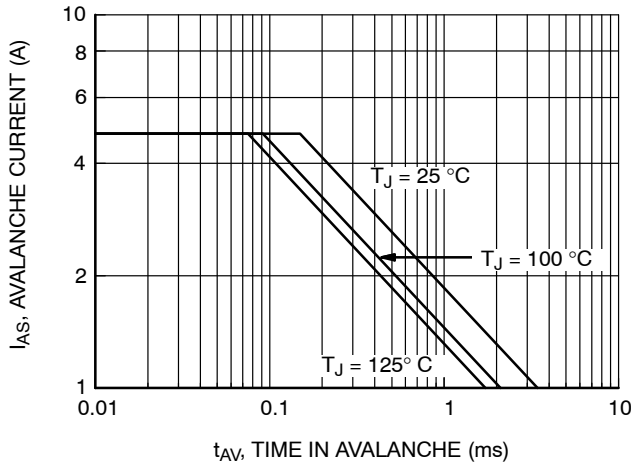


Figure 9. Unclamped Inductive Switching Capability

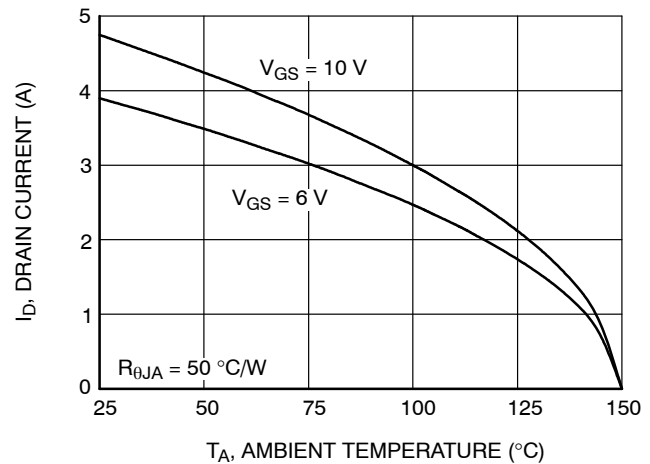


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

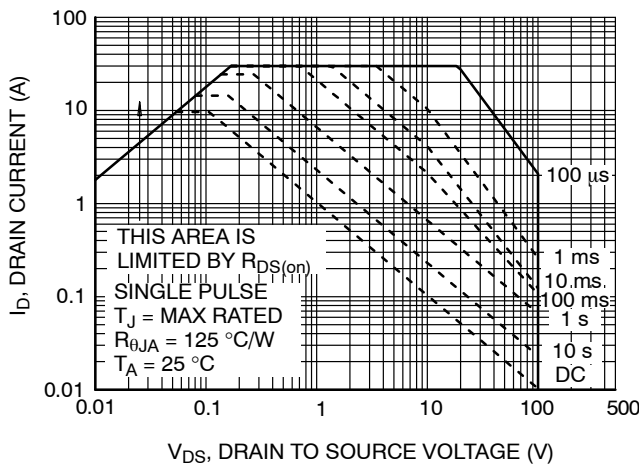


Figure 11. Forward Bias Safe Operating Area

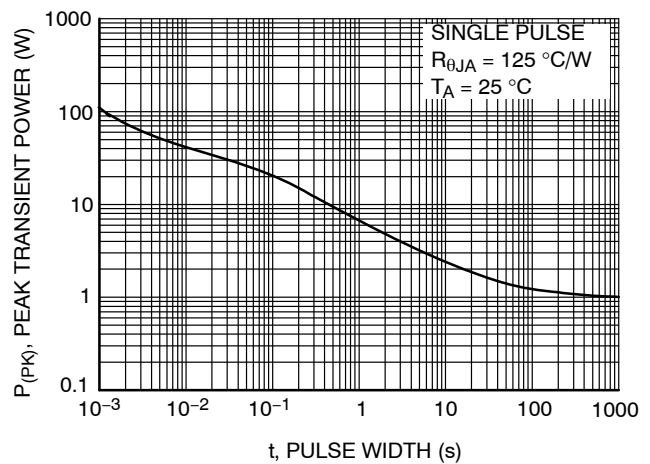


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

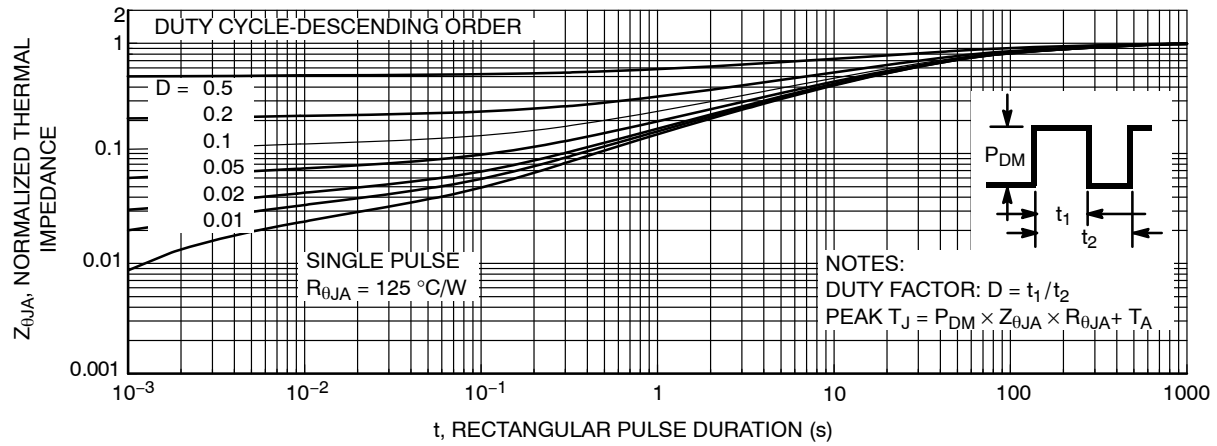


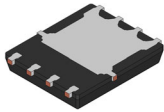
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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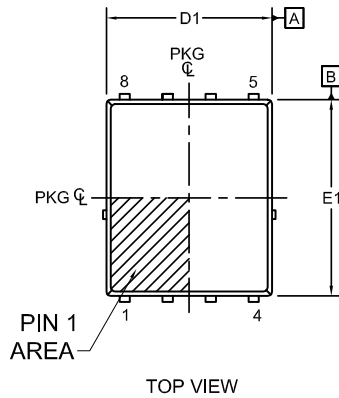
REVISION HISTORY

Revision	Description of Changes	Date
3	Document converted to onsemi format. Added new OPN FDMS8622-NC.	4/22/2026

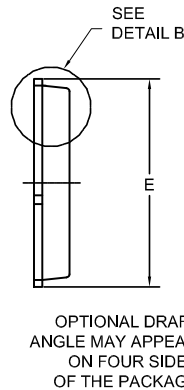
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

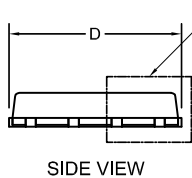


TOP VIEW

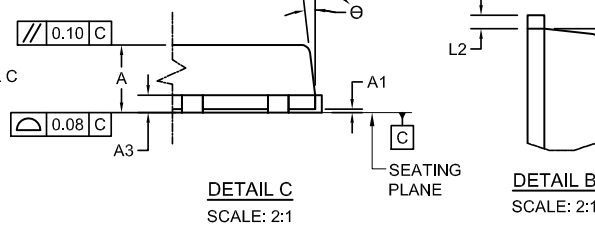
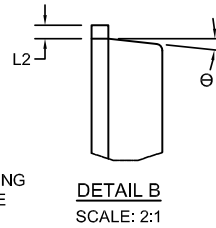
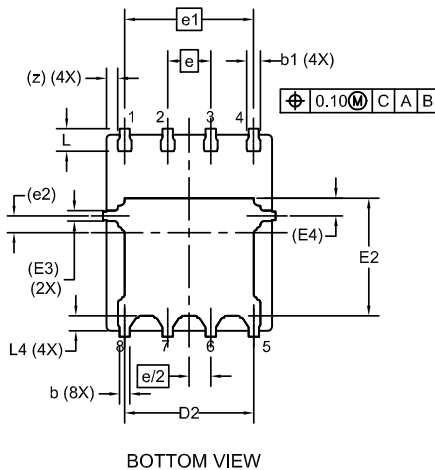

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

NOTES:

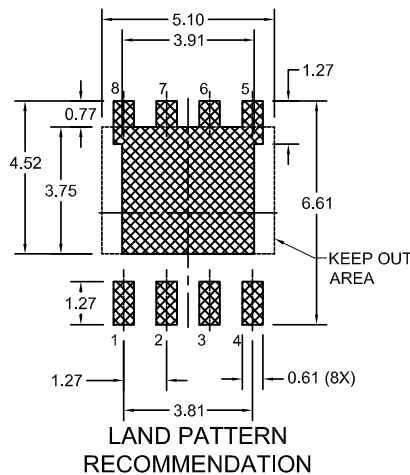
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



SIDE VIEW


DETAIL C
SCALE: 2:1

DETAIL B
SCALE: 2:1


BOTTOM VIEW


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING
DETAILS, PLEASE DOWNLOAD THE ON
SEMICONDUCTOR SOLDERING AND
MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

DOCUMENT NUMBER: 98AON13655G

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DESCRIPTION: PQFN8 5X6, 1.27P

PAGE 1 OF 1

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