Datasheet

80-mW Coupling Capacitorless Stereo Headphone Amplifiers

BD88400FJ

General Description

BD88400FJ is an output coupling capacitorless headphone amplifier. This IC has a built-in regulated negative voltage generator type that generates the direct regulated negative voltage from the supply voltage. It is possible to drive headphones in a ground standard with both voltage of the positive voltage (+2.4V) and the negative voltage (-2.4V). Therefore a large capacitance output coupling capacitor becomes needless and can reduce cost, board area and height of the part.
In addition, there is no signal degradation at the low range caused by the output coupling capacitor and output load impedance, thus a rich low tone can be outputted.

Package

W(Typ) x D(Typ) x H(Max)



SOP-J14
8.65mm x 6.00mm x 1.65mm

Features

- No Bulky DC-Blocking Capacitors Required
- No Degradation of Low-Frequency Response Due to Output Capacitors
- Ground-Referenced Outputs
- Gain setting: Variable Gain with External Resistors
- Low THD+N
- Low Supply Current
- Integrated Negative Power Supply
- Integrated Short-Circuit and Thermal-Overload Protection

Applications

Home Audio, TVs, Portable Audio Players, PCs, Digital Cameras, Electronic Dictionaries, Voice Recorders, Bluetooth Headsets, etc.

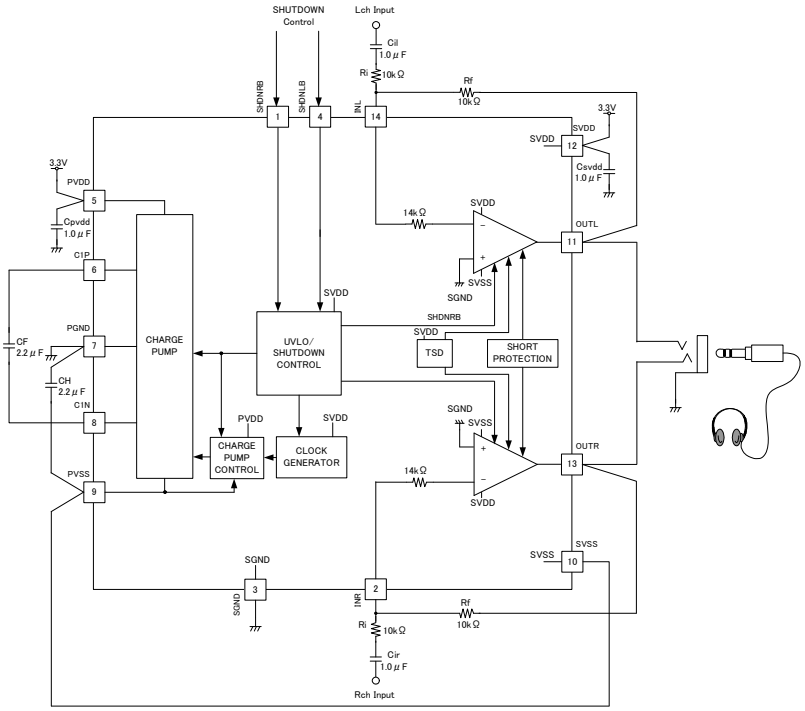
Key Specifications and Lineup

Supply Voltage [V]	+2.4 to +5.5
Supply Current [mA]	2.0 (No Signal)
Gain [V/V]	Variable Gain with External Resistor
Maximum Output Power [mW]	80 (V_{DD}=3.3V,R_L=16Ω, THD+N≤1%,f=1kHz)
THD+N [%]	0.006 (V_{DD}=3.3V,R_L=16Ω,Po=10mW,f=1kHz)
Noise Voltage [μVrms]	10
PSRR [dB]	-80 (f=217Hz)

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Typical Application Circuit



Part	Function	Value	Remarks
CF	Flying Capacitor	2.2μF	Temp. Characteristic : Class-B
CH	Hold Capacitor	2.2μF	Temp. Characteristic : Class-B
CPVDD	Bypass Capacitor	1.0μF	Temp. Characteristic : Class-B
CSVDD	Bypass Capacitor	1.0μF	Temp. Characteristic : Class-B
Cil	Coupling Capacitor	1.0μF	Temp. Characteristic : Class-B
Cir	Coupling Capacitor	1.0μF	Temp. Characteristic : Class-B
Ri	Input Resistor	10kΩ	MCR006YZPJ103 (ROHM)
Rf	Feedback Resistor	10kΩ	MCR006YZPJ103 (ROHM)

In BD88400FJ, the Pass Gain follows formula (4). The Pass Gain and the resistor Rf is limited by table.1.

$$\text{Gain} = \frac{R_f}{R_i} \quad (4)$$

Table 1. Pass Gain and Resistor Limit

Item	Min	Typ	Max	Unit
Pass Gain	0.5	1.0	2.0	V/V
Rf	1.0	10	-	kΩ
Ri	-	10	-	kΩ

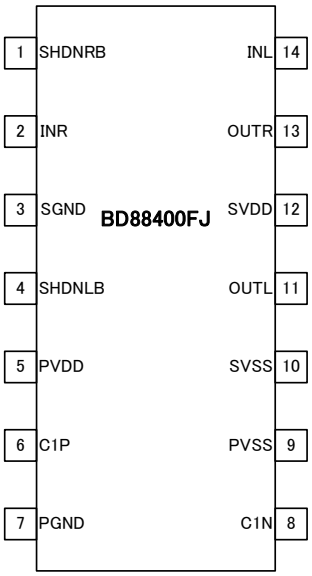
Ri is not limited. But, if this resistor Ri is very small, the signal degradation happens at the low frequency (Refer to formula (2)).

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Pin Configuration

(Top View)



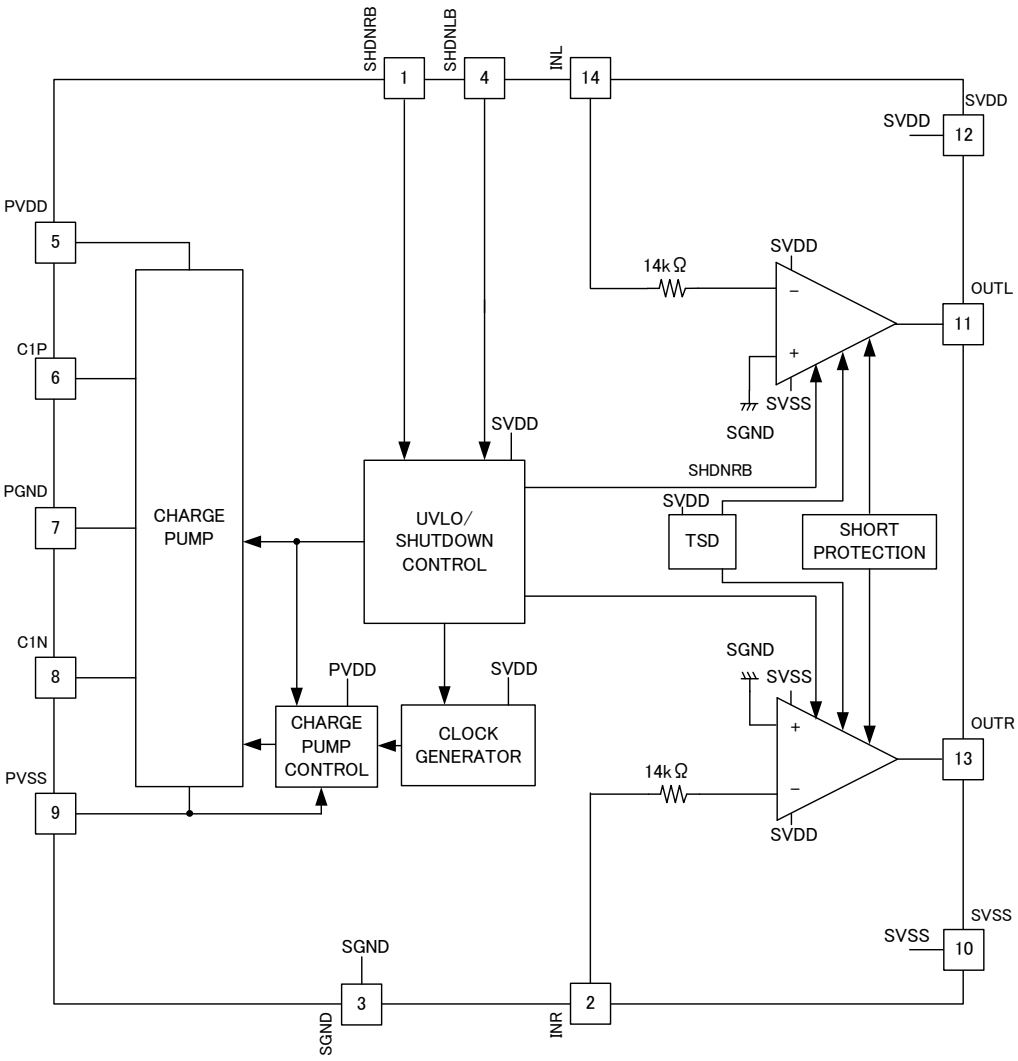
Pin Descriptions

No.	Pin Name	Function	Symbol
1	SHDNRB	Headphone Amplifier (Rch) Shutdown Control (H:active, L:shutdown)	E
2	INR	Headphone Amplifier (Rch) input	C
3	SGND	Ground for Headphone Amplifier	-
4	SHDNLB	Headphone Amplifier (Lch) Shutdown Control (H:active, L:shutdown)	E
5	PVDD	Positive Power Supply for Charge Pump	-
6	C1P	Flying Capacitor Positive	A
7	PGND	Ground for Charge Pump	-
8	C1N	Flying Capacitor Negative	B
9	PVSS	Negative Supply Voltage output	F
10	SVSS	Negative Supply Voltage for Signal	-
11	OUTL	Headphone Amplifier (Lch) output	D
12	SVDD	Ground for Headphone Amplifier	-
13	OUTR	Headphone Amplifier (Rch) output	D
14	INL	Headphone Amplifier (Lch) input	C

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
SGND to PGND Voltage	V_{GG}	0.0	V
SVDD to PVDD Voltage	V_{DD}	-0.3 to +0.3	V
SVSS to PVSS Voltage	V_{SS}	0.0	V
SGND or PGND to SVDD, PVDD Voltage (Note 1)	V_{DG}	-0.3 to +6.0	V
SVSS, PVSS to SGND Or PGND Voltage	V_{SG}	-3.5 to +0.3	V
SGND to IN_- Voltage	V_{IN}	(SVSS-0.3) to 2.8	V
SGND to OUT_- Voltage	V_{OUT}	(SVSS-0.3) to 2.8	V
PGND to C1P- Voltage	V_{C1P}	(PGND-0.3) to (PVDD+0.3)	V
PGND to C1N- Voltage	V_{C1N}	(PVSS-0.3) to (PGND+0.3)	V
SGND to SHDN_B- Voltage	V_{SH}	(SGND-0.3) to (SVDD+0.3)	V
Input Current	I_{IN}	-10 to +10	mA
Power Dissipation (Note 2)	Pd	1.02	W
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Pd must not be exceeded.
(Note 2) When mounted on 70mm×70mm×1.6mm FR4, 1-layer glass epoxy board. Derate by 8.19mW/°C when operating above Ta=25°C
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage Range	V_{SVDD},V_{PVDD}	2.4	-	5.5	V
Operating Temperature Range	T_{OPR}	-40	-	+85	°C

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Electrical Characteristics

Unless otherwise specified, T Ta=25°C, SVDD=PVDD=3.3V, SGND=PGND=0V, SHDNLB=SHDNRB=SVDD, CF=CH=2.2µF, RL=No load, Ri=Rf=10kΩ

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current						
Shutdown Supply Current	I_{ST}	-	0.1	2	µA	SHDNLB=SHDNRB=L
Quiescent Supply Current	I_{DD1}	-	1.3	-	mA	(SHDNLB,SHDNRB)=(H,L) or (L,H), No Signal
	I_{DD2}	-	2.0	7.4	mA	SHDNLB=SHDNRB=H, No Signal
SHDN_B Terminal						
H Level Input Voltage	V_{IH}	1.95	-	-	V	
L Level Input Voltage	V_{IL}	-	-	0.70	V	
Input Leak Current	I_{LEAK}	-	-	±1	µA	
Headphone Amplifier						
Shutdown to Full Operation	t_{SON}	-	80	-	µs	SHDNLB=SHDNRB=L to H
Offset Voltage	V_{IS}	-	±0.5	±6.0	mV	
Maximum Output Power	P_{OUT}	30	60	-	mW	R_L=32Ω, THD+N≤-40dB, f=1kHz, 20kHz LPF, for Single Channel
		40	80	-	mW	R_L=16Ω, THD+N≤-40dB, f=1kHz, 20kHz LPF, for Single Channel
Total Harmonic Distortion + Noise	THD+N	-	0.008	0.056	%	R_L=32Ω, P_{OUT}=10mW, f=1 kHz, 20kHz LPF
		-	0.006	0.100	%	R_L=16Ω, P_{OUT}=10mW, f= kHz, 20kHz LPF
Gain	A_V	-	-1.00	-	V/V	Gain Is variable by the external resistor of Ri and Rf.
Gain Match	ΔA_V	-	1	-	%	
Noise	V_N	-	10	-	µVrms	20kHz LPF + JIS-A
Slew Rate	SR	-	0.15	-	V/µs	
Maximum Capacitive Load	CL	-	200	-	pF	
Crosstalk	CT	-	-90	-	dB	R_L=32Ω, f=1kHz, V_{OUT}=200mV_{P-P}, 1kHz BPF
Power Supply Rejection Ratio	PSRR	-	-80	-	dB	f=217Hz, 100mV_{P-P}-ripple, 217Hz BPF
Charge-Pump Oscillator Frequency	f_{OSC}	200	300	430	kHz	
Thermal-Shutdown Threshold	TSD	-	145	-	°C	
Thermal-Shutdown Hysteresis	T_{HYS}	-	5	-	°C	

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Typical Performance Curves

General Items

Unless otherwise specified, Ta=25°C, SGND=PGND=0V, SHDNLB=SHDNRB=SVDD, CF=CH=2.2µF,
Input coupling capacitor=1µF, R_L=No Load
(Note) In BD88400FJ the input resistor (Ri)=10kΩ, feedback resistor(Rf)=10kΩ.

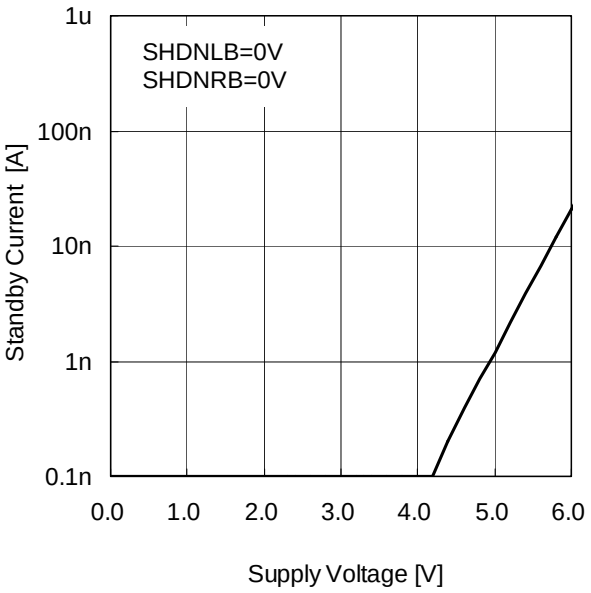


Figure 1. Standby Current vs Supply Voltage

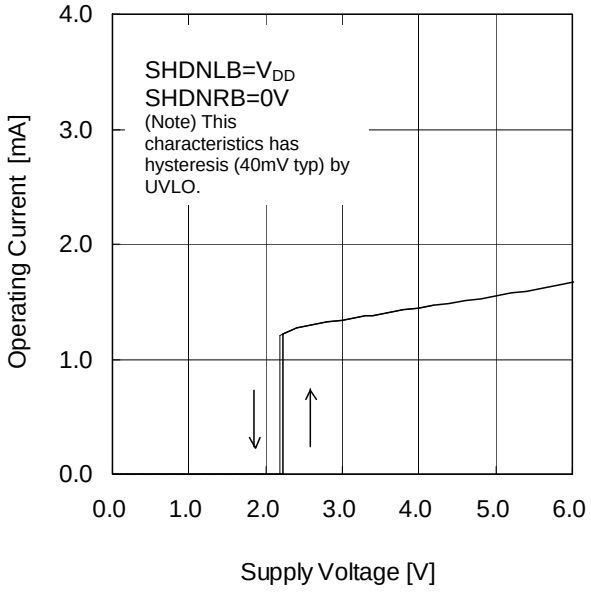


Figure 2. Monaural Operating Current vs Supply Voltage

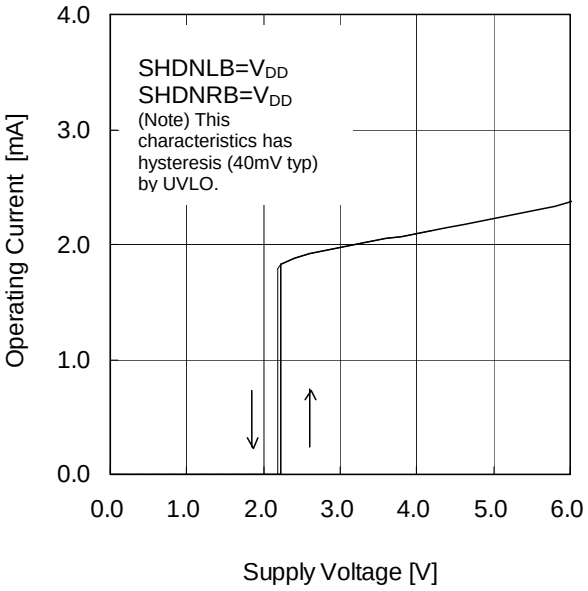


Figure 3. Stereo Operating Current vs Supply Voltage

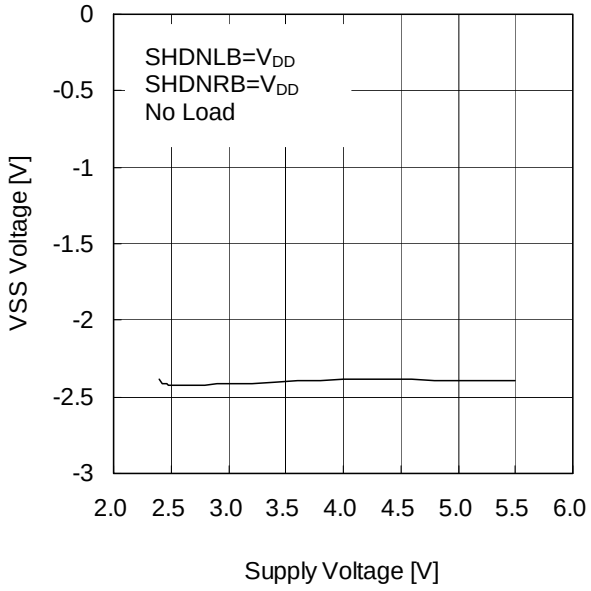


Figure 4. Negative Voltage vs Supply Voltage

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Typical Performance Curves – continued

General Items

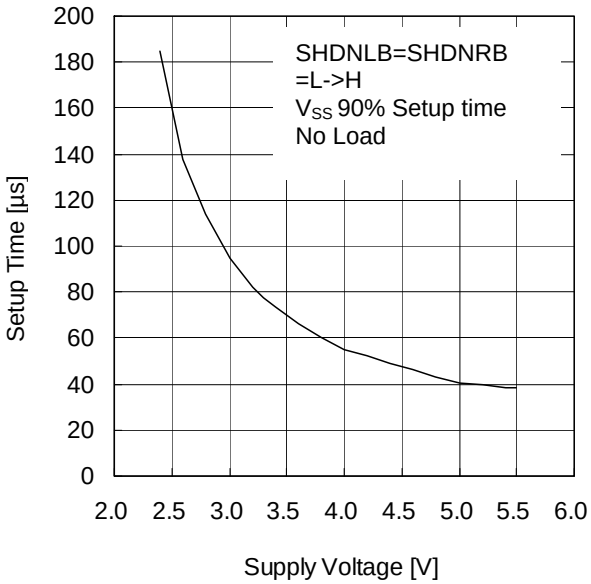


Figure 5. Setup Time vs Supply Voltage

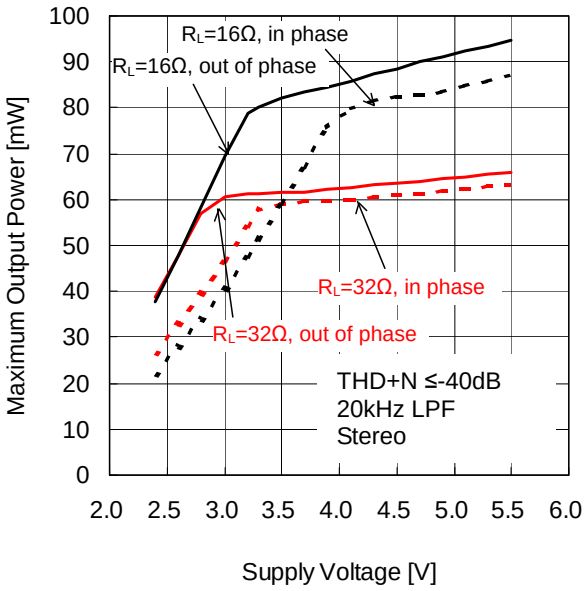


Figure 6. Maximum Output Power vs Supply Voltage

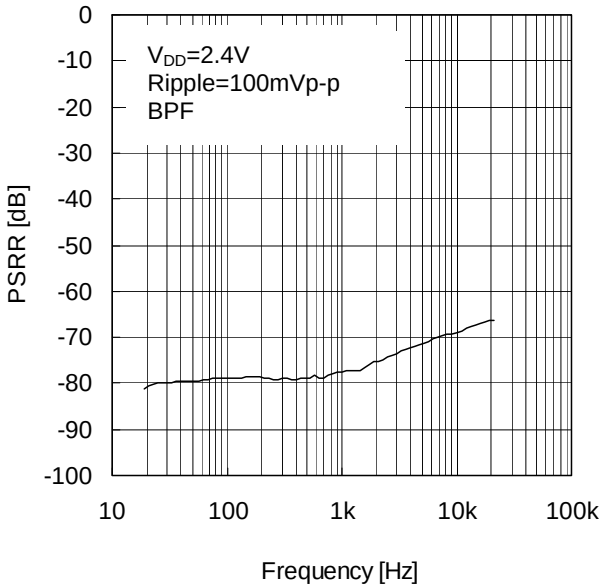


Figure 7. PSRR vs Frequency
(V_{DD}=2.4V)

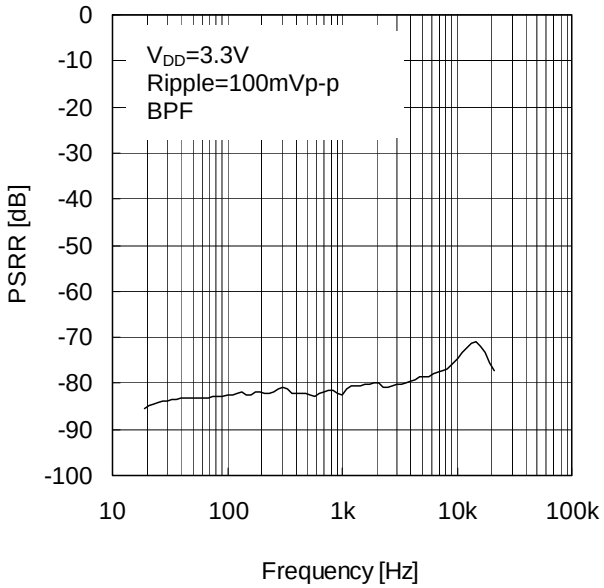


Figure 8. PSRR vs Frequency
(V_{DD}=3.3V)

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Typical Performance Curves – continued

General Items

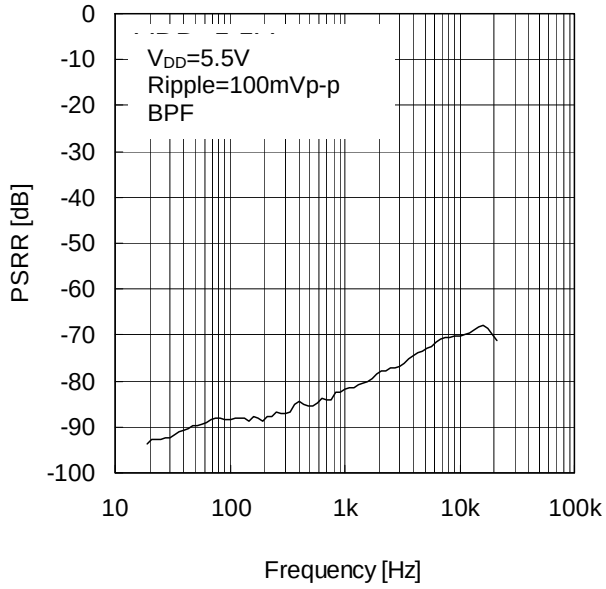


Figure 9. PSRR vs Frequency
(V_{DD}=5.5V)

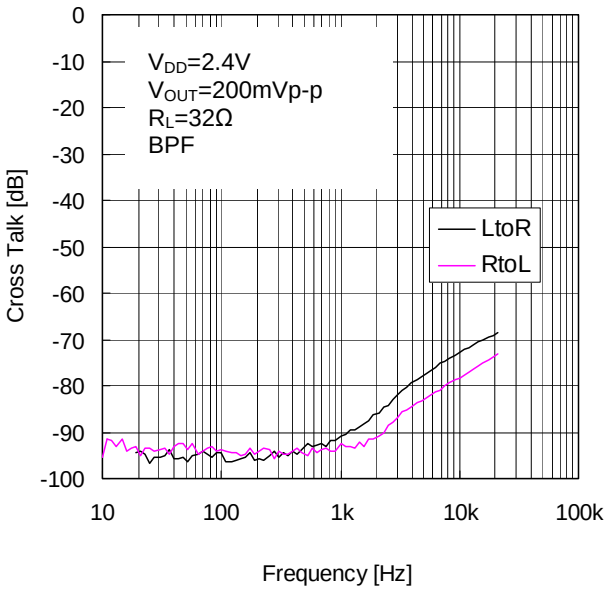


Figure 10. Crosstalk vs Frequency
(V_{DD}=2.4V)

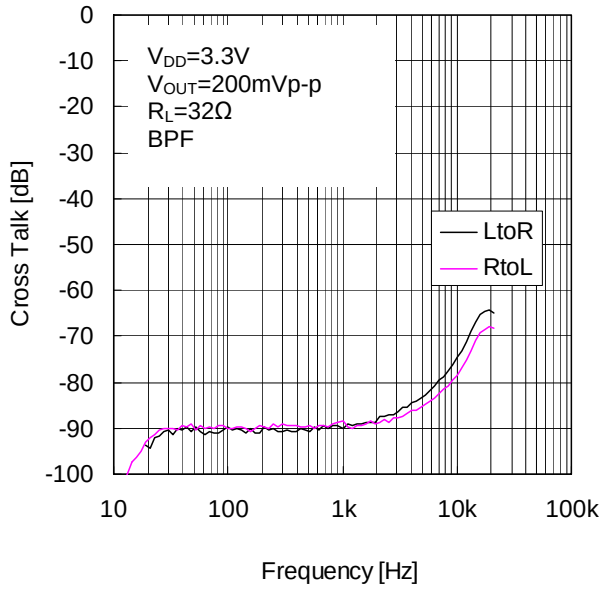


Figure 11. Crosstalk vs Frequency
(V_{DD}=3.3V)

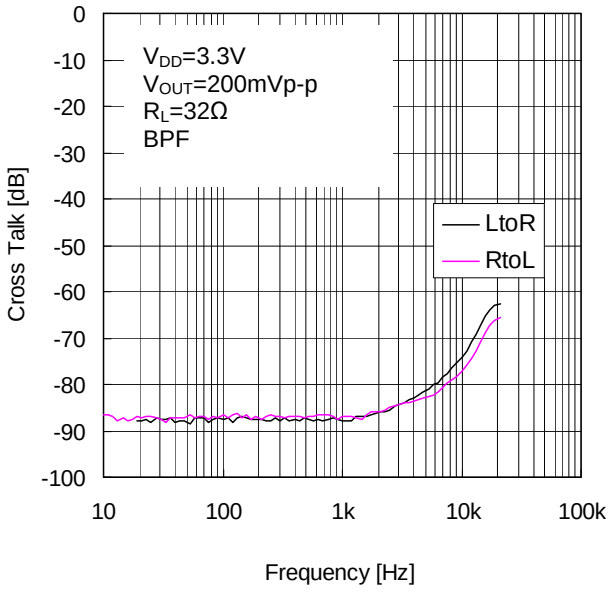


Figure 12.Crosstalk vs Frequency
(V_{DD}=5.5V)

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Typical Performance Curves – continued

BD88400FJ

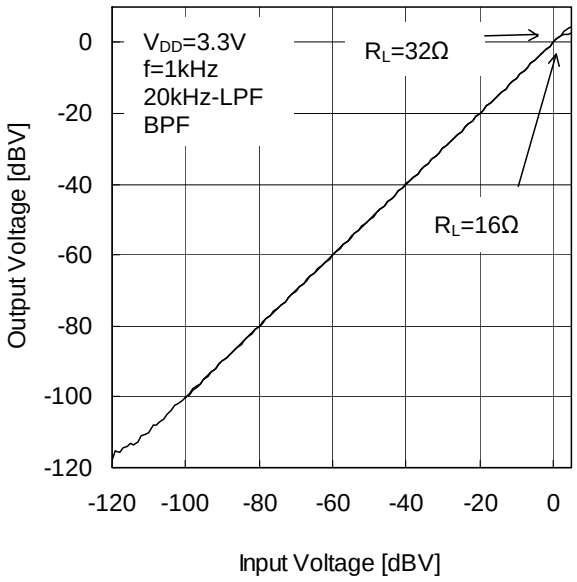


Figure 13. Output Voltage vs Input Voltage
(V_{DD}=3.3V)

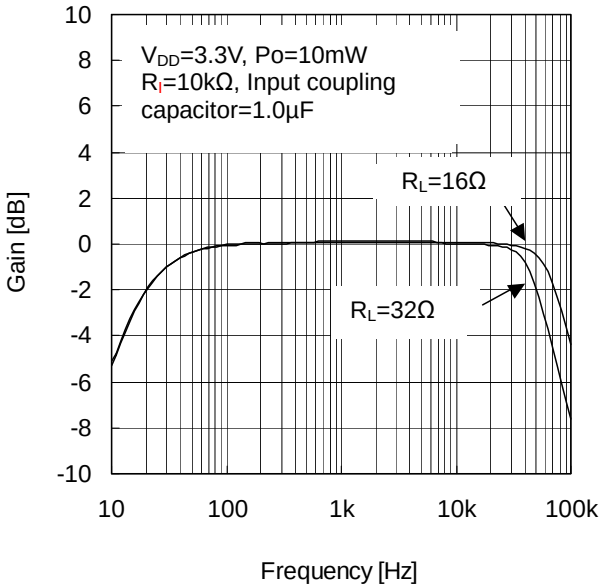


Figure 14. Gain vs Frequency
(V_{DD}=3.3V)

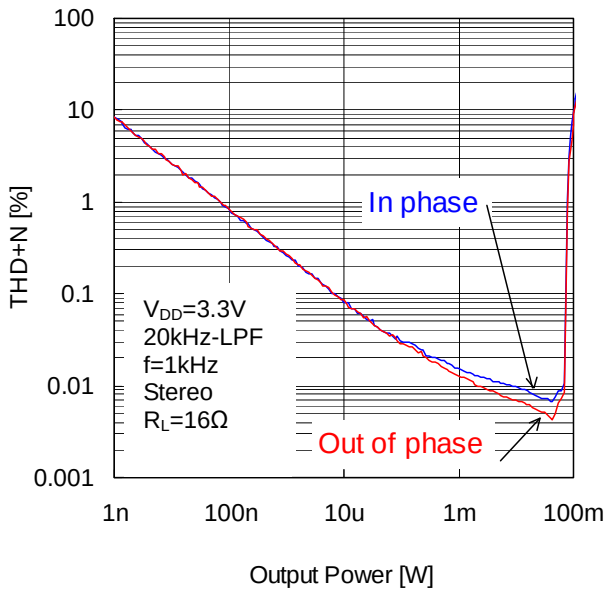


Figure 15. THD+N vs Output Power
(V_{DD}=3.3V, R_L=16Ω)

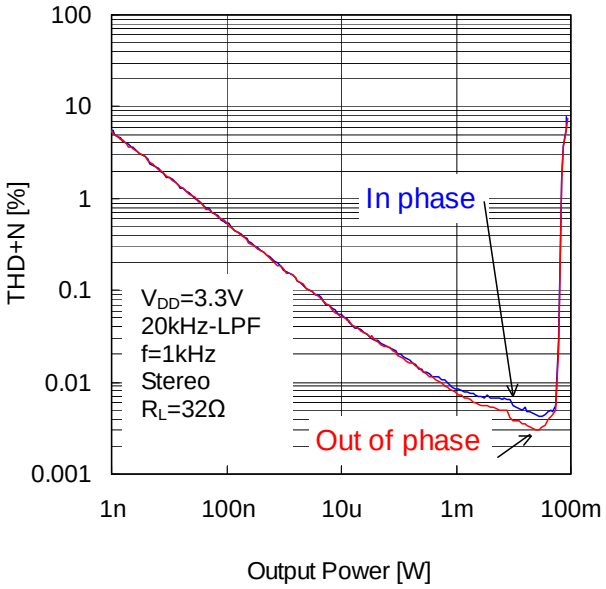


Figure 16. THD+N vs Output Power
(V_{DD}=3.3V, R_L=32Ω)

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Typical Performance Curves – continued

BD88400FJ

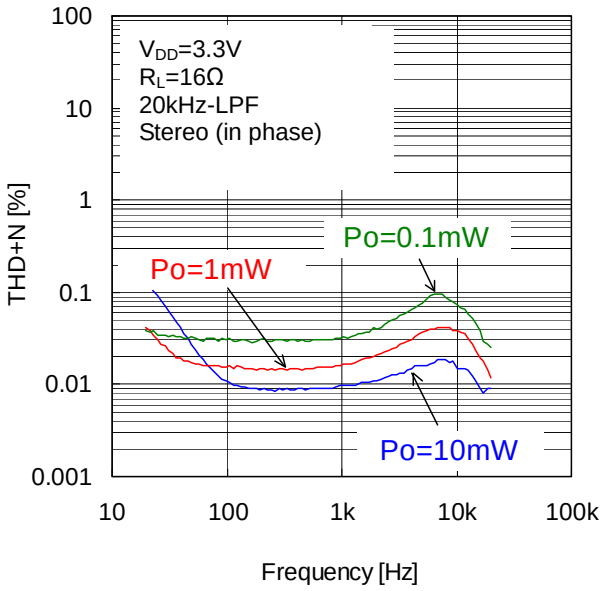


Figure 17. THD+N vs Frequency
(V_{DD}=3.3V, R_L=16Ω)

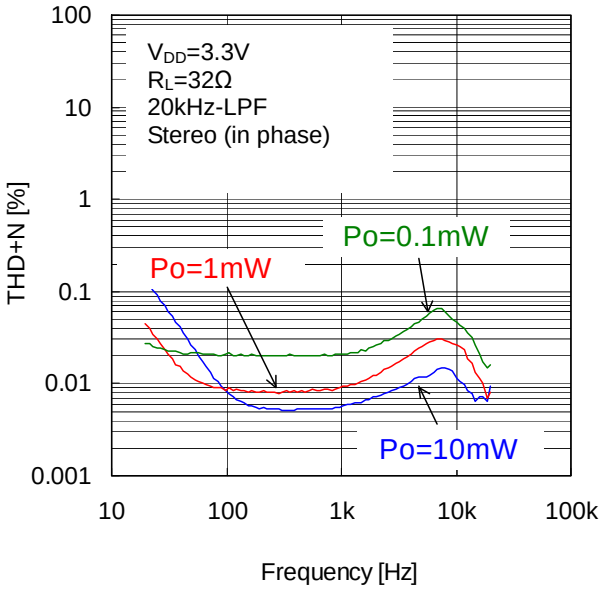


Figure 18. THD+N vs Frequency
(V_{DD}=3.3V, R_L=32Ω)

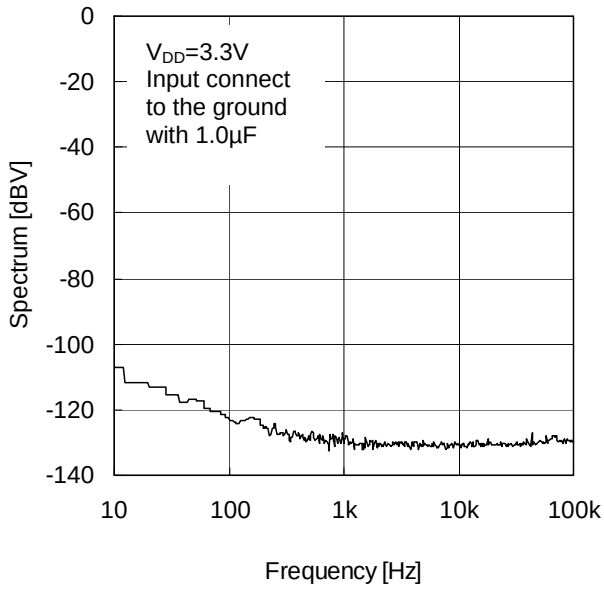


Figure 19. Noise Spectrum vs Frequency
(V_{DD}=3.3V)

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Timing Chart

(Usually Operation)

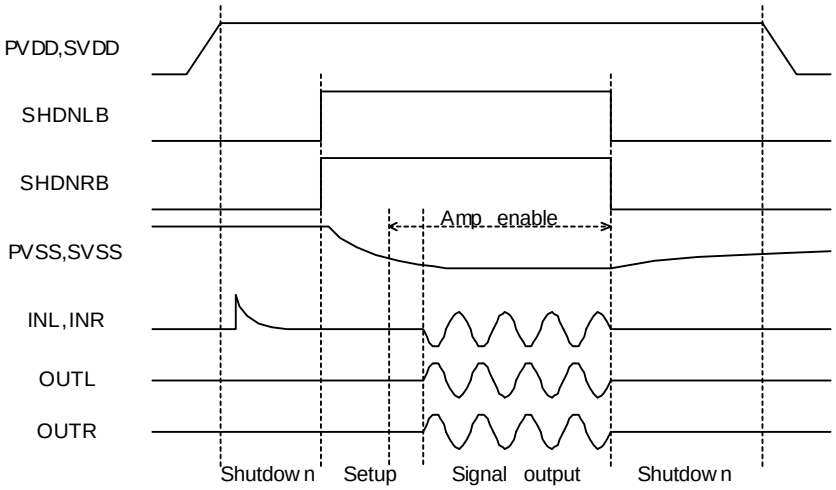


Figure 20. Usually Operation

(UVLO Operation)

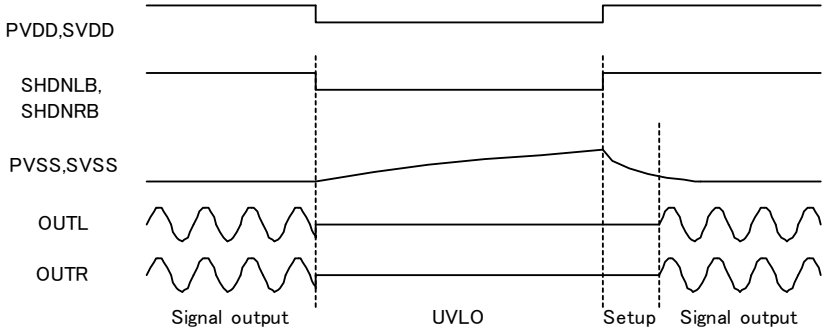


Figure 21. UVLO Operation

(TSD Operation)

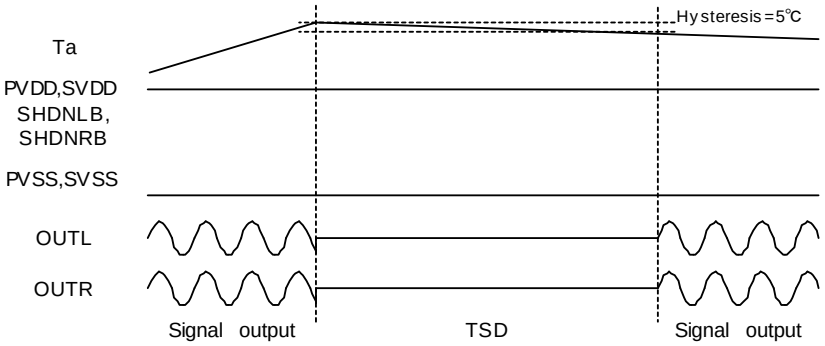


Figure 22. TSD Operation

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Application Information

1. Functional Descriptions

Figure 23 shows the conventional headphone amplifier circuit. In this circuit, the signal is outputted using the middle point bias circuit based on the middle point bias. Therefore, the output coupling capacitor that removes the DC voltage difference and does the AC coupling is necessary. This coupling capacitor and the impedance of the headphone compose the high-pass filter. Therefore, the signal degradation in the low frequency region is experienced. The output coupling capacitor should be of large capacitance because the cutoff frequency of this high-pass filter follows formula (1).

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (1)$$

(Note) Cc is the coupling capacitor, and R_L is the impedance of the headphone.

Moreover, POP noise by the middle point bias start-up is generated and the degradation of PSRR is experienced.

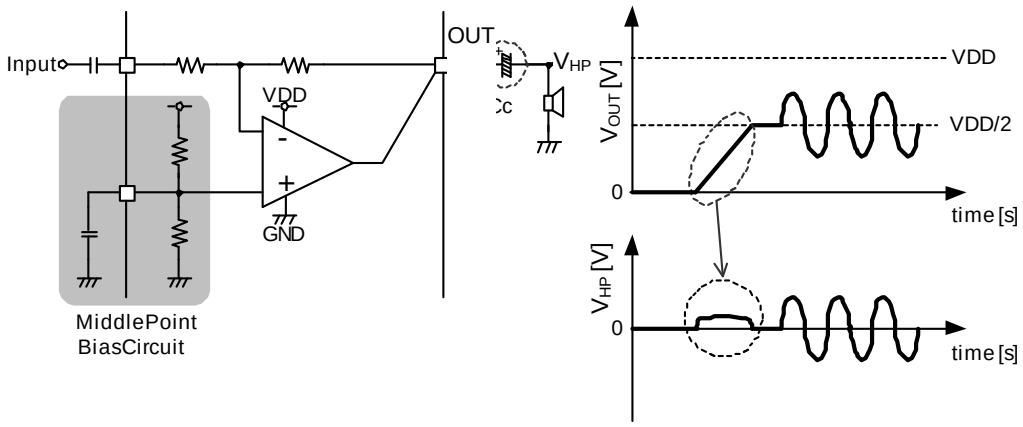


Figure 23. Conventional Headphone Amplifier Circuit

Figure 24 shows the BD88400FJ series circuit. In this circuit, the signal is outputted using a negative voltage based on the ground level. Therefore, the amplifier output can be connected directly to the headphone, making the output coupling capacitor unnecessary. In addition, the signal degradation in the low frequency region with the coupling capacitor is not generated, thus a deep bass is achieved.
Moreover, POP noise is not controlled by the middle point bias start-up. Thus, the degradation of PSRR doesn't occur since it is based on the ground.

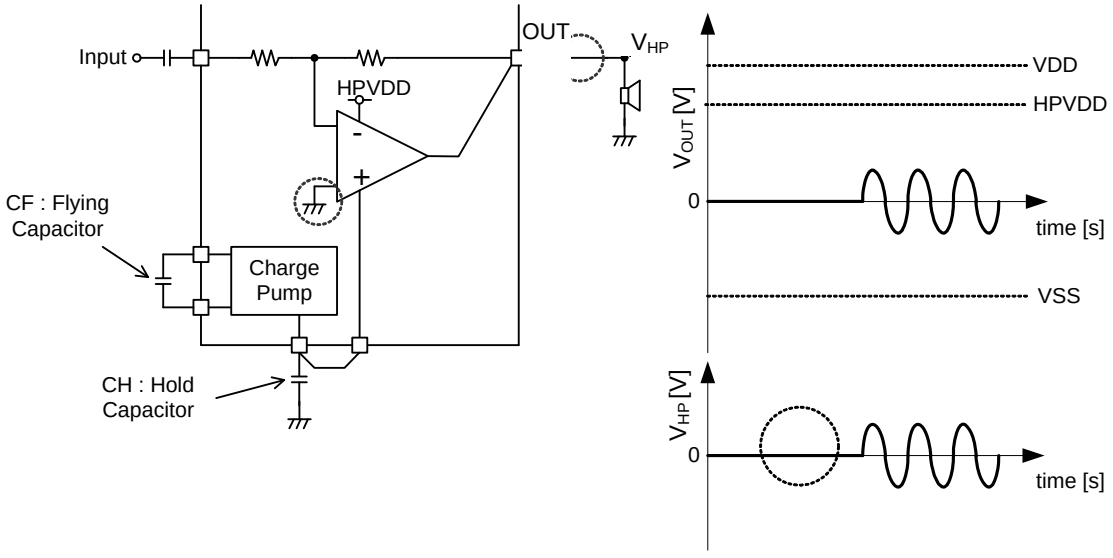


Figure 24.BD88400FJ Series Circuit

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(1) CHARGE PUMP / CHARGE PUMP CONTROL

The negative power supply circuit is composed of the regulated charge-pump. This circuit outputs the regulated negative voltage (PVSS) directly from power-supply voltage (PVDD). Therefore, it doesn't depend on the power-supply voltage and a constant voltage is outputted (PVSS=-2.4$V_{@Typ}$, refer to Figure 4). Moreover, there is no power supply swinging caused by the output current of the headphone amplifier. Also, it doesn't influence the headphone amplifier characteristic.

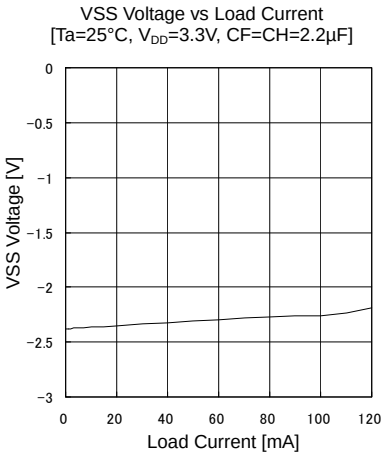


Figure 25. PVSS Load Current Regulation Characteristics (Reference Data)

(a) Power Control

The power control is a logical sum of SHDNLB and SHDNRB. The negative power supply circuit starts when H level is inputted to either SHDNLB or SHDNRB, and power down when SHDNLB=SHDNRB=L level.

Table.2 Charge Pump Control

SHDNLB	SHDNRB	Control
L	L	Power down
L	H	Power ON
H	L	Power ON
H	H	Power ON

(b) Operating Frequency

The operating frequency of the negative power supply charge pump is designed to minimize temperature and voltage dependency. Figure 26 shows the reference data (measurements). Please note the frequency interference in the application board.

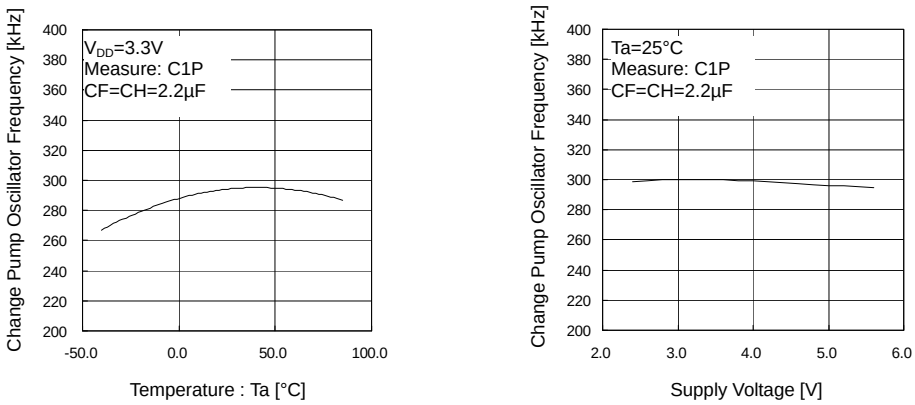


Figure 26. Temperature Characteristic and Voltage Characteristic of Operating Frequency (Reference Data)

(c) The Flying Capacitor and the Hold Capacitor

The flying capacitor (CF) and the hold capacitor (CH) greatly influence the characteristic of the charge pump. Therefore, please connect 2.2µF capacitor with an excellent temperature characteristic and voltage characteristic as near as possible to the IC.

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(2) HEADPHONE AMP

The headphone amplifier is driven by the internal positive voltage (+2.4V) and negative voltage (SVSS, -2.4V) based on ground (SGND). Therefore, the headphone can be connected without the output coupling capacitor. As a result, it brings improvement to low-frequency characteristic compared with the conventional coupling capacitor headphone type.

(a) Power Control

L channel and R channel of the headphone amplifier can be independently controlled by SHDNLB and SHDNRB logic. When the SVSS voltage is -1.1V$_{@Typ}$ or more, the headphone amplifier does not operate to protect from illegal operation. In addition, the over-current protection circuit is built in. The amplifier shutdowns when the over-current occurs because of the output short-circuit etc., thus IC is protected from being destroyed.

Table.3 Control of the headphone amplifier

SHDNLB	SHDNRB	L Channel	R Channel
L	L	Power down	Power down
L	H	Power down	Power ON
H	L	Power ON	Power down
H	H	Power ON	Power ON

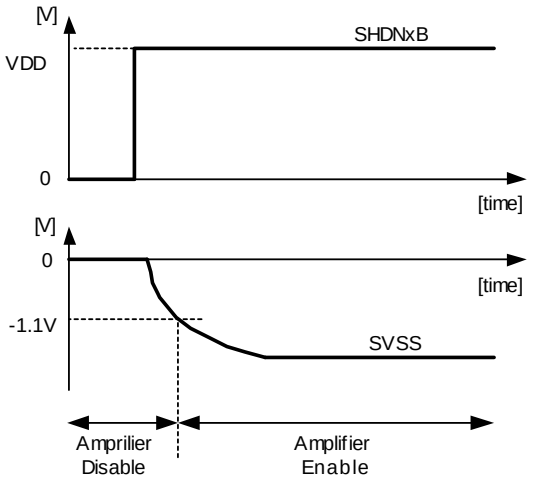


Figure 27. Area of Headphone Amplifier can Operate

SVSS does not have internal connection with PVSS. Please connect SVSS with PVSS on the application board.

(b) Input Coupling Capacitor

Input DC level of BD88400FJ is 0V (SGND). The input coupling capacitor is necessary for the connection with the signal source device. The signal degradation happens in the low frequency because of the high-pass filter composed by this input coupling capacitor and the input impedance of BD88400FJ.

The input impedance of BD88400FJ is external resistance Ri. The cutoff frequency of this high-pass filter follows formula (2).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \quad (2)$$

Where:

C_{IN} is the input coupling capacitor. R_{IN}=Ri

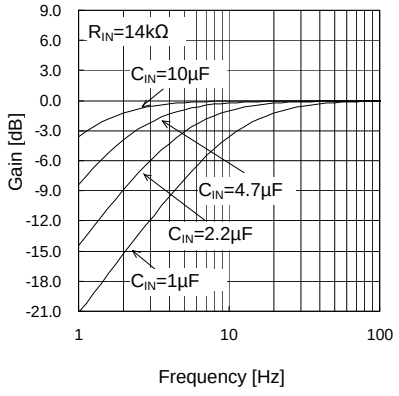
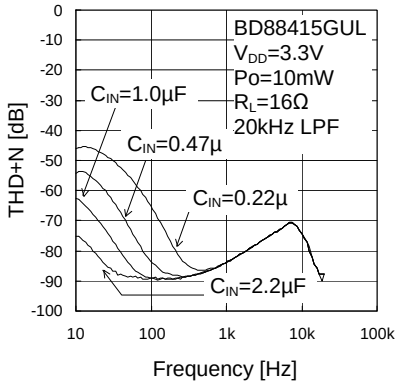


Figure 28. Input Coupling Capacitor Frequency Response (Reference Data)

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The degradation of THD+N happens because of the input coupling capacitor. Therefore, please consider these when selecting components.



(Note) Capacitor size: 1608

Figure 29. THD+N by the Input Coupling Capacitor (Reference Data)

(c) Terminal State during Power Down

The power control of the headphone amplifier changes the state of the terminal. When in shutdown, the input impedance of the input terminal becomes 7.1kΩ$_{@Typ}$ (In BD88400FJ, become RI + 7.1kΩ). The time constant can be reduced when the input coupling capacitor is charged.

The input voltage changes while charging up the input coupling capacitor. Therefore, do not operate the headphone amplifier while charging.

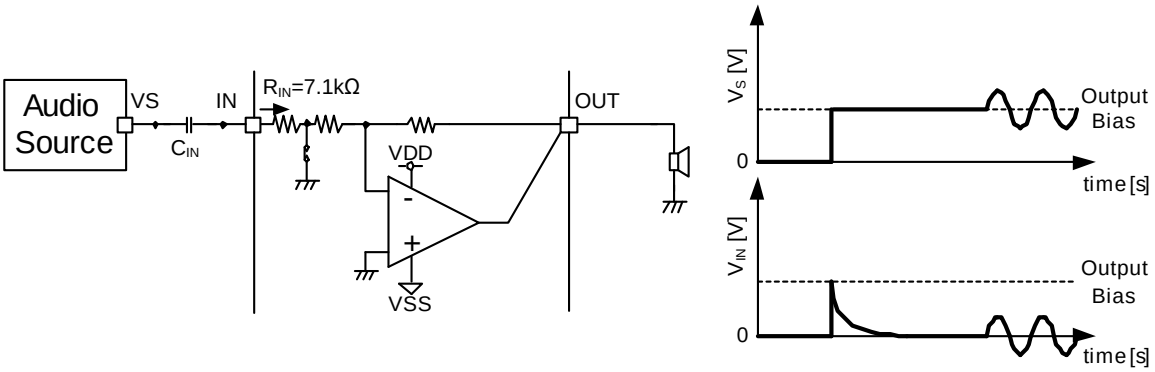


Figure 30. Input voltage transition with input coupling capacitor

Charge time constant follows formula (3) by using the input coupling capacitor and the input impedance. The calculation of the convergence value to wait time is indicated in Figure 31.

$$\tau = R_{IN}C_{IN} \qquad (3)$$

(Note) R_{IN}=7.1kΩ$_{@Typ}$ In BD88400FJ, R_{IN}=Ri+7.1kΩ

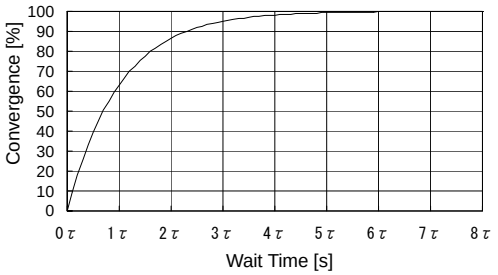


Figure 31. Convergence vs Wait Time (Reference)

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(3) UVLO / SHUTDOWN CONTROL
BD88400FJ has low voltage protection function (UVLO: Under Voltage Lock Out). This protects the IC from the illegal operation during a low power supply voltage.
The detection voltage is $2.13V_{@Typ}$, so it does not influence recommended operation voltage of 2.4V. UVLO controls the whole IC, and also both the negative power supply charge pump and the headphone amplifier during power down.

(4) TSD
BD88400FJ has overheating protection function (TSD: Thermal Shutdown). The headphone amplifier shutdowns when overheating occurs due to headphone amplifier illegal operation. (The detection temp. $145°C_{@Typ}$)

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2. Evaluation Board

BD88400FJ evaluation Board loads and operates with the necessary parts only. It uses RCA Connector for input terminal and Headphone jack (φ=3.5mm) for output terminal. Therefore it can easily connect between Audio equipment. Also, it can operate using a single supply (2.4V to 5.5V). The switch on the board (SDB) can control shutdown.

(Spec.)

Item	Limit	Unit
Supply Voltage Range (VDD)	2.4 to 5.5	V
Maximum Supply Current	1.0	A
Operating Temperature Range	-40 to +85	°C
Input Voltage Range	-2.5 to +2.5	V
Output Voltage Range	-2.5 to +2.5	V
Minimum Load Impedance	15	Ω

(Schematic)

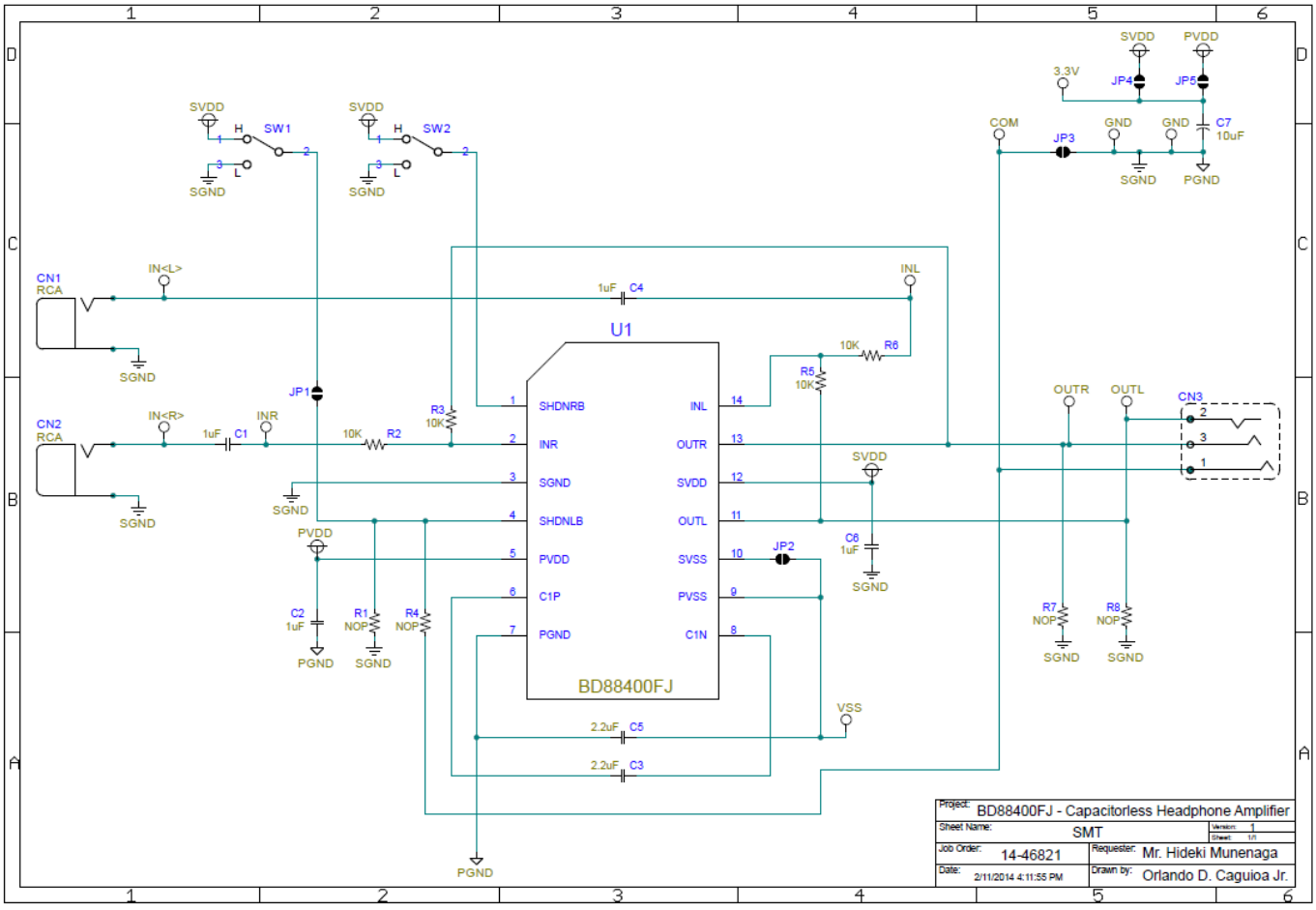


Figure 32. Evaluation Board Schematic (BD88400FJ)

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(Parts List)

Parts Name	Type	Value	Size
U1	SOP-J14pin	BD88400FJ	8.65mm x 6.00mm
C3, C5	Chip Ceramic capacitor	2.2µF	1608
C1,C2,C4,C6	Chip Ceramic capacitor	1.0µF	1608
C7	Tantalum capacitor	10µF	3216
R2,R3,R5,R6	Chip Resistor	10kΩ	1608
R7, R8	Chip Resistor	Open	-
CN3	Headphone jack	-	φ=3.5mm

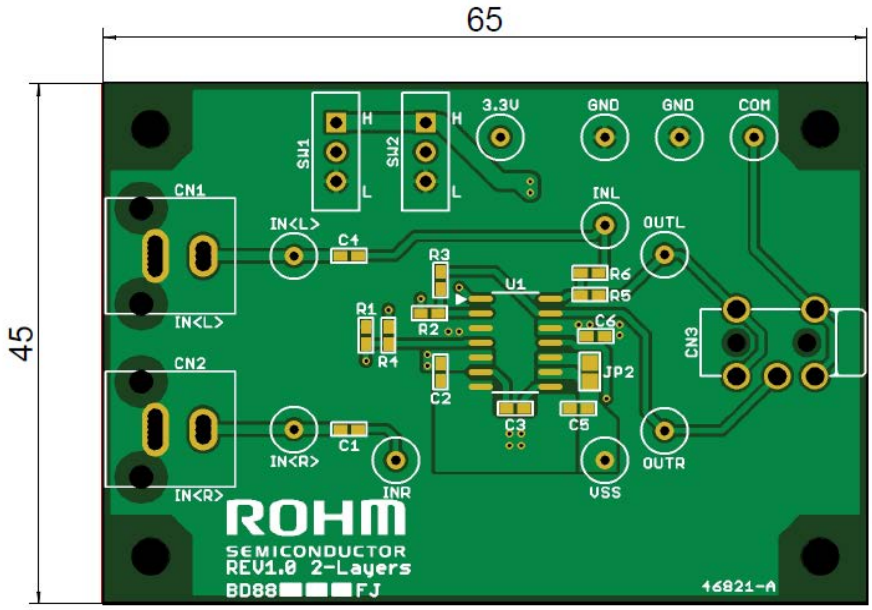
(Operation procedure)

① Turn OFF the switch (SHNDLB/SHDNRB) on evaluation board.
② Connect the positive terminal of the power supply to the VDD pin and ground terminal to the GND pin.
③ Connect the left output of the audio source to the INL and connect the right output to the INR.
④ Turn ON the power supply.
⑤ Turn ON the switch (SHDNLB/SHDNRB) on the evaluation board. (H)
⑥ Input the audio source.

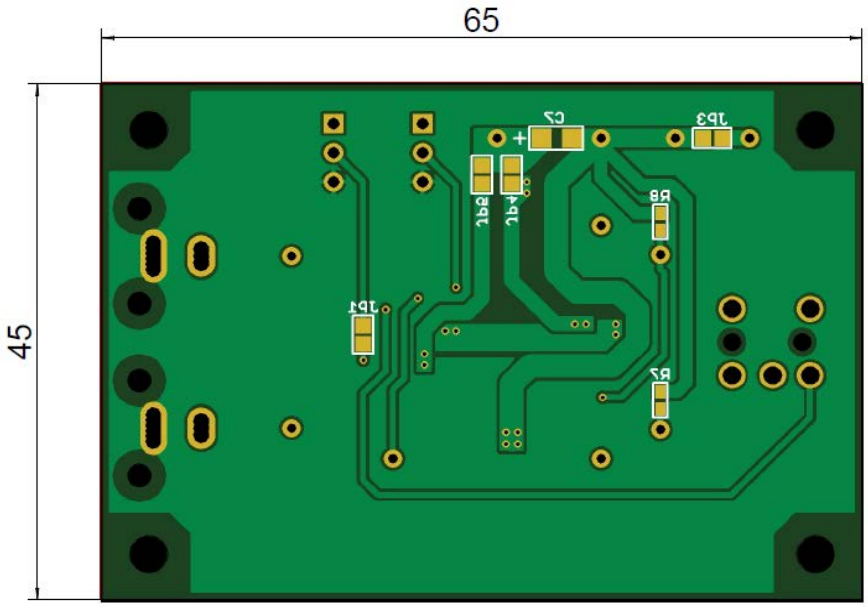
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(Board Layout)



(TOP LAYER - TOP VIEW)



(BOTTOM LAYER – TOP VIEW)

Figure 33. ROHM Application Board Layout (BD88400FJ)

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Power Dissipation

Figure 34 shows the reference value of the thermal derating curve.

(Conditions)
This value is for mounted on the ROHM standard board
Board size: 70mm x 70mm x 1.6mm (FR4, 1-Layer PCB)

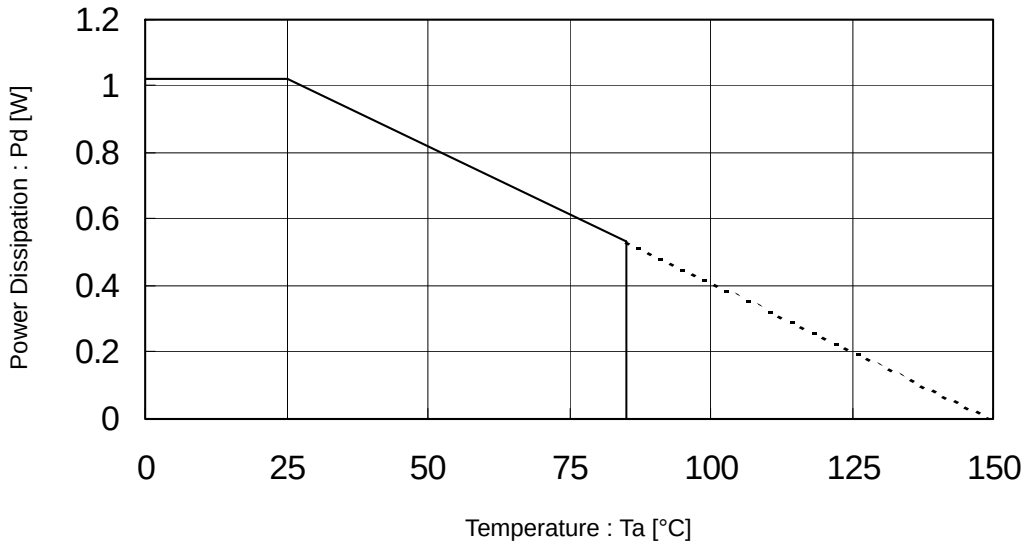
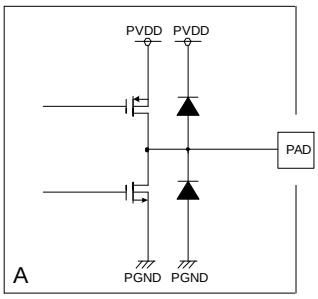


Figure 34. Thermal Derating Curve

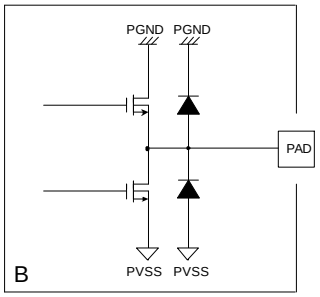
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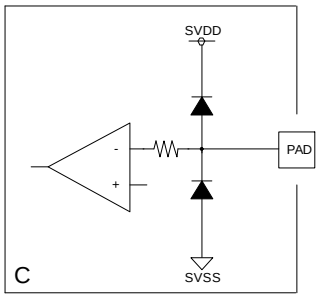
I/O Equivalent Circuits



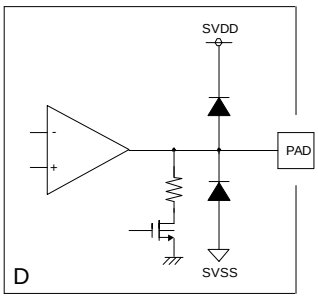
PIN6



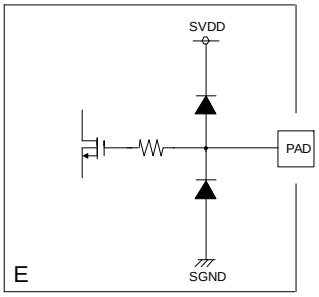
PIN8



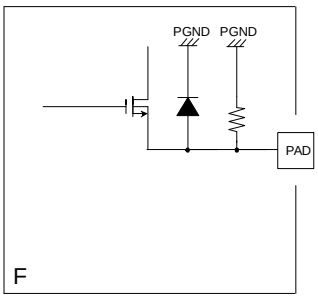
PIN2,14



PIN11,13



PIN1,4



PIN9

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

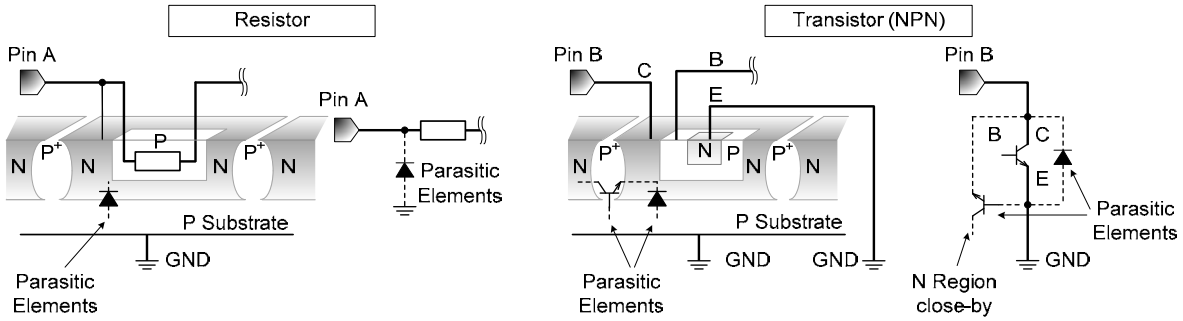


Figure 35. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over-Current Protection Circuit (OCP)

This IC has a built-in overcurrent protection circuit that activates when the output is accidentally shorted. However, it is strongly advised not to subject the IC to prolonged shorting of the output.

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Ordering Information

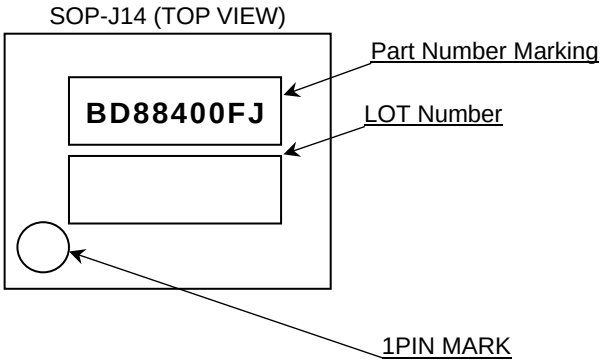
B D 8 8 4 0 0 F J - GE 2

Part Number

Package
FJ: SOP-J14

Packaging and forming specification
GE2: Embossed tape and reel

Marking Diagram

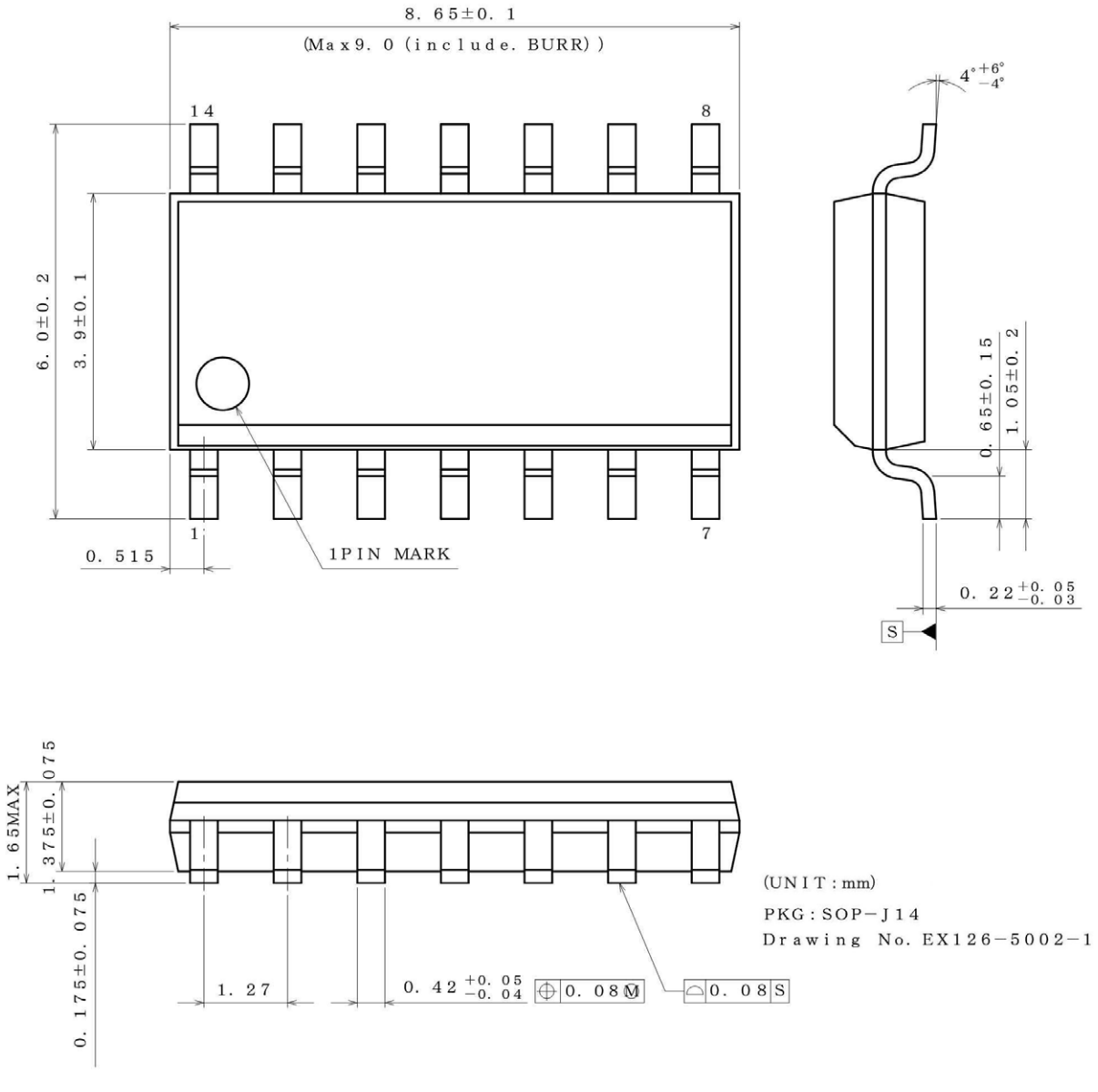


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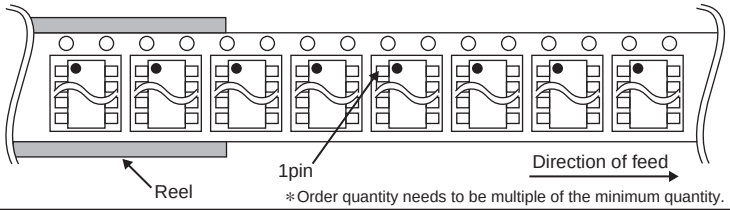
Physical Dimension, Tape and Reel Information

Package Name	SOP-J14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
26.May.2014	001	New Release.
07.Aug.2014	002	p.6 Electrical Characteristics Limit : Offset Voltage Max ±5.0mV -> ±6.0mV

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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