

Addendum: Automotive Mobile LPDDR2 SDRAM

MT42L32M16D1, MT42L32M32D2, MT42L16M32D1

Introduction

This addendum provides information for the fuse-blow automotive (FA) option for the Micron 512Mb Mobile Low-Power DDR2 SDRAM (LPDDR2) device. The FA option device disables the device power-saving functionality.

This addendum does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications unless specified herein. Information provided here is in addition to or supersedes information in the device data sheet.

Features

- Ultra low-voltage core and I/O power supplies
 - $V_{DD2} = 1.14\text{--}1.30\text{V}$
 - $V_{DDCA}/V_{DDQ} = 1.14\text{--}1.30\text{V}$
 - $V_{DD1} = 1.70\text{--}1.95\text{V}$
- Clock frequency range
 - 400–10 MHz (data rate range: 800–20 Mb/s/pin)
- Four-bit pre-fetch DDR architecture
- Four internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- On-chip temperature sensor: self-refresh rate control
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, “green” packaging

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	t_{RCD}/t_{RP}
-25	400	800	6	3	Typical
-3	333	667	5	2	Typical

Options	Marking
• V_{DD2} : 1.2V	L
• Configuration – 4 Meg x 32 x 4 banks – 8 Meg x 16 x 4 banks – 2 x 8 Meg x 16 x 4 banks	16M32 32M16 32M32
• Device type – LPDDR2-S4, 1 die in package – LPDDR2-S4, 2 die in package	D1 D2
• FBGA “green” package – 134-ball FBGA (10mm x 11.5mm) – 168-ball FBGA (12mm x 12mm)	AC LG
• Timing – cycle time – 2.5ns @ RL = 6 – 3.0ns @ RL = 5	-25 -3
• Automotive certified – Fuse-blow, Package-level burn-in	FA
• Operating temperature range – From -40°C to $+105^{\circ}\text{C}$	AT
• Revision	:A

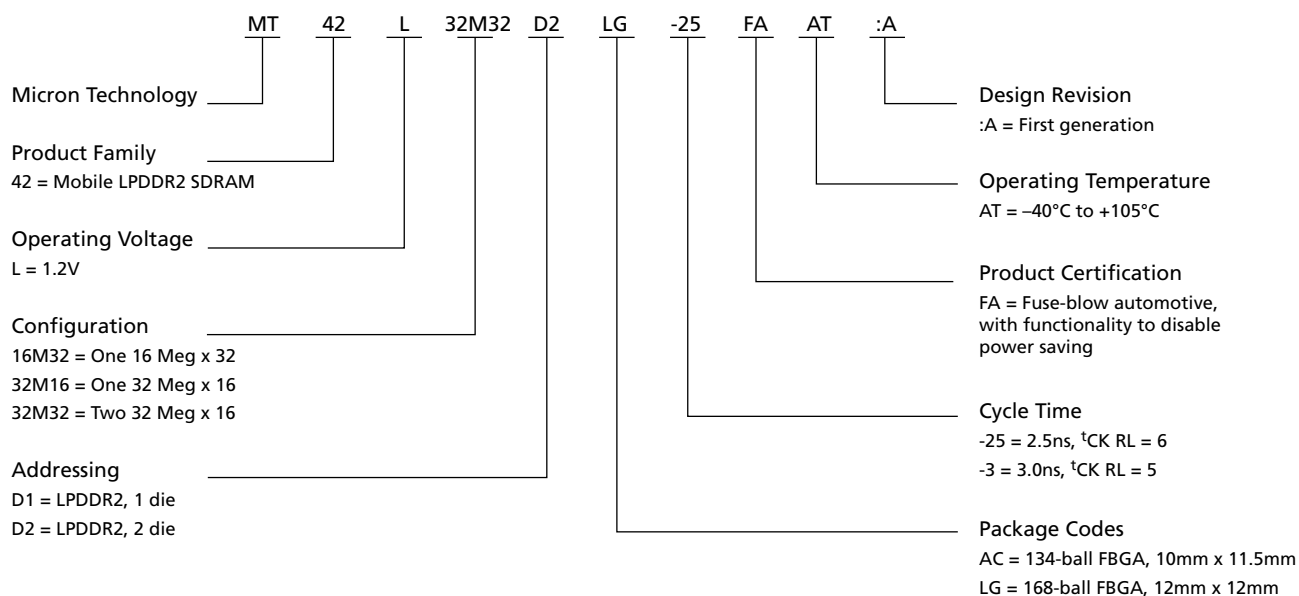
Table 2: S4 Configuration Addressing

Architecture	16 Meg x 32	32 Meg x 16	32 Meg x 32
Die configuration	4 Meg x 32 x 4 banks	8 Meg x 16 x 4 banks	2 x 8 Meg x 16 x 4 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	512 (A[8:0])	1K (A[9:0])	1K (A[9:0])
Number of die	1	1	2
Number of channels	1	1	1
Die per rank	1	1	2
Ranks per channel	1	1	1

See Package Block Diagrams for descriptions of signal connections and die configurations for each respective architecture.

Part Numbering

Figure 1: 512Mb LPDDR2 Part Numbering



General Description

The 512Mb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The LPDDR2-S4 device is internally configured as an four-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ} .

I_{DD} Specifications

Table 3: 16 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD01}	V _{DD1}	9	9	mA
I _{DD02}	V _{DD2}	29	29	
I _{DD0,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD2P1}	V _{DD1}	200	200	μA
I _{DD2P2}	V _{DD2}	500	500	
I _{DD2P,in}	V _{DDCA} + V _{DDQ}	75	75	
I _{DD2PS1}	V _{DD1}	200	200	μA
I _{DD2PS2}	V _{DD2}	500	500	
I _{DD2PS,in}	V _{DDCA} + V _{DDQ}	75	75	
I _{DD2N1}	V _{DD1}	2	2	mA
I _{DD2N2}	V _{DD2}	10	10	
I _{DD2N,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD2NS1}	V _{DD1}	0.7	0.7	mA
I _{DD2NS2}	V _{DD2}	2.5	2.5	
I _{DD2NS,in}	V _{DDCA} + V _{DDQ}	6	6	
I _{DD3P1}	V _{DD1}	750	750	μA
I _{DD3P2}	V _{DD2}	4	4	mA
I _{DD3P,in}	V _{DDCA} + V _{DDQ}	240	240	μA
I _{DD3PS1}	V _{DD1}	750	750	μA
I _{DD3PS2}	V _{DD2}	4	4	mA
I _{DD3PS,in}	V _{DDCA} + V _{DDQ}	240	240	μA
I _{DD3N1}	V _{DD1}	0.7	0.7	mA
I _{DD3N2}	V _{DD2}	13.5	13.5	
I _{DD3N,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD3NS1}	V _{DD1}	0.7	0.7	mA
I _{DD3NS2}	V _{DD2}	2.5	2.5	
I _{DD3NS,in}	V _{DDCA} + V _{DDQ}	6	6	
I _{DD4R1}	V _{DD1}	2	2	mA
I _{DD4R2}	V _{DD2}	165	165	
I _{DD4R,in}	V _{DDCA}	10	10	
I _{DD4W1}	V _{DD1}	2	2	mA
I _{DD4W2}	V _{DD2}	130	130	
I _{DD4W,in}	V _{DDCA} + V _{DDQ}	50	50	

Table 3: 16 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD51}	V _{DD1}	22	22	mA
I _{DD52}	V _{DD2}	60	60	
I _{DD5,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD5AB1}	V _{DD1}	1.2	1.2	mA
I _{DD5AB2}	V _{DD2}	12	12	
I _{DD5AB,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD61}	V _{DD1}	500	500	μA
I _{DD62}	V _{DD2}	2000	2000	
I _{DD6,in}	V _{DDCA} + V _{DDQ}	50	50	
I _{DD81}	V _{DD1}	25	25	μA
I _{DD82}	V _{DD2}	60	60	
I _{DD8,in}	V _{DDCA} + V _{DDQ}	25	25	

Table 4: 32 Meg x 16 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD01}	V _{DD1}	9	9	mA
I _{DD02}	V _{DD2}	29	29	
I _{DD0,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD2P1}	V _{DD1}	200	200	μA
I _{DD2P2}	V _{DD2}	500	500	
I _{DD2P,in}	V _{DDCA} + V _{DDQ}	75	75	
I _{DD2PS1}	V _{DD1}	200	200	μA
I _{DD2PS2}	V _{DD2}	500	500	
I _{DD2PS,in}	V _{DDCA} + V _{DDQ}	75	75	
I _{DD2N1}	V _{DD1}	2	2	mA
I _{DD2N2}	V _{DD2}	10	10	
I _{DD2N,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD2NS1}	V _{DD1}	0.7	0.7	mA
I _{DD2NS2}	V _{DD2}	2.5	2.5	
I _{DD2NS,in}	V _{DDCA} + V _{DDQ}	6	6	
I _{DD3P1}	V _{DD1}	750	750	μA
I _{DD3P2}	V _{DD2}	4	4	mA
I _{DD3P,in}	V _{DDCA} + V _{DDQ}	240	240	μA

Table 4: 32 Meg x 16 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD3PS1}	V _{DD1}	750	750	μA
I _{DD3PS2}	V _{DD2}	4	4	mA
I _{DD3PS,in}	V _{DDCA} + V _{DDQ}	240	240	μA
I _{DD3N1}	V _{DD1}	0.7	0.7	mA
I _{DD3N2}	V _{DD2}	13.5	13.5	
I _{DD3N,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD3NS1}	V _{DD1}	0.7	0.7	mA
I _{DD3NS2}	V _{DD2}	2.5	2.5	
I _{DD3NS,in}	V _{DDCA} + V _{DDQ}	6	6	
I _{DD4R1}	V _{DD1}	2	2	mA
I _{DD4R2}	V _{DD2}	125	125	
I _{DD4R,in}	V _{DDCA}	10	10	
I _{DD4W1}	V _{DD1}	2	2	mA
I _{DD4W2}	V _{DD2}	90	90	
I _{DD4W,in}	V _{DDCA} + V _{DDQ}	30	30	
I _{DD51}	V _{DD1}	22	22	mA
I _{DD52}	V _{DD2}	60	60	
I _{DD5,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD5AB1}	V _{DD1}	1.2	1.2	mA
I _{DD5AB2}	V _{DD2}	12	12	
I _{DD5AB,in}	V _{DDCA} + V _{DDQ}	10	10	
I _{DD61}	V _{DD1}	500	500	μA
I _{DD62}	V _{DD2}	2000	2000	
I _{DD6,in}	V _{DDCA} + V _{DDQ}	50	50	
I _{DD81}	V _{DD1}	25	25	μA
I _{DD82}	V _{DD2}	60	60	
I _{DD8,in}	V _{DDCA} + V _{DDQ}	25	25	

Table 5: 32 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD01}	V _{DD1}	18	18	mA
I _{DD02}	V _{DD2}	58	58	
I _{DD0,in}	V _{DDCA} + V _{DDQ}	20	20	

Table 5: 32 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD2P1}	V _{DD1}	400	400	μA
I _{DD2P2}	V _{DD2}	1000	1000	
I _{DD2P,in}	V _{DDCA} + V _{DDQ}	150	150	
I _{DD2PS1}	V _{DD1}	400	400	μA
I _{DD2PS2}	V _{DD2}	1000	1000	
I _{DD2PS,in}	V _{DDCA} + V _{DDQ}	150	150	
I _{DD2N1}	V _{DD1}	4	4	mA
I _{DD2N2}	V _{DD2}	20	20	
I _{DD2N,in}	V _{DDCA} + V _{DDQ}	20	20	
I _{DD2NS1}	V _{DD1}	1.4	1.4	mA
I _{DD2NS2}	V _{DD2}	5	5	
I _{DD2NS,in}	V _{DDCA} + V _{DDQ}	12	12	
I _{DD3P1}	V _{DD1}	1500	1500	μA
I _{DD3P2}	V _{DD2}	8	8	mA
I _{DD3P,in}	V _{DDCA} + V _{DDQ}	480	480	μA
I _{DD3PS1}	V _{DD1}	1500	1500	μA
I _{DD3PS2}	V _{DD2}	8	8	mA
I _{DD3PS,in}	V _{DDCA} + V _{DDQ}	480	480	μA
I _{DD3N1}	V _{DD1}	1.4	1.4	mA
I _{DD3N2}	V _{DD2}	27	27	
I _{DD3N,in}	V _{DDCA} + V _{DDQ}	20	20	
I _{DD3NS1}	V _{DD1}	1.4	1.4	mA
I _{DD3NS2}	V _{DD2}	5	5	
I _{DD3NS,in}	V _{DDCA} + V _{DDQ}	12	12	
I _{DD4R1}	V _{DD1}	4	4	mA
I _{DD4R2}	V _{DD2}	250	250	
I _{DD4R,in}	V _{DDCA}	20	20	
I _{DD4W1}	V _{DD1}	4	4	mA
I _{DD4W2}	V _{DD2}	180	180	
I _{DD4W,in}	V _{DDCA} + V _{DDQ}	60	60	
I _{DD51}	V _{DD1}	44	44	mA
I _{DD52}	V _{DD2}	120	120	
I _{DD5,in}	V _{DDCA} + V _{DDQ}	20	20	
I _{DD5AB1}	V _{DD1}	2.4	2.4	mA
I _{DD5AB2}	V _{DD2}	24	24	
I _{DD5AB,in}	V _{DDCA} + V _{DDQ}	20	20	

Table 5: 32 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-25	-3	
I _{DD61}	V _{DD1}	1000	1000	μA
I _{DD62}	V _{DD2}	4000	4000	
I _{DD6,in}	V _{DDCA} + V _{DDQ}	100	100	
I _{DD81}	V _{DD1}	50	50	μA
I _{DD82}	V _{DD2}	120	120	
I _{DD8,in}	V _{DDCA} + V _{DDQ}	50	50	

Table 6: 32 Meg x 16 I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit
Full array	V _{DD1}	500	μA
	V _{DD2}	2000	
	V _{DDi}	50	
1/2 array	V _{DD1}	300	
	V _{DD2}	1200	
	V _{DDi}	50	
1/4 array	V _{DD1}	250	
	V _{DD2}	800	
	V _{DDi}	50	

Figure 2: 32 Meg x 16 I_{DD61} Typical Self Refresh Current vs. Temperature

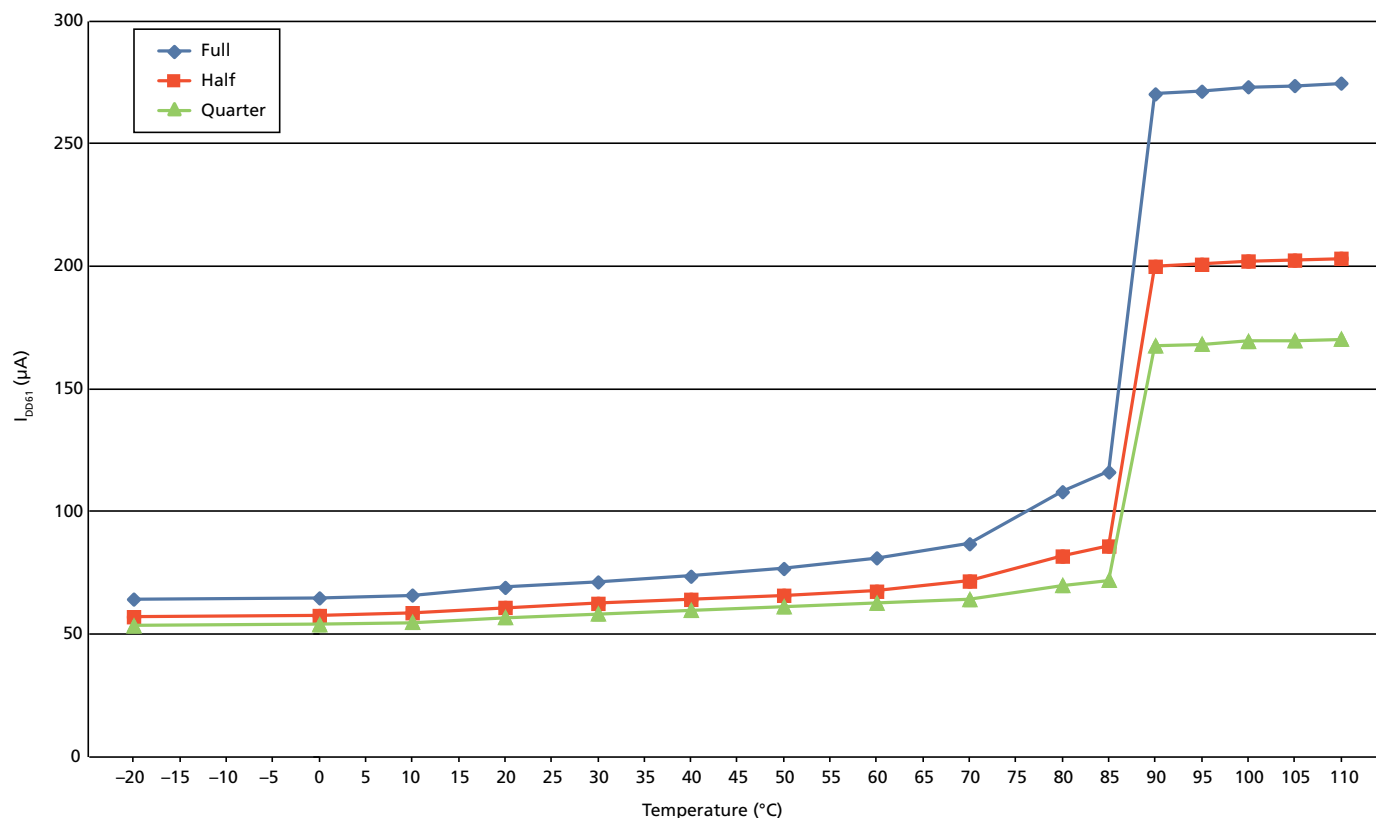


Table 7: 32 Meg x 32 DDP I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit
Full array	V _{DD1}	1000	μA
	V _{DD2}	4000	
	V _{DDi}	100	
1/2 array	V _{DD1}	600	
	V _{DD2}	2400	
	V _{DDi}	100	
1/4 array	V _{DD1}	500	
	V _{DD2}	1600	
	V _{DDi}	100	



Revision History

Rev. B – 11/15

- Production release

Rev. A – 06/15

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.