Single 2-Input AND Gate

NL17SG08

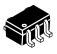
The NL17SG08 MiniGate™ is an advanced high−speed CMOS 2−input AND gate in ultra−small footprint.

The NL17SG08 input and output structures provide protection when voltages up to 3.6 V are applied.

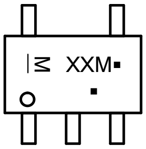
Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 2.5 ns (Typ) at V_{CC} = 3.0 V, C_L = 15 pF
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Available in SC−88A, SOT−953 and UDFN Packages
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen−Free/BFR−Free and RoHS−Compliant

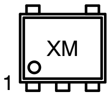
MARKING DIAGRAMS

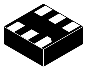


SC−88A
DF SUFFIX
CASE 419A

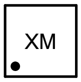


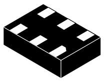
SOT−953
CASE 527AE



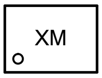


UDFN6
1.0 x 1.0
CASE 517BX





UDFN6
1.45 x 1.0
CASE 517AQ



XX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

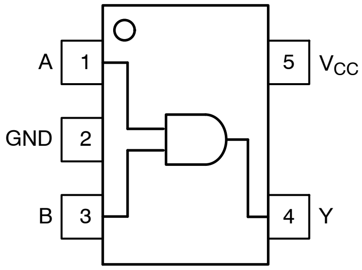


Figure 1. SOT−953
(Top Thru View)

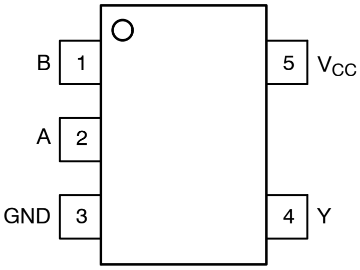


Figure 2. SC−88A
(Top View)

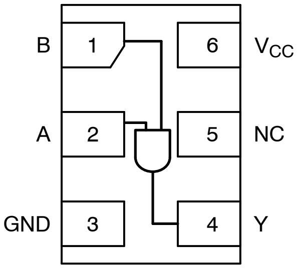


Figure 3. UDFN6
(Top View)

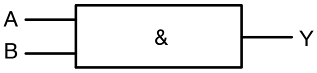


Figure 4. Logic Symbol

PIN ASSIGNMENT

PIN	SOT−953	SC−88A	UDFN6
1	A	B	B
2	GND	A	A
3	B	GND	GND
4	Y	Y	Y
5	V_{CC}	V_{CC}	NC
6	−	−	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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Table 1. MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +4.3	V
V_{IN}	DC Input Voltage	−0.5 to +4.3	V
V_{OUT}	DC Output Voltage Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current V_{OUT} < GND	−20	mA
I_{OUT}	DC Output Source/Sink Current	±20	mA
I_{CC} or I_{GND}	DC Supply Current Per Supply Pin or Ground Pin	±20	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SC−88A SOT−953 UDFN6	377 254 154	°C/W
P_D	Power Dissipation in Still Air at 85°C SC−88A SOT−953 UDFN6	332 491 812	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 4)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm – by – 1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	0.9	3.6	V
V_{IN}	Digital Input Voltage	0	3.6	V
V_{OUT}	Output Voltage Active Mode (High or Low State) Tri−State Mode (Note 1) Power Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	V
T_A	Operating Free−Air Temperature	−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate V_{CC} = 3.3 V ± 0.3 V	0	10	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 3. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		0.9	−	V_{CC}	−	−	−	V
			1.1 to 1.3	0.7 x V_{CC}	−	−	0.7 x V_{CC}	−	
			1.4 to 1.6	0.65 x V_{CC}	−	−	0.65 x V_{CC}	−	
			1.65 to 1.95	0.65 x V_{CC}	−	−	0.65 x V_{CC}	−	
			2.3 to 2.7	1.7	−	−	1.7	−	
			3.0 to 3.6	2.0	−	−	2.0	−	
V_{IL}	Low−Level Input Voltage		0.9	−	GND	−	−	−	V
			1.1 to 1.3	−	−	0.3 x V_{CC}	−	0.3 x V_{CC}	
			1.4 to 1.6	−	−	0.35 x V_{CC}	−	0.35 x V_{CC}	
			1.65 to 1.95	−	−	0.35 x V_{CC}	−	0.35 x V_{CC}	
			2.3 to 2.7	−	−	0.7	−	0.7	
			3.0 to 3.6	−	−	0.8	−	0.8	
V_{OH}	High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		I_{OH} = −20 μA	0.9	−	0.75	−	−	−	
		I_{OH} = −0.3 mA	1.1 to 1.3	0.75 x V_{CC}	−	−	0.75 x V_{CC}	−	
		I_{OH} = −1.7 mA	1.4 to 1.6	0.75 x V_{CC}	−	−	0.75 x V_{CC}	−	
		I_{OH} = −3.0 mA	1.65 to 1.95	V_{CC} − 0.45	−	−	V_{CC} − 0.45	−	
		I_{OH} = −4.0 mA	2.3 to 2.7	2.0	−	−	2.0	−	
		I_{OH} = −8.0 mA	3.0 to 3.6	2.48	−	−	2.48	−	
V_{OL}	Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		I_{OL} = 20 μA	0.9	−	0.1	−	−	−	
		I_{OL} = 0.3 mA	1.1 to 1.3	−	−	0.25 x V_{CC}	−	0.25 x V_{CC}	
		I_{OL} = 1.7 mA	1.4 to 1.6	−	−	0.25 x V_{CC}	−	0.25 x V_{CC}	
		I_{OL} = 3.0 mA	1.65 to 1.95	−	−	0.45	−	0.45	
		I_{OL} = 4.0 mA	2.3 to 2.7	−	−	0.4	−	0.4	
		I_{OL} = 8.0 mA	2.7 to 3.6	−	−	0.4	−	0.4	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	−	−	±0.1	−	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V; V_{OUT} = 0 V to 3.6 V	0	−	−	1.0	−	10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	0.9 to 3.6	−	−	1.0	−	10.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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Table 4. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25° C			T_A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y (Figures 5 and 6)	C_L = 10 pF, R_L = 1 MΩ	0.9	-	46.5	–	-	–	ns
			1.1 to 1.3	-	14.1	26.7	-	31.7	
			1.4 to 1.6	-	5.9	9.6	-	11.3	
			1.65 to 1.95	-	4.5	7.0	-	7.5	
			2.3 to 2.7	-	2.9	4.4	-	4.9	
			3.0 to 3.6	-	2.2	3.5	-	4.1	
		C_L = 15 pF, R_L = 1 MΩ	0.9	-	47.9	–	-	–	ns
			1.1 to 1.3	-	14.4	27.3	-	32.4	
			1.4 to 1.6	-	6.5	9.5	-	12.6	
			1.65 to 1.95	-	5.0	7.7	-	8.0	
			2.3 to 2.7	-	3.2	4.9	-	5.6	
			3.0 to 3.6	-	2.5	3.8	-	4.4	
		C_L = 30 pF, R_L = 1 MΩ	0.9	-	52.5	–	-	–	ns
			1.1 to 1.3	-	15.3	29.3	-	34.7	
			1.4 to 1.6	-	8.9	11.8	-	14.9	
			1.65 to 1.95	-	6.9	10.3	-	10.8	
			2.3 to 2.7	-	4.4	6.4	-	6.8	
			3.0 to 3.6	-	3.5	4.9	-	5.4	

Table 5. CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	3.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, V_{CC} = 0.9 V to 3.6 V, V_{IN} = 0 V or V_{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

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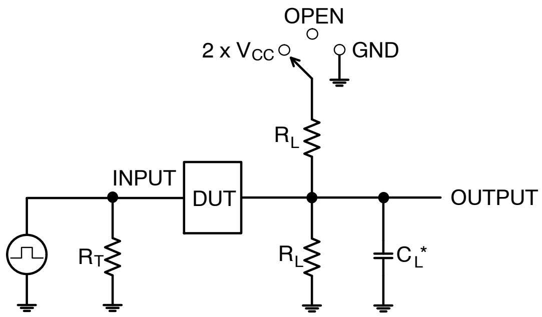


Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 5. Test Circuit

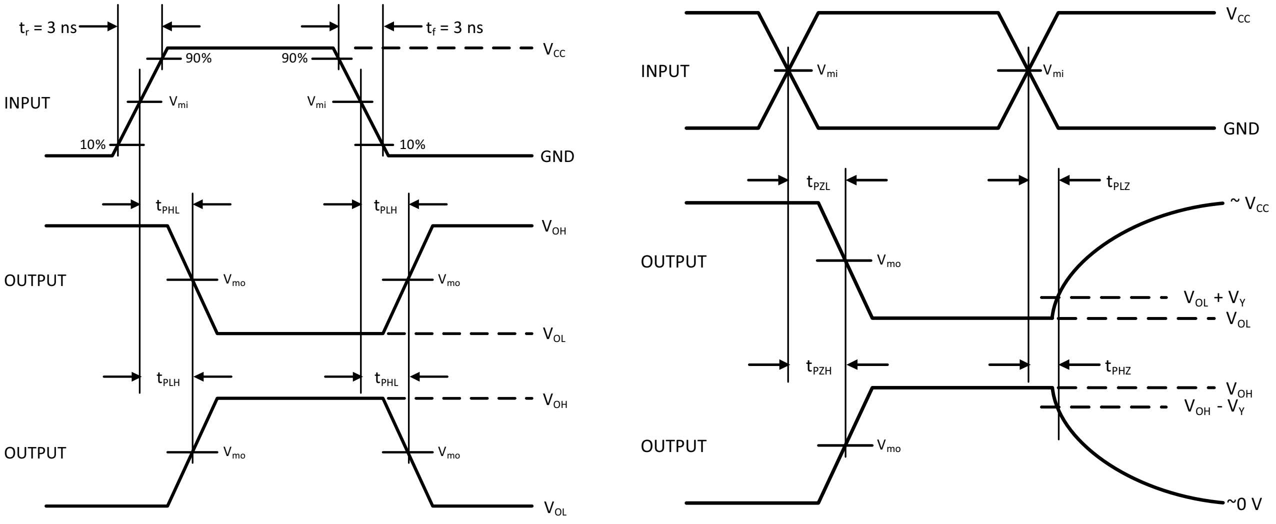


Figure 6. Switching Waveforms

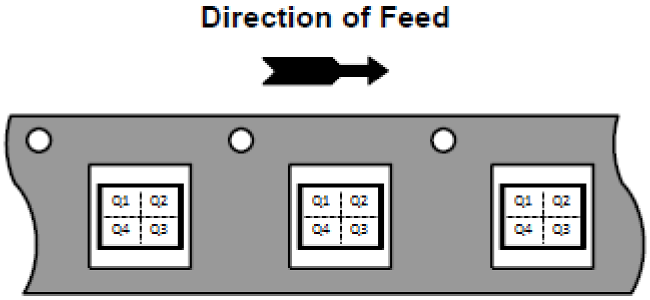
ORDERING INFORMATION

Device	Marking	Pin 1 Orientation (See below)	Package	Shipping†
NL17SG08DFT2G	AT	Q4	SC−88A	3000 / Tape & Reel
NLV17SG08DFT2G*	AU	Q4	SC−88A	3000 / Tape & Reel
NL17SG08P5T5G	Y	Q2	SOT−953	8000 / Tape & Reel
NL17SG08AMUTCG	L (Rotated 180°CW)	9Q	UDFN6 1.45x1 mm	3000 / Tape & Reel
NL17SG08CMUTCG	L (Rotated 90°CW)	Q4	UDFN6 1x1 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

PIN 1 ORIENTATION IN TAPE AND REEL



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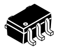
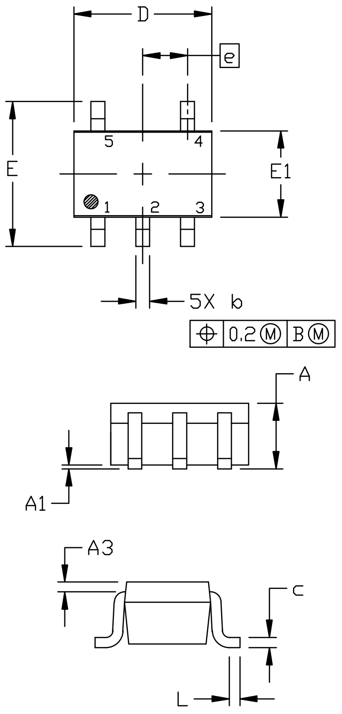
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M



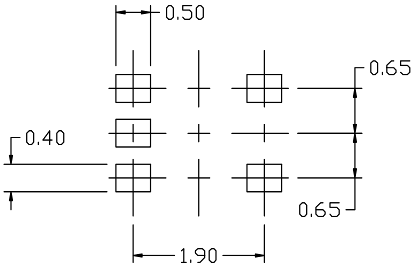
SCALE 2:1

DATE 11 APR 2023



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

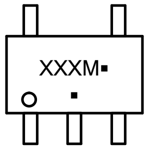
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	**98ASB42984B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

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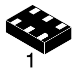
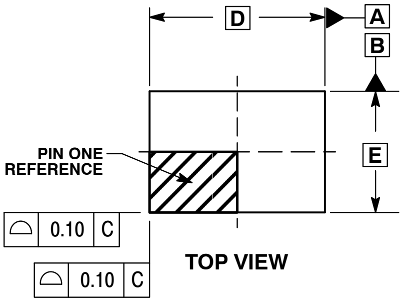


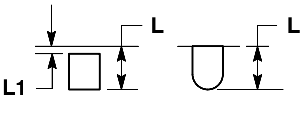
SCALE 4:1

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

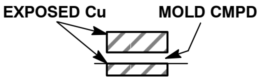
DATE 15 MAY 2008



TOP VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS

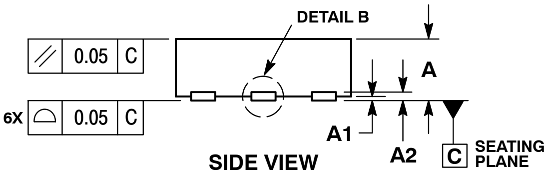


DETAIL B
OPTIONAL CONSTRUCTIONS

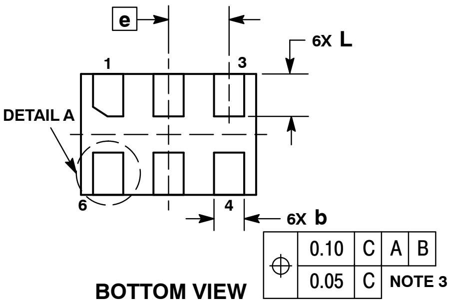
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

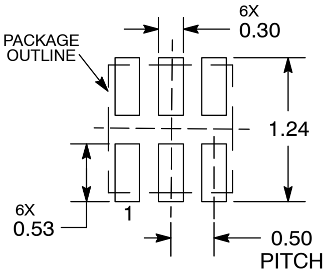


SIDE VIEW



BOTTOM VIEW

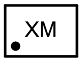
MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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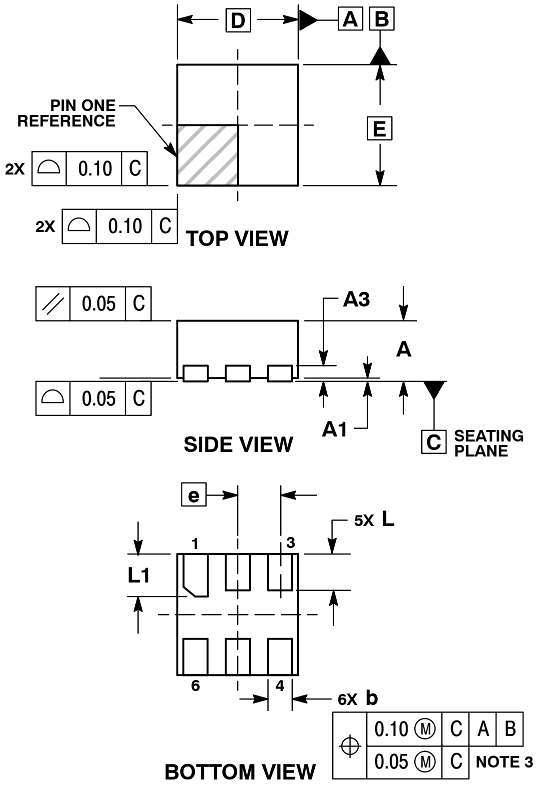
UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O

SCALE 4:1

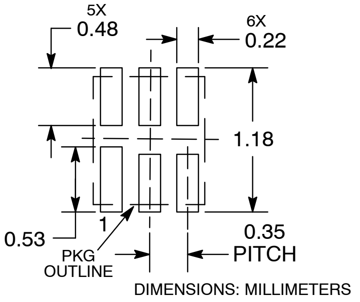
DATE 18 MAY 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

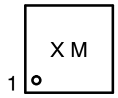
	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

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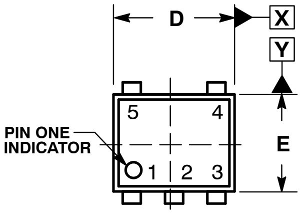
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

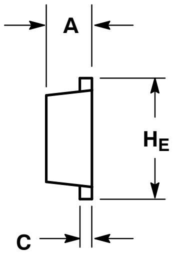
SOT−953
CASE 527AE
ISSUE E

SCALE 4:1

DATE 02 AUG 2011



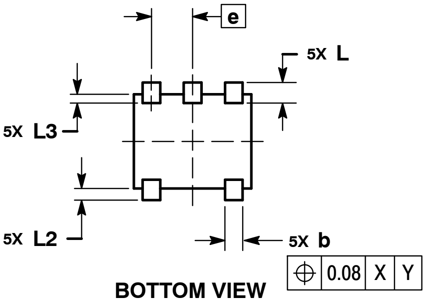
TOP VIEW



SIDE VIEW

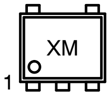
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15



BOTTOM VIEW

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Month Code

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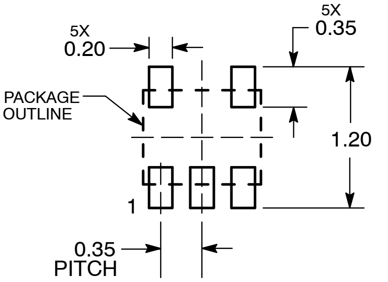
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**SOT−953**	**PAGE 1 OF 1**

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