

# MC74HCU04A

## Hex Unbuffered Inverter

### High-Performance Silicon-Gate CMOS

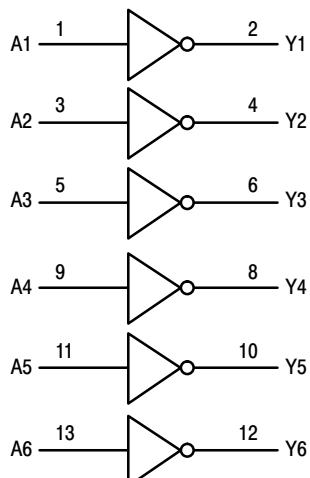
The MC74HCU04A is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04A is recommended.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V; 2.5 to 6.0 V in Oscillator Configurations
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 12 FETs or 3 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

#### LOGIC DIAGRAM



ON

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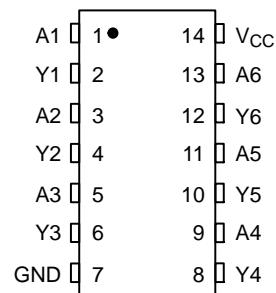


SOIC-14 NB  
D SUFFIX  
CASE 751A

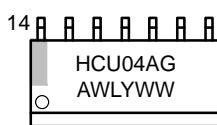


TSSOP-14  
DT SUFFIX  
CASE 948G

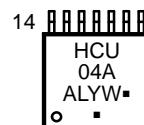
#### PIN ASSIGNMENT



#### MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	−0.5 to $V_{CC}$ + 0.5	V
$V_{out}$	DC Output Voltage (Referenced to GND)	−0.5 to $V_{CC}$ + 0.5	V
$I_{in}$	DC Input Current, per Pin	±20	mA
$I_{out}$	DC Output Current, per Pin	±25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	±50	mA
$P_D$	Power Dissipation in Still Air SOIC Package TSSOP Package	500 450	mW
$T_{stg}$	Storage Temperature	−65 to +150	°C
$T_L$	Lead Temperature, 1 mm from case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: −7 mW/°C from 65° to 125°C  
TSSOP Package: −6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	−55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage		2.0 3.0 4.5 6.0	1.7 2.5 3.6 4.8	1.7 2.5 3.6 4.8	1.7 2.5 3.6 4.8	V
$V_{IL}$	Maximum Low-Level Input Voltage		2.0 3.0 4.5 6.0	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	0.3 0.5 0.8 1.1	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = GND$ $ I_{out}  \leq 20 \mu A$	2.0 4.5 6.0	1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		$V_{in} = GND$ $ I_{out}  \leq 2.4 \text{ mA}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	3.0 4.5 6.0	2.36 3.86 5.36	2.26 3.76 5.26	2.20 3.70 5.20	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For  $V_{CC} = 2.0$  V,  $V_{out} = 0.2$  V or  $V_{CC} = 0.2$  V.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (continued)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>CC</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.5	0.5	0.5	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	0.5	0.5	0.5	μA
			3.0	0.32	0.32	0.32	
			4.5	0.32	0.37	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	0.32	0.37	0.40	μA
			6.0	1	10	40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For V<sub>CC</sub> = 2.0 V, V<sub>out</sub> = 0.2 V or V<sub>CC</sub> – 0.2 V.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	70	90	105	ns
		3.0	40	45	50	
		4.5	14	18	21	
		6.0	12	15	18	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	–	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Inverter)*		Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
			15			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

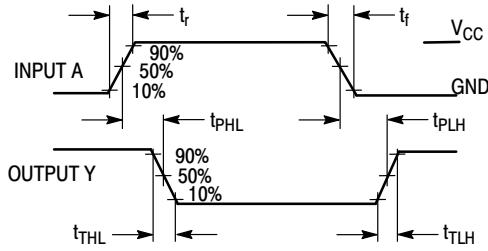
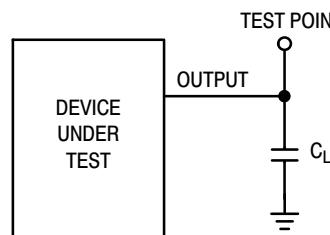


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

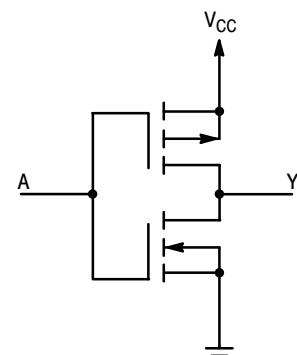


Figure 3. Logic Detail  
(1/6 of Device Shown)

# MC74HCU04A

## TYPICAL APPLICATIONS

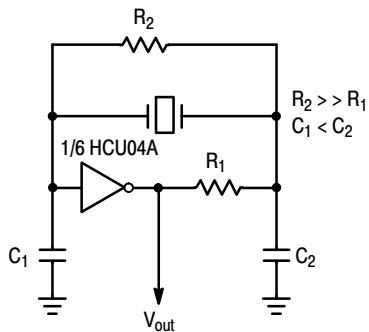


Figure 4. Crystal Oscillator

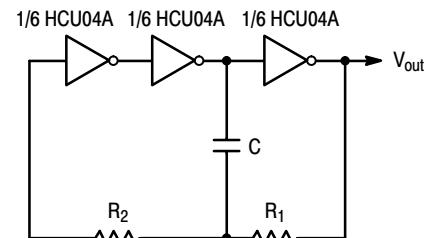


Figure 5. Stable RC Oscillator

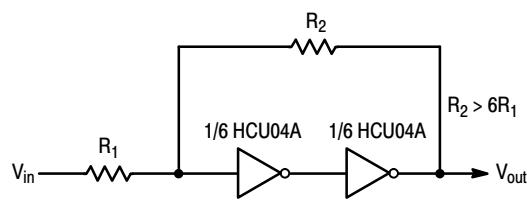


Figure 6. Schmitt Trigger

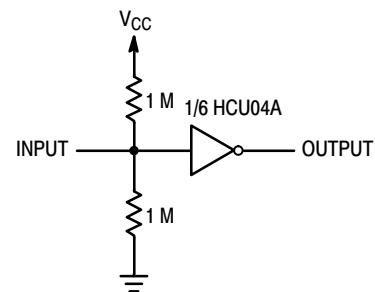


Figure 7. High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range

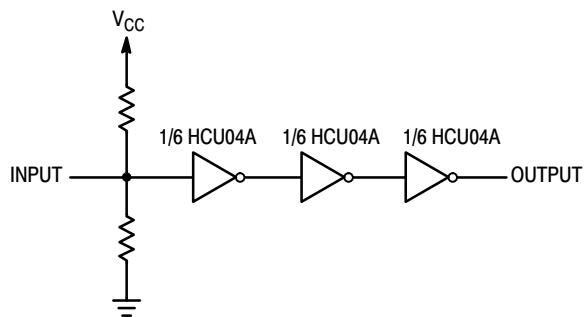
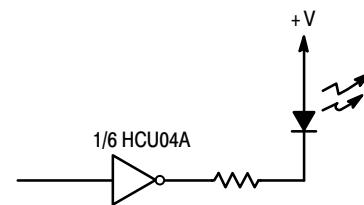


Figure 8. Multi-Stage Amplifier



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

Figure 9. LED Driver

# MC74HCU04A

## ORDERING INFORMATION

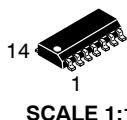
Device	Package	Shipping <sup>†</sup>
MC74HCU04ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HCU04ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HCU04ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HCU04ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HCU04ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HCU04ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

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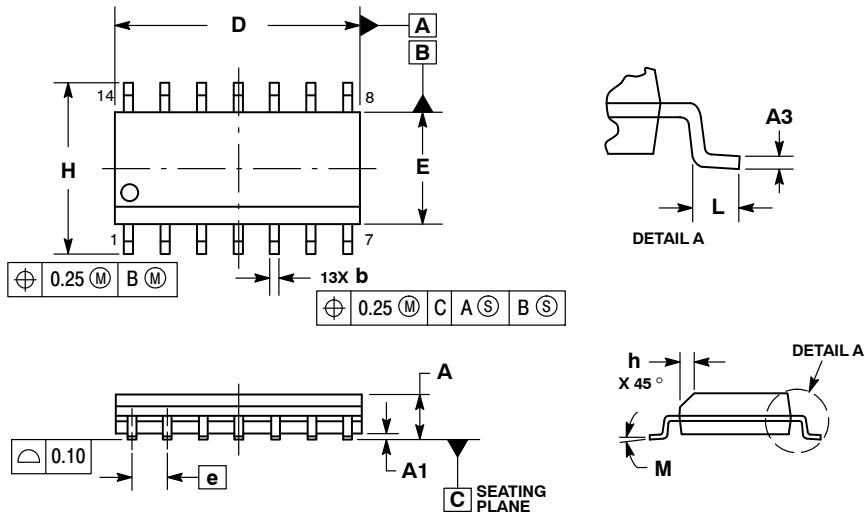
14

1

SCALE 1:1

**SOIC-14 NB**  
CASE 751A-03  
ISSUE L

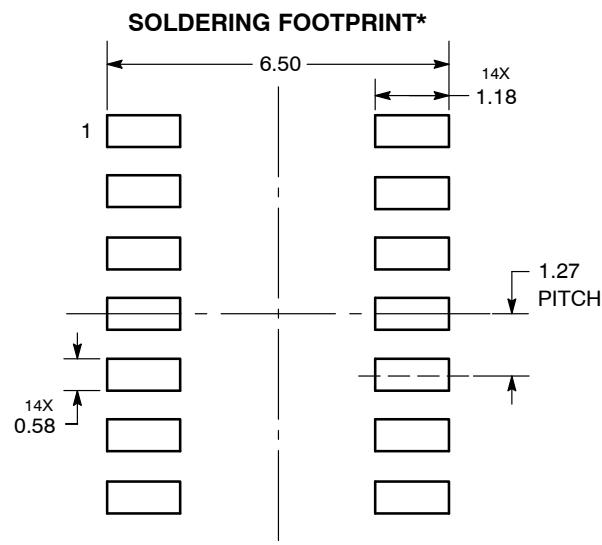
DATE 03 FEB 2016



NOTES:

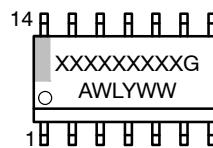
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

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**SOIC-14**  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

**STYLE 1:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 2:**  
CANCELLED

**STYLE 3:**  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

**STYLE 4:**  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 5:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 6:**  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

**STYLE 7:**  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

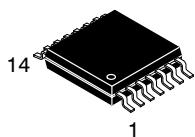
**STYLE 8:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

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**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

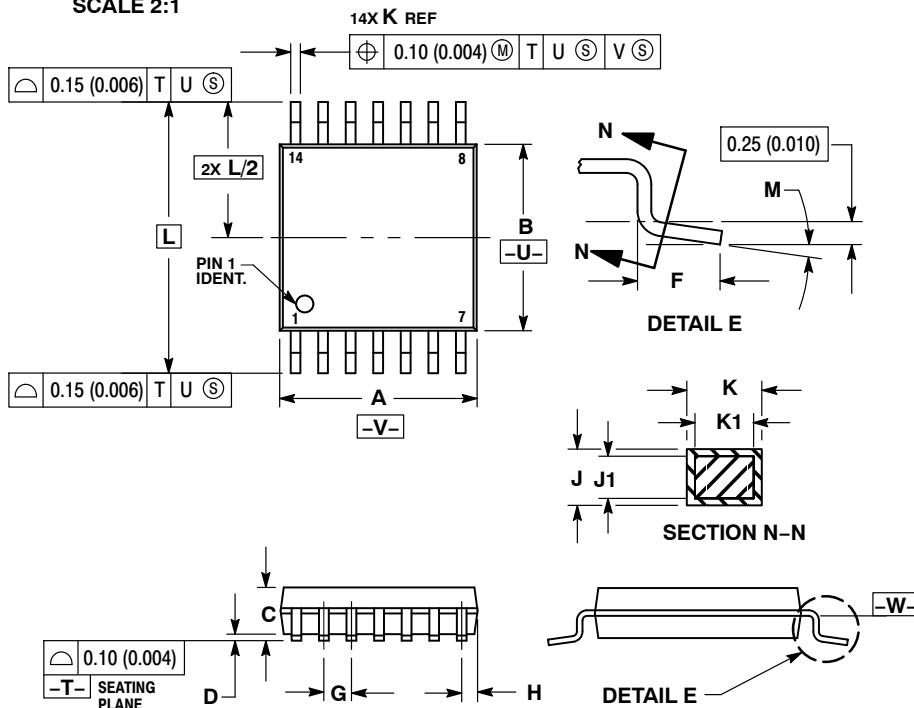
**onsemi**<sup>TM</sup>



1  
SCALE 2:1

**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

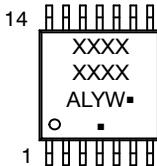


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

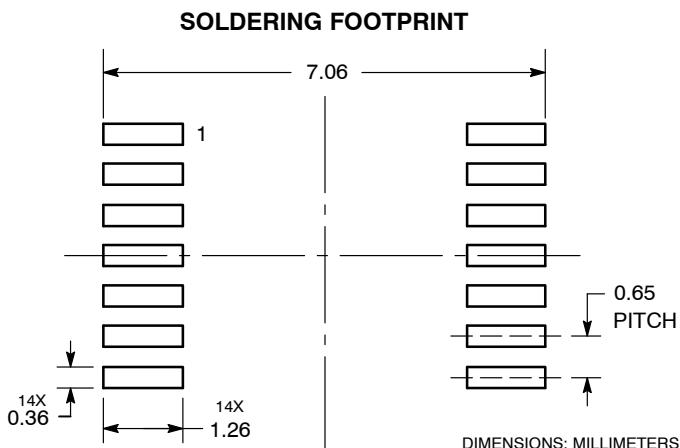
**GENERIC  
MARKING DIAGRAM\***



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "C" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



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