



# **IS66WVO32M8DALL/BLL**

# **IS67WVO32M8DALL/BLL**

**256Mb OctalRAM**

**1.8V/3.0V SERIAL PSRAM MEMORY WITH 200MHZ DTR OPI  
(OCTAL PERIPHERAL INTERFACE) PROTOCOL**

**DATA SHEET**

## 256Mb OctalRAM

SERIAL PSRAM MEMORY WITH 200MHz DTR OPI (Octal Peripheral Interface) Protocol

### FEATURES

- **Industry Standard Serial Interface**

- Octal Peripheral Interface (OPI) Protocol
- Low Signal Counts :11 Signal pins (CS#, SCLK, DQSM, SIO0~SIO7)

- **High Performance**

- Up to 400MB/s
- Double Transfer Rate (DTR) Operation
- 200MHz (400MB/s) at 105°C
- Source Synchronous Output signal during Read Operation (DQSM)
- Data Mask during Write Operation (DQSM)
- Configurable Latency for Read/Write Operation)
- Supports Variable Latency mode and Fixed Latency mode
- Configurable Drive Strength
- Supports Wrapped Burst mode and Continuous Burst mode
- Supports Deep Power Down mode
- Hidden Refresh

- **Burst Operation**

- Configurable Wrapped Burst Length : 16, 32, 64, and 128
- Word Order Burst Sequence
- Continuous Burst Operation:  
Continues Read operation until the end of array address  
Continues Write operation even after the end of array address

- **Low Power Consumption**

- Single 1.7V to 1.95V Voltage Supply
- Single 2.7V to 3.6V Voltage Supply
- 750  $\mu$ A Standby Current (typ.)

- **Hardware Features**

- **SCLK Input:** Serial clock input
- **SIO0 - SIO7:**  
Serial Data Input or Serial Data Output
- **DQSM:**
  - Output during command, address transactions as Refresh Collision Indicator
  - Output during read data transactions as Read Data Strobe
  - Input during write data transactions as Write Data Mask
- **RESET#:** Hardware Reset pin

- **Temperature Grades**

- Industrial: -40°C to +85°C
- Auto (A2) Grade: -40°C to +105°C

- **Industry Standard PACKAGE**

- B = 24-ball TFBGA 6x8mm 5x5 Array
- KGD (Call Factory)

## GENERAL DESCRIPTION

The IS66/67WVO32M8DALL/BLL are integrated memory device containing 256Mb Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 32M words by 8 bits.

The device supports Octal Peripheral Interface (Address, Command, and Data through 8 SIO pins), Very Low Signal Count (11 signal pins; SCLK, CS#, DQSM, and 8 SIOs), Hidden Refresh Operation, and Automotive temperature (A2, -40°C to +105°C) operation.

Due to DTR operation, minimum transferred data size is word (16 bits) base instead of byte (8 bits) base.

## PERFORMANCE SUMMARY

| Read / Write Operation              |         |
|-------------------------------------|---------|
| Maximum Clock Rate at 3.0V VCC/VCCQ | 200 MHz |
| Maximum Clock Rate at 1.8V VCC/VCCQ | 200 MHz |

| Maximum Current Consumption          |              |         |
|--------------------------------------|--------------|---------|
| VCC Active Read Current              | 3V, 166MHz   | 30 mA   |
|                                      | 1.8V, 200MHz | 30 mA   |
| VCC Active Write Current             | 3V, 166MHz   | 25 mA   |
|                                      | 1.8V, 200MHz | 25 mA   |
| Standby (CS# = High, 105°C )         | 3V           | 1200 uA |
|                                      | 1.8V         | 1200 uA |
| Deep Power Down (CS# = High, 105°C ) | 3V           | 50 uA   |
|                                      | 1.8V         | 30 uA   |

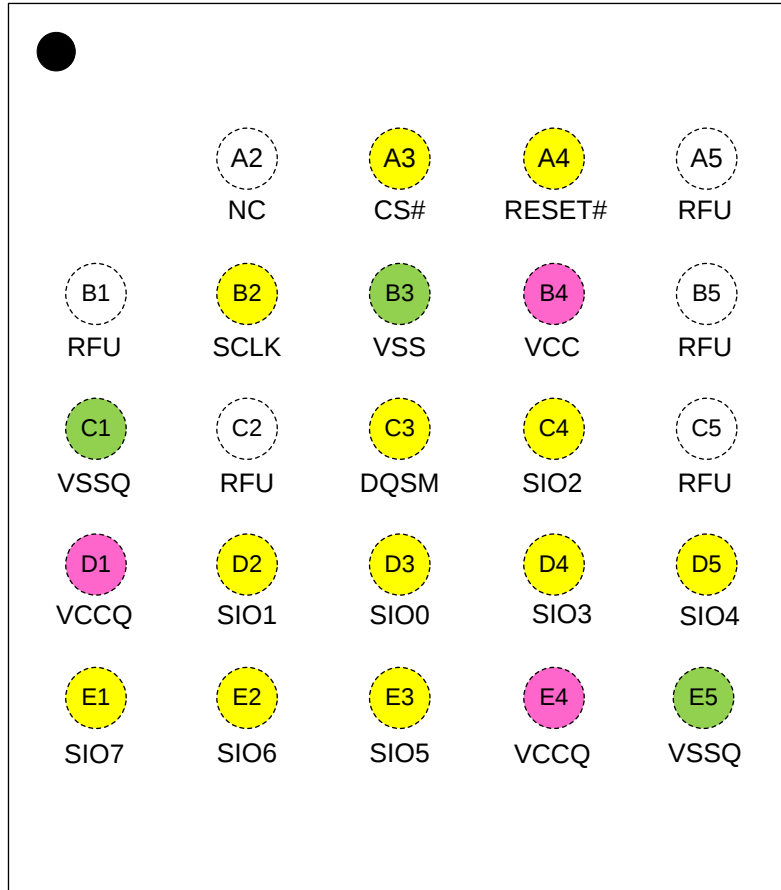
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## 1. PIN CONFIGURATION

24-ball TFBGA (5x5 ball array)

Top View, Balls Facing Down



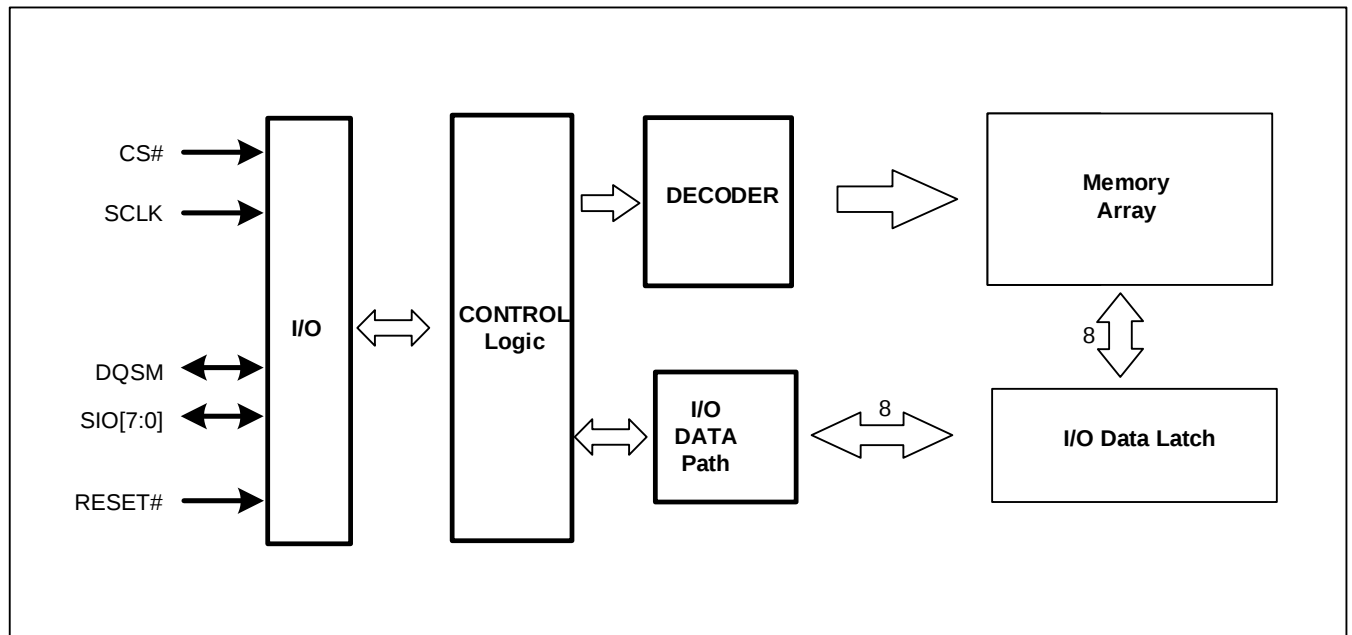
## 2. PIN DESCRIPTIONS

| SYMBOL                | TYPE         | DESCRIPTION                                                                                                                                                                                                     |
|-----------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CS#                   | INPUT        | <b>Chip Select:</b> Bus transactions are initiated with a High to Low transition. Bus transactions are initiated with a Low to High transition.                                                                 |
| DQSM                  | INPUT/OUTPUT | <b>Refresh Collision Indicator <sup>(2)</sup>, Data Strobe Signal in Read operation, and Write Data Mask in Write operation:</b>                                                                                |
| RESET# <sup>(1)</sup> | INPUT        | <b>RESET#:</b> The RESET# pin is a hardware RESET signal. When RESET# is driven High, the memory is in the normal operating mode. When RESET# is driven Low, the memory enters reset mode and output is High-Z. |
| SIO0-SIO7             | INPUT        | <b>Serial Data Input &amp; Output pins.</b>                                                                                                                                                                     |
| SCLK                  | INPUT        | <b>Serial Data Clock:</b> Synchronized Clock for input and output timing operations.                                                                                                                            |
| VCC                   | POWER        | <b>Power Supply</b>                                                                                                                                                                                             |
| VCCQ                  | POWER        | <b>IO Power Supply</b>                                                                                                                                                                                          |
| VSS                   | GROUND       | <b>Ground</b>                                                                                                                                                                                                   |
| VSSQ                  | GROUND       | <b>IO Ground</b>                                                                                                                                                                                                |
| RFU                   | Reserved     | <b>RFU:</b> Reserved for future use: May or may not be connected internally.                                                                                                                                    |
| NC                    | Unused       | <b>NC:</b> No Connect: Not connected internally. The ball may be used in PCB routing.                                                                                                                           |

### Notes:

- RESET# pin has an internal pull-up.**
- Contact ISSI MKT for DQSM without Refresh Collision Indicator

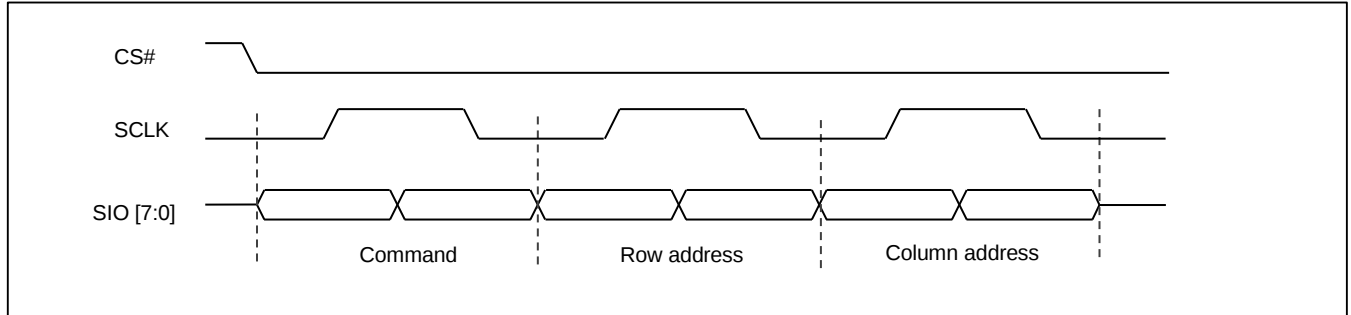
### 3. BLOCK DIAGRAM



#### 4. COMMAND AND ADDRESS ASSIGNMENTS

The device is serial interface, so all command and address inputs are transferred through SIO pins.

**Figure 4.1 Command and Address Cycles**



**Notes:**

1. The figure shows the initial three clock cycles of all operations on the OctalRAM Interface.
2. Command and Address information is "center aligned" with the clock during both Read and Write operations.

**Table 4.1 Command / Address bit assignment**

| Clock    | 1 <sup>st</sup> clock | 2 <sup>nd</sup> clock | 3 <sup>rd</sup> clock |
|----------|-----------------------|-----------------------|-----------------------|
| Function | Command               | Row address           | Column address        |
| SIO[7]   | Command               | Reserved              | CA9                   |
| SIO[6]   |                       | RA14                  | CA8                   |
| SIO[5]   |                       | RA13                  | CA7                   |
| SIO[4]   |                       | RA12                  | CA6                   |
| SIO[3]   |                       | RA11                  | CA5                   |
| SIO[2]   |                       | RA10                  | CA4                   |
| SIO[1]   |                       | RA9                   | CA3                   |
| SIO[0]   |                       | RA8                   | CA2                   |
|          |                       | RA7                   | CA1                   |
|          |                       | RA6                   | CA0 <sup>(3)</sup>    |

**Notes:**

1. The 256Mb OctalRAM address assignments:  
- Row Address 14 ~ 0: 32K (15bits), Column Address 9 ~ 0: 1k (10bits), 256Mb density = 32K X 1K X 8 (bits)
2. Data is always transferred in full word increment (word granularity -2 bytes-transfer).
3. Column Address A0 should be always 0.

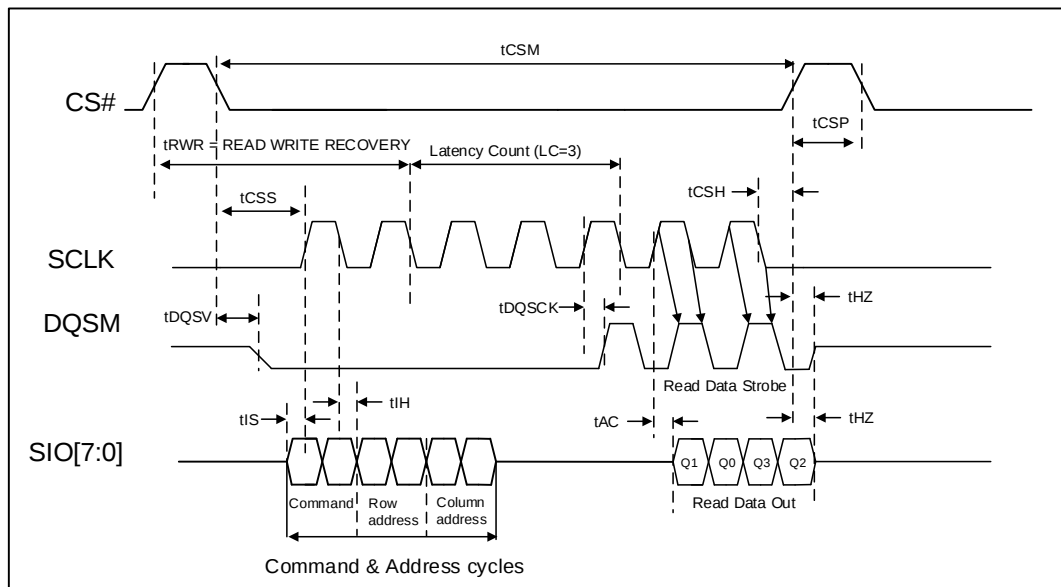
**Table 4.2 Command / Address bit assignment**

| Command                             | 1 <sup>st</sup> clock |     | 2 <sup>nd</sup> clock |     | 3 <sup>rd</sup> clock                         |     |
|-------------------------------------|-----------------------|-----|-----------------------|-----|-----------------------------------------------|-----|
|                                     | Command               |     | Row address           |     | Column address                                |     |
| Memory READ with continuous burst   | A0h                   | 00h | RA[14:0]              |     | CA[9:0]                                       |     |
| Memory READ with wrapped burst      | 80h                   | 00h | RA[14:0]              |     | CA[9:0]                                       |     |
| Memory WRITE with continuous burst  | 20h                   | 00h | RA[14:0]              |     | CA[9:0]                                       |     |
| Memory WRITE with wrapped burst     | 00h                   | 00h | RA[14:0]              |     | CA[9:0]                                       |     |
| Identification Register (read only) | C0h or E0h            | 00h | 00h                   | 00h | 00h                                           | 00h |
| Configuration Register READ         | C0h or E0h            | 00h | 00h                   | 04h | 00h                                           | 00h |
| Configuration Register WRITE        | 40h or 60h            | 00h | 00h                   | 04h | 00h                                           | 00h |
| Preamble Bit Pattern READ           | F0h                   | 00h | Don't care            |     | CA[9:1] Don't care<br>CA[0] Pattern Selection |     |

## 5. Memory READ/WRITE OPERATIONS

### 5.1 MEMORY READ OPERATIONS

Figure 5.1 Read Timing Diagram - No Refresh Collision at Variable Latency READ (1LC operation)



**Notes:**

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks, CR [8] = 1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with no refresh collision access**.
4. Read access (LC) starts once RA [7:0] is captured (falling edge of 2<sup>nd</sup> command/address clock)
5. The memory drives DQSM during read cycles.
6. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM driven by the OctalRAM.
7. Column address A0 must be 0.

The diagram shows the timing for a read operation. The signals are CS#, SCLK, DQSM, and SIO[7:0]. The SIO[7:0] signal is divided into Command, Row address, and Column address phases. The Command & Address cycles are followed by two Latency Count (LC=3) periods. The Read Data Strobe is then asserted, and the Read Data Out is valid. The timing parameters are defined as follows:

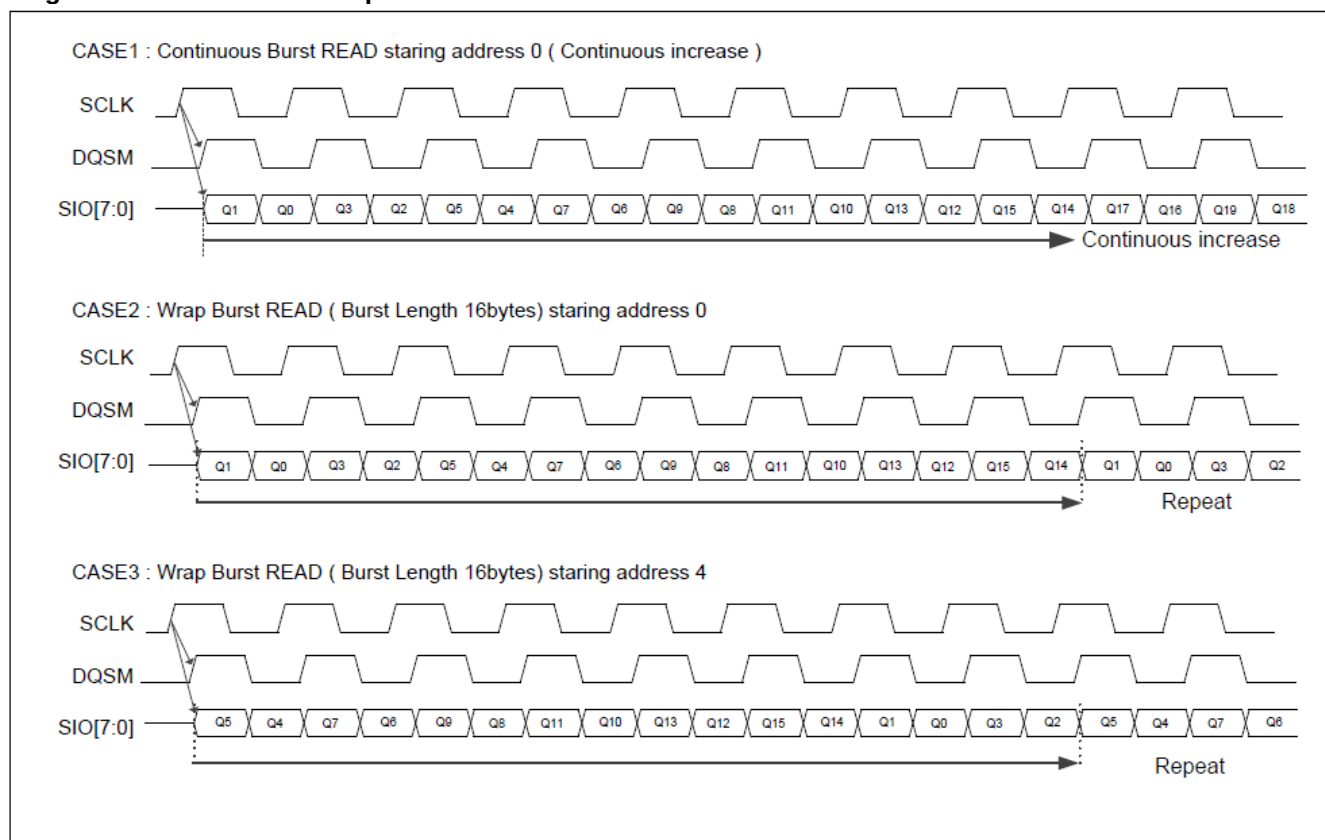
- $t_{CSS}$ : CS# setup time before SCLK.
- $t_{DOSV}$ : DQSM setup time before SCLK.
- $t_{DOSCK}$ : DQSM setup time before SCLK during the Read Data Strobe.
- $t_{CSH}$ : CS# hold time after SCLK.
- $t_{HZ}$ : DQSM hold time after SCLK.
- $t_{IS}$ : SIO[7:0] setup time before SCLK.
- $t_{IH}$ : SIO[7:0] hold time after SCLK.
- $t_{AC}$ : Read Data Strobe setup time before SCLK.
- $t_{CSM}$ : CS# setup time before SCLK during the Read Data Strobe.

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks, CR [8] =1 (DQSM 1 clock pre-cycle before Valid READ Data).
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access** (2LC operation).
4. In this Read there is a 2 Latency Count (2LC) for read access.
5. Read access (LC) starts once RA [7:0] is captured.
6. The memory drives DQSM during read cycles.
7. DQSM is a read data strobe with data values edge aligned with the transitions of DQSM.
8. Column address A0 must be 0.
9. **Fixed initial READ access latency outputs the first data at a consistent time regardless of worst-case refresh collisions.**

The diagram illustrates the timing relationships between several signals:

- CS#**: Chip Select signal. Timing parameters shown are  $t_{CH}$  (high pulse width) and  $t_{CL}$  (low pulse width).
- SCLK**: Serial Clock signal. Timing parameter shown is  $t_{CSH}$  (time from last clock edge to CS# deassertion).
- DQSM**: Data Strobe Master signal. Timing parameters shown are  $t_{DQSCK}$  (setup time before SCLK),  $t_{AC}$  (access time after SCLK), and  $t_{HZ}$  (hold time after CS# deassertion).
- Slow SIO[i]**: Slow Side Input/Output signal. Timing parameters shown are  $t_{QHS}$  (output hold time before SCLK) and  $t_{QH}$  (output hold time after SCLK).
- Fast SIO[j]**: Fast Side Input/Output signal. Timing parameters shown are  $t_{QHS}$  (output hold time before SCLK) and  $t_{QH}$  (output hold time after SCLK).
- All SIO[7:0]**: General purpose I/O signals. Timing parameters shown include  $t_{LZ}$  (input latency time),  $t_{QH}$  (output hold time after SCLK), and  $t_{DSQ}$  (data strobe delay time).

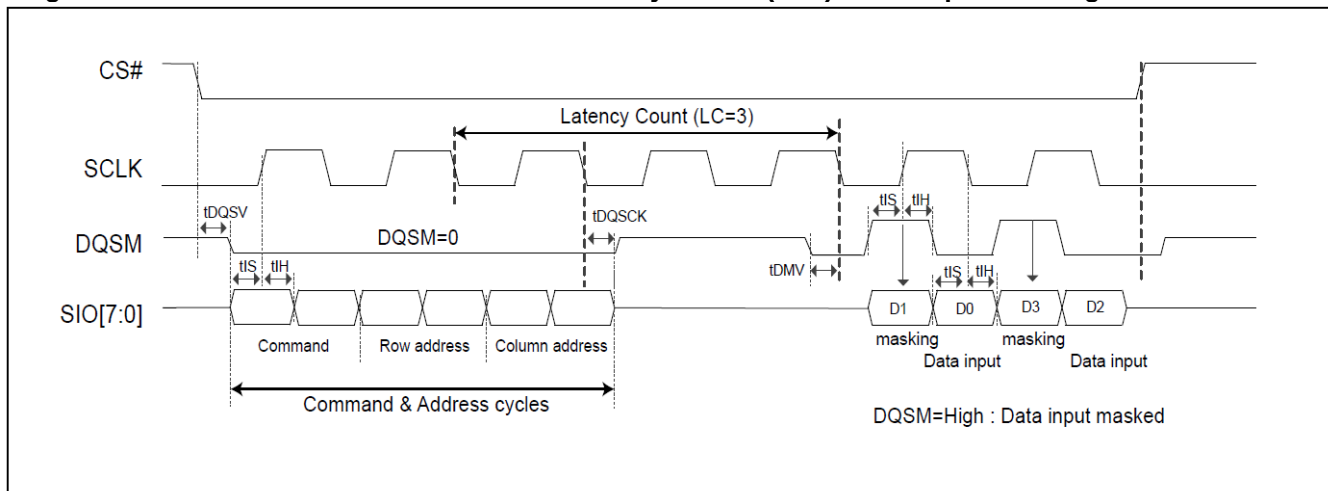
1. Burst READ data valid timing in detail.
2. tAC defines CLK transition to DQ Valid.
3. tDQSCK defines CLK transition to DQSM Valid.
4. tDQSQ defines DQSM-DQ skew.
5. tQHS defines Data Hold skew factor.
6. tQH defines DQ hold time from DQSM.

**Figure 5.4 READ Burst Wrap**

**Notes:**

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Read operation can be ended at any time by bringing CS# High.
3. Continues Read operation until last address. Continuing beyond last address, undefined data will be available.

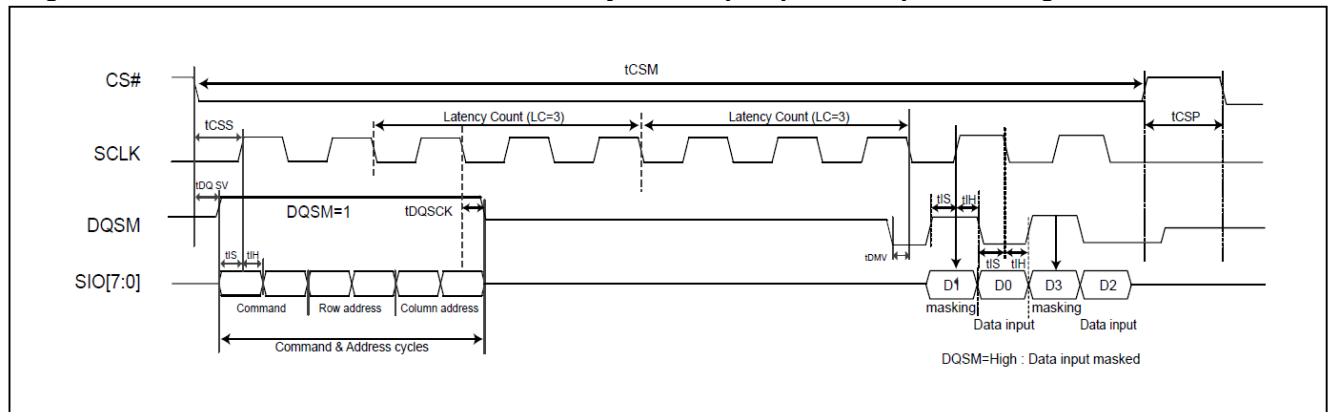
## 5.2 WRITE OPERATIONS

Figure 5.5 No Refresh Collision at Variable Latency WRITE (1LC) / Data Input Masking

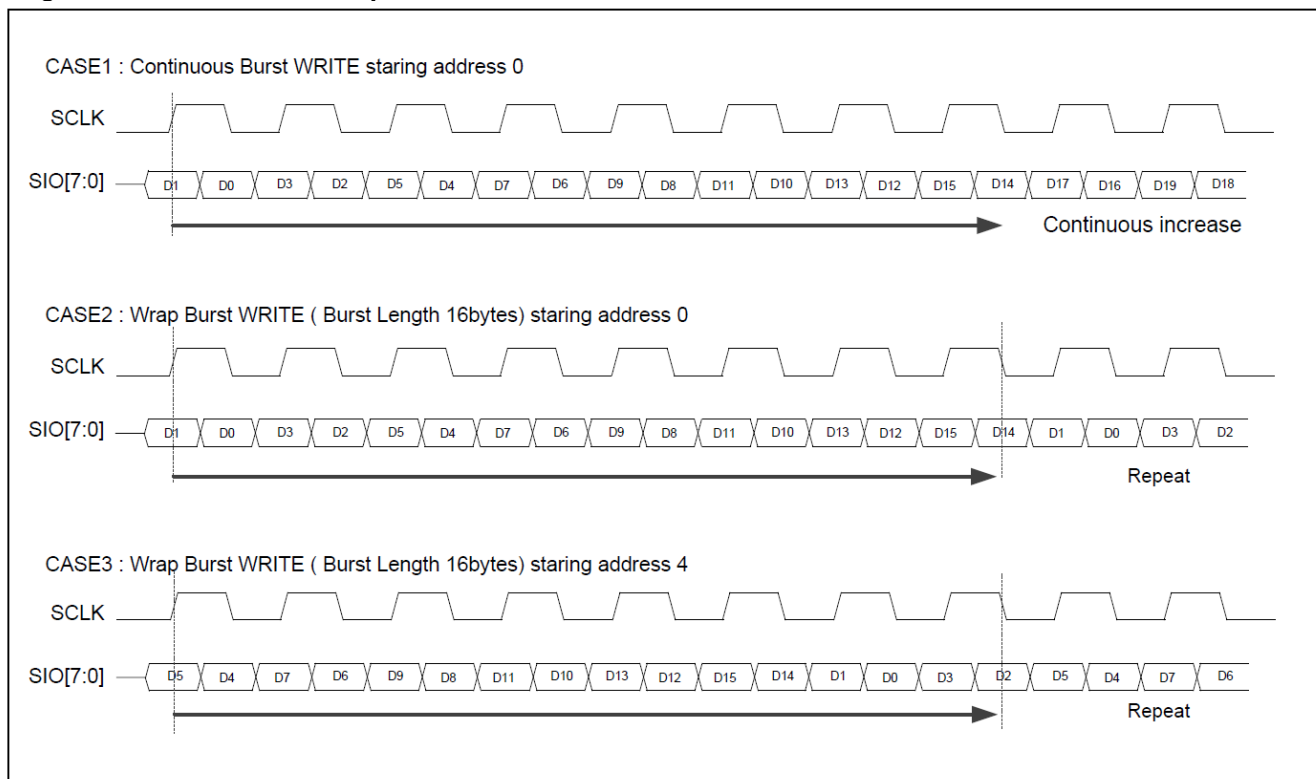
**Notes:**

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks.
3. Diagram in the figure above is representative of **variable latency with no refresh collision access**.
4. Write access (LC) starts once RA [7:0] is captured.
5. The memory drives DQSM "Low" during command address cycles and DQSM goes to "Hi-Z" after command address cycles.
6. The system memory controller must drive DQSM to a valid Low before the end of initial latency to provide a data mask preamble time.  
This can be done during the last cycle of LC cycle.
7. During Write data input, data is center aligned with the clock.
8. During Write data input, DQSM indicates whether each data byte is masked with DQSM High or not masked with DQSM Low.
9. D1, D3 are masked.
10. Column address A0 must be 0.

Figure 5.6 Refresh Collision at Variable Latency WRITE (2LC) / Data Input Masking

**Notes:**

1. The Latency count is defined by the initial latency value in a configuration register.
2. Latency count (LC) is 3 clocks.
3. Diagram in the figure above is representative of **variable latency with refresh collision or fixed-latency access. (2LC operation)**
4. **In this Write there is a latency count (2LC) for WRITE operation**
5. Write access (LC) starts once RA [7:0] is captured.
6. The memory drives DQSM High during command address cycles and DQSM goes to "Hi-Z" after command address cycles.
7. The system memory controller must drive DQSM to a valid Low before the end of initial latency to provide a data mask preamble time.  
This can be done during the last cycle of LC cycle.
8. During Write data input, data is center aligned with the clock.
9. During Write data input, DQSM indicates whether each data byte is masked with DQSM High or not masked with DQSM Low.
10. D1, D3 are masked.
11. Column address A0 must be 0.

**Figure 5.7 WRITE Burst Wrap**

**Notes:**

1. CS# can stay Low between burst operations, but CS# must not remain Low longer than tCSM.
2. Write operation can be ended at any time by bringing CS# High.
3. When continuous burst write reaches the last address in the memory array, continuing the burst will write to the beginning of the address.

### 5.3 PREAMBLE BIT DATA PATTERN READ OPERATION

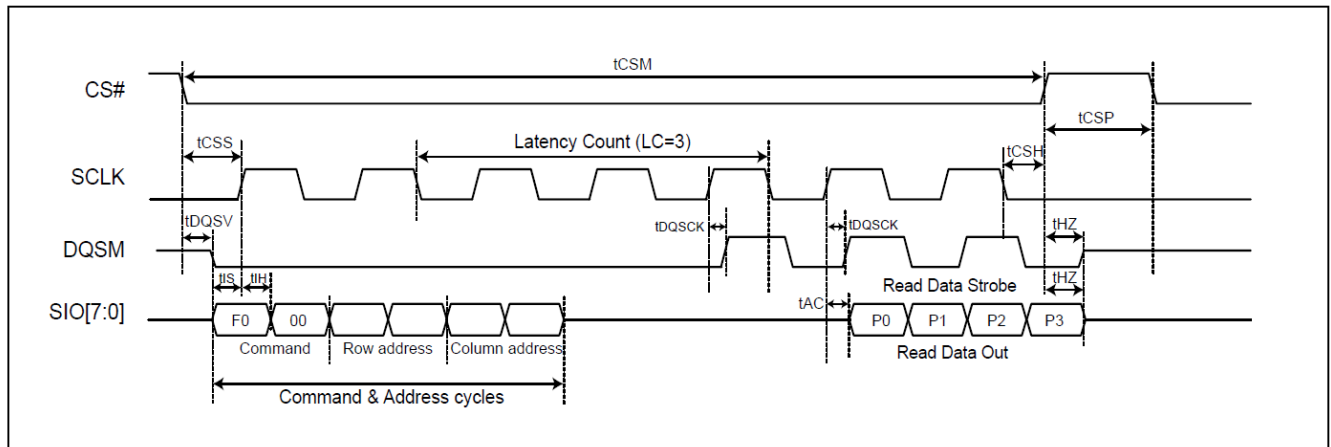
The Preamble Bit Data Pattern READ Operation can improve data capture reliability while the OctalRAM is running in high frequency, while supporting the System/Memory Controller to determine the data output valid windows more easily.

The Preamble Bit is designed as a 16-bits data pattern, it can be output by Preamble Bit READ Command (F0h + 00h). The Row Address and Column Address are “don’t care”, except Column Address A0 is used for selecting the pattern.

Once Preamble Bit feature is enabled, a fixed 16-bits data pattern will output on all SIO pins, according to A0 setting in Column Address. Refer to ["Table 5.1. Preamble Bit Data Pattern SIO assignments"](#).

The Latency Count values are defined in configuration register CR [7-4] which is the same as Read timing diagram -1LC operation case.

**Figure 5.8 Preamble Bit Data Pattern READ Timing, No Refresh Collision at Variable Latency**



**Notes:**

1. Latency Count (LC) = 3 clocks, CR[8]=1 (DQSM 1 clock pre-cycle before Valid READ Data)
2. The memory drives DQSM during the entire Data Learning Pattern Read.
3. The required latency count is device and clock frequency dependent.
4. Column address A0 is used for pattern selection, and Row address RA [14:0] and Column address CA [9:1] are don't care.

**Table 5.1 Preamble Bit Data Pattern SIO assignments**

| Column Address A0 | All SIOs (except SIO3) | SIO3                |
|-------------------|------------------------|---------------------|
| A0=0              | 0011 0100 1001 1010    | 0011 0101 0001 0100 |
| A0=1              | 0101 0101 0101 0101    | 0101 0101 0101 0101 |

## 5.4 RESET OPERATION

Figure 5.9 RESET Timing

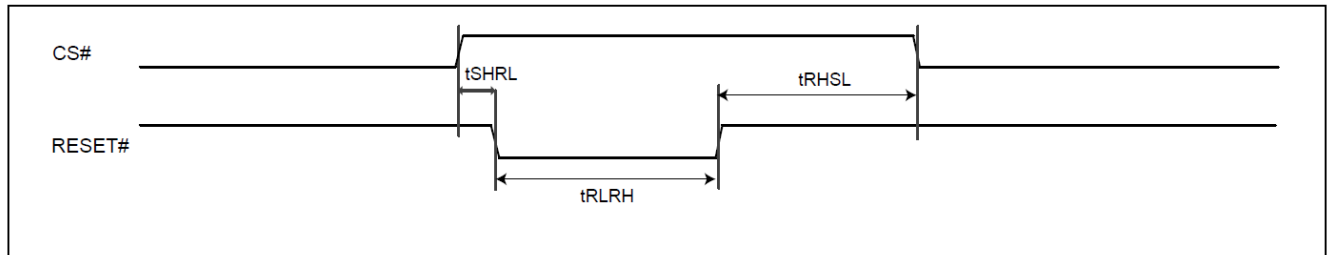
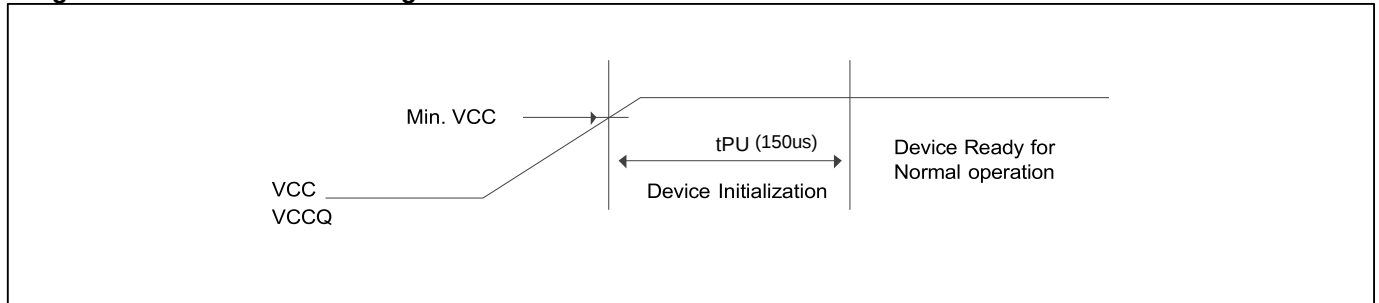


Table 5.2 RESET Timing Parameters

| Parameter  | Description                | Min | Max | Unit |
|------------|----------------------------|-----|-----|------|
| $t_{SHRL}$ | RESET# Low after CS# High  | 15  | -   | ns   |
| $t_{RLRH}$ | RESET# Low Pulse width     | 10  | -   | us   |
| $t_{RHSL}$ | RESET# High before CS# Low | 10  | -   | us   |

## 5.5 POWER-UP INITIALIZATION

Figure 5.10 POWER-UP Timing

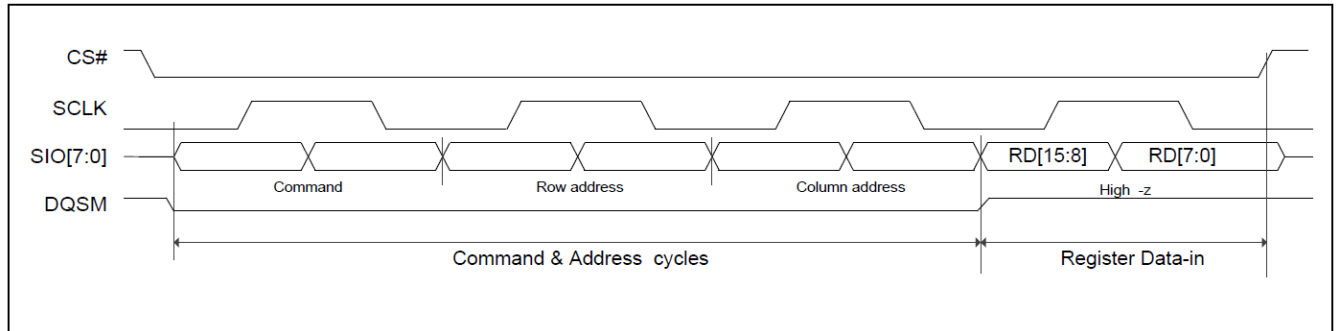


## 6. REGISTER

The device has 16 bit Configuration Register and ID Register, and they can be accessed by Register Read or Write command.

### 6.1 REGISTER READ/WRITE OPERATION

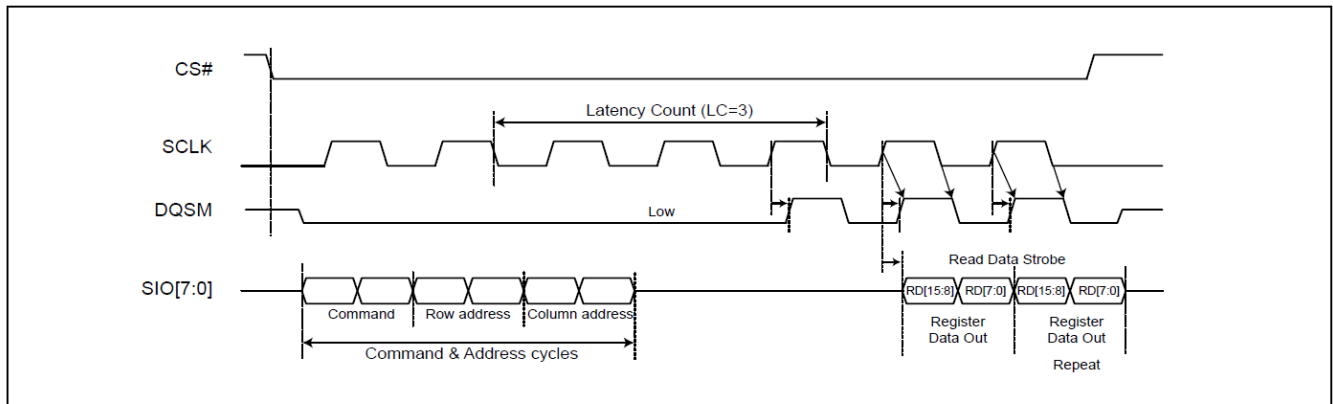
**Figure 6.1 Register WRITE, No Refresh Collision at Variable Latency**



**Notes:**

1. The device drives DQSM "Low or High for Refresh indication" during command address cycles, which must be ignored by host. DQSM goes to "Hi-Z" after command address cycles.
2. The register value is always provided immediately after the Command Address cycles ( 0 cycle latency)
3. The DQSM signal keep Hi-Z during register data-in cycles. DQSM will be ignored by host and device during entire register write operation.

**Figure 6.2 Register READ (Initial Latency = 1LC), No Refresh Collision at Variable Latency**



**Notes:**

1. The device drives DQSM "Low or High for Refresh indication" during command address cycles, which must be ignored by host. DQSM goes to "Low" after command address cycles until DQSM pre-cycle.
2. Initial Latency is 1LC for Register Read operation when DQSM is Low during command & address cycle. Refresh Indication. Initial Latency is always 2LC for Register Read operation when fixed initial latency is selected by configuration register.
3. DQSM is a read data strobe with register values edge aligned with the transitions of DQSM driven by the device.

## 6.2 CONFIGURATION REGISTER

The Configuration Register is able to change the defaulted status of the device. The device will be configured after the CR bit is set.

**Table 6.1 Configuration Register**

| Bit   | Function                    | Settings (Binary)                                                                                    |
|-------|-----------------------------|------------------------------------------------------------------------------------------------------|
| 15    | Deep Power Down Enable      | 1- Normal operation (default)<br>0- Writing 0 to CR [15] causes the device to enter Deep Power Down. |
| 14-12 | ODS (Output Drive Strength) | Refer to " <a href="#">Table 6.2. Output Driver Strength Table</a> "                                 |
| 11-9  | Reserved                    | Set to 000b                                                                                          |
| 8     | DQSM READ Pre-cycle         | 1 - 1 clock<br>0 - 0 clock (default)                                                                 |
| 7-4   | Latency counter             | Refer to " <a href="#">Table 6.3. Latency counter Table</a> "                                        |
| 3     | Initial Access Latency      | 0 - Variable Latency (default)<br>1 - Fixed Latency                                                  |
| 2     | Reserved                    | Set to 0b                                                                                            |
| 1-0   | Burst Length                | 00- 128 bytes<br>01- 64 bytes<br>10- 32 bytes (default)<br>11- 16 bytes                              |

**Table 6.2 Output Driver Strength Table**

| ODS2 | ODS1 | ODS0 | Description       |
|------|------|------|-------------------|
| 0    | 0    | 0    | 146 Ohms          |
| 0    | 0    | 1    | 76 Ohms           |
| 0    | 1    | 0    | 52 Ohms           |
| 0    | 1    | 1    | 41 Ohms           |
| 1    | 0    | 0    | 34 Ohms           |
| 1    | 0    | 1    | 30 Ohms           |
| 1    | 1    | 0    | 26 Ohms           |
| 1    | 1    | 1    | 24 Ohms (Default) |

**Table 6.3 Latency counter Table**

| CR[7:4]   | Latency Counter           |
|-----------|---------------------------|
| 0000      | 3 clocks                  |
| 0001      | 4 clocks                  |
| 0010      | 5 clocks (default at 3V)  |
| 0011      | 6 clocks                  |
| 0100      | 7 clocks                  |
| 0101      | 8 clocks(default at 1.8V) |
| 0110~1111 | Reserved                  |

### 6.2.1 WRAPPED BURST LENGTH

**Table 6.4 Wrapped Burst Sequences**

| Command | Configuration Register[1:0] | Burst Type | Wrap Boundary Col. Addr | Start Address (Hex) | Address Sequence (Hex) : Bytes                                  |
|---------|-----------------------------|------------|-------------------------|---------------------|-----------------------------------------------------------------|
| Read    | 00                          | Wrap 128   | CA[6:0]                 | XXXXXX06            | 07. 06, 09, 08,.... 7F, 7E, 01, 00, 03, 02, 05, 04, 07, 06, ... |
| Write   | 00                          | Wrap 128   | CA[6:0]                 | XXXXXX06            | 07. 06, 09, 08,.... 7F, 7E, 01, 00, 03, 02, 05, 04, 07, 06, ... |
| Read    | 01                          | Wrap 64    | CA[5:0]                 | XXXXXX02            | 03. 02, 05, 04, 07, 06,.... 3D, 3C, 3F, 3E, 01, 00, 03, 02, ... |
| Write   | 01                          | Wrap 64    | CA[5:0]                 | XXXXXX02            | 03. 02, 05, 04, 07, 06,.... 3D, 3C, 3F, 3E, 01, 00, 03, 02, ... |
| Read    | 10                          | Wrap 32    | CA[4:0]                 | XXXXXX1A            | 1B. 1A, 1D, 1C, 1F, 1E,.... 17, 16, 19, 18, 1B, 1A, 1C, 1B, ... |
| Write   | 10                          | Wrap 32    | CA[4:0]                 | XXXXXX1A            | 1B. 1A, 1D, 1C, 1F, 1E,.... 17, 16, 19, 18, 1B, 1A, 1C, 1B, ... |
| Read    | 11                          | Wrap 16    | CA[3:0]                 | XXXXXX0A            | 0B. 0A, 0D, 0C, 0F, 0E, 01, 00,.... 07, 06, 09, 08, 0B, 0A, ... |
| Write   | 11                          | Wrap 16    | CA[3:0]                 | XXXXXX0A            | 0B. 0A, 0D, 0C, 0F, 0E, 01, 00,.... 07, 06, 09, 08, 0B, 0A, ... |
| Read    | XX                          | Continuous | X                       | XXXXXX0C            | 0D, 0C, 0F, 0E, 11, 10, 13, 12, 15, 14, 17, 16, 19. 18, ...     |
| Write   | XX                          | Continuous | X                       | XXXXXX0C            | 0D, 0C, 0F, 0E, 11, 10, 13, 12, 15, 14, 17, 16, 19. 18, ...     |

**Notes:** When Continuous burst type is operated on burst operations, Memory access address will increase continuously regardless of Burst Wrap Length code.

### 6.2.2 INITIAL LATENCY (CR [3])

Initial Latency for Variable Latency setting (CR [3]=0) is LC or 2LC , based on Refresh Collision like below table. So host chipset must monitor DQSM signal, which indicates Refresh Collision occurrence or not. But Initial Latency for Fixed Latency setting (CR [3] = 1) is always 2LC.

**Table 6.5 Variable Latency (CR[3] = 0)**

| Latency code<br>CR[7:4] | Initial Latency Counter          |                         | Maximum Operating Frequency |               |
|-------------------------|----------------------------------|-------------------------|-----------------------------|---------------|
|                         | No Refresh Collision (LC)        | Refresh Collision (2LC) | 1.8V                        | 3.0V          |
| 0000                    | 3 clocks                         | 6 clocks                | 83Mhz                       | 83Mhz         |
| 0001                    | 4 clocks                         | 8 clocks                | 100Mhz                      | 100Mhz        |
| <b>0010</b>             | <b>5 clocks (default at 3V)</b>  | <b>10 clocks</b>        | 166Mhz                      | <b>133Mhz</b> |
| 0011                    | 6 clocks                         | 12 clocks               | 166MHz                      | 166MHz        |
| 0100                    | 7 clocks                         | 14 clocks               | 200MHz                      | 200MHz        |
| <b>0101</b>             | <b>8 clocks(default at 1.8V)</b> | <b>16 clocks</b>        | <b>200Mhz</b>               | 200MHz        |
| 0100 - 1111             | Reserved                         | -                       | NA                          |               |

**Notes:** Default setting for 1.8V device is “0101”, and that for 3.0V device is “0010”.

**Table 6.6 Initial Latency Summary Table**

| Destination | Operating mode | Variable mode (default)<br>initial Latency Count |                          | Fixed mode<br>Initial Latency Count |
|-------------|----------------|--------------------------------------------------|--------------------------|-------------------------------------|
|             |                | No Refresh Collision                             | Refresh Collision        |                                     |
| Memory      | READ           | 1LC                                              | 2LC                      | 2LC                                 |
|             | WRITE          | 1LC                                              | <b>2LC<sup>(2)</sup></b> | <b>2LC<sup>(2)</sup></b>            |
| Register    | READ           | 1LC                                              | <b>2LC<sup>(2)</sup></b> | <b>2LC<sup>(2)</sup></b>            |
|             | WRITE          | 0LC                                              |                          | 0LC                                 |

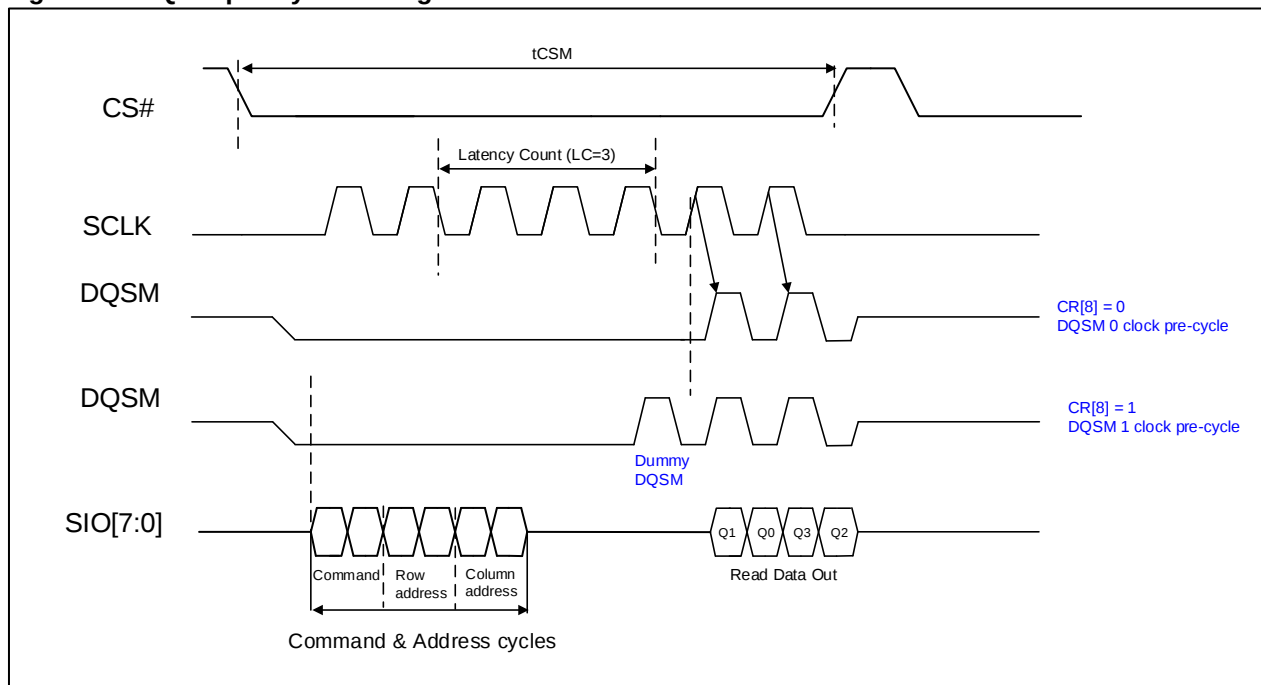
**Notes:**

1. LC means Latency Counter clocks, which is in Configuration Register Bit [7:4], as defined in ["Table 6.1"](#) and ["Table 6.3"](#).
2. Contact ISSI MKT if 1LC is required instead of 2LC.

### 6.2.3 DQSM READ Pre-Cycle (CR [8])

CR [8] defines DQSM Pre-Cycle.

Figure 6.3 DQSM pre-cycle during Burst READ



**Notes:**

1. Latency count (LC) is 3 clocks.
2. When Configuration Register bit8 = 0, the Device will output DQSM with valid data cycle.
3. When Configuration Register bit8 = 1, the Device will output **dummy DQSM** one clock cycle period prior to valid data cycle.
4. The memory drives DQSM during read cycles.

## 6.2.4 Deep Power Down (CR [15])

Figure 6.4 Deep Power Down Entry Timing

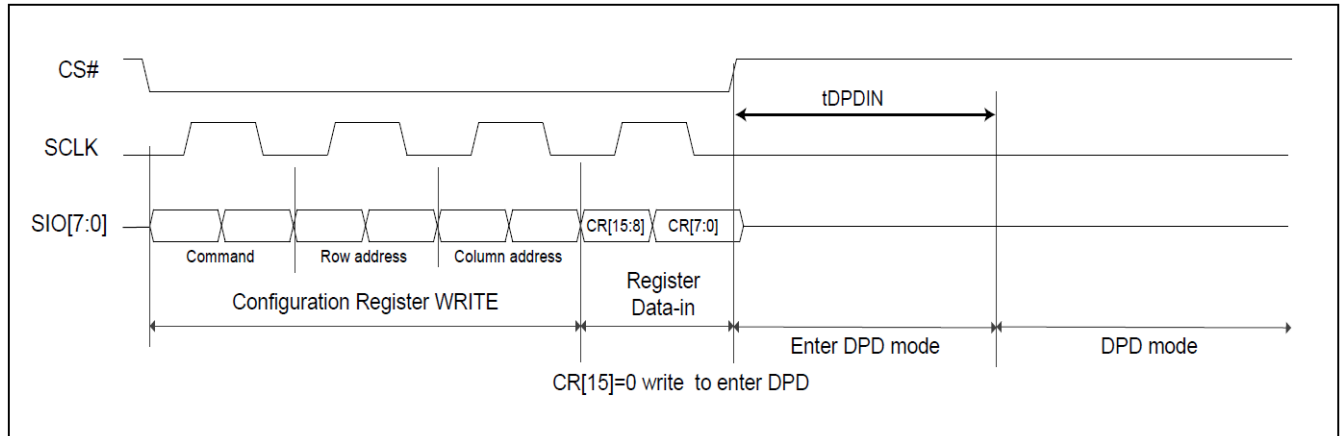
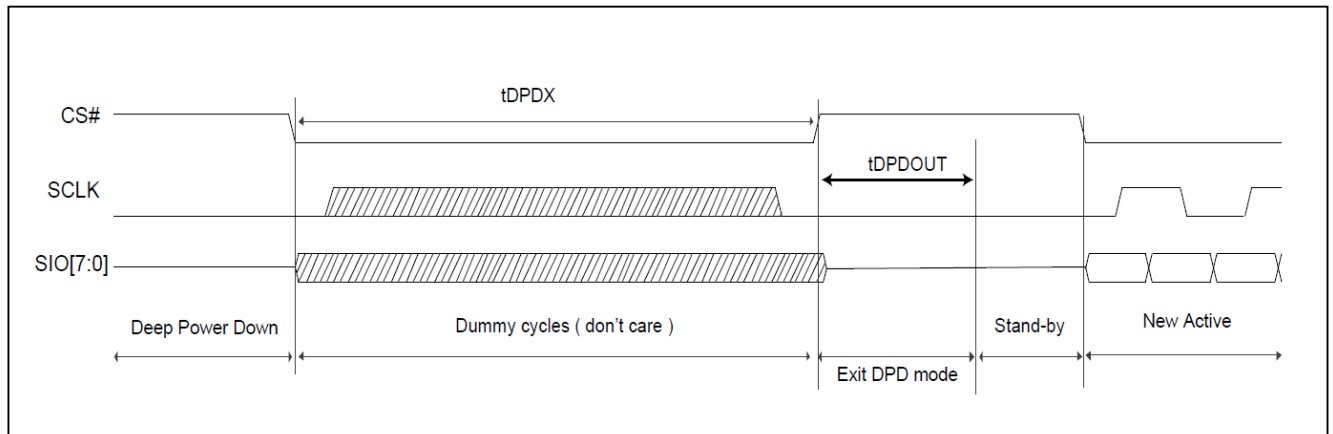


Figure 6.4 Deep Power Down Exit Timing



**Notes:** Memory Cell Data cannot be retained at deep power down(DPD) mode.

Table 6.7 Deep Power Down Timing Parameters

| Parameter | Description                                                | Min | Max | Unit |
|-----------|------------------------------------------------------------|-----|-----|------|
| tDPDIN    | Deep Power Down CR[15]=0 register write to DPD power level | 150 | -   | us   |
| tDPDX     | CS# Low period to exit from Deep Power Down                | 200 | -   | ns   |
| tDPDOUT   | CS# Low then High to Standby wakeup time                   | -   | 150 | us   |

### 6.3 DEVICE IDENTIFICATION REGISTER

It is a read only, non-volatile, word register that provides device information. The device information fields can be identified as below.

- a. Device Type
- b. Density
  - i. Row address bit count
  - ii. Column address bit count
- c. Manufacturer

**Table 6.8 ID Register**

| Bits    | Function                 | Settings (Binary)                                                                                |
|---------|--------------------------|--------------------------------------------------------------------------------------------------|
| 15 - 13 | Device Voltage           | 000: 1.8V<br>001: 3V                                                                             |
| 12 - 8  | Row address bit count    | 00000 : 1 row address<br>.....<br>01110 : 15 row address<br>.....<br>11111 : 32 row address      |
| 7 - 4   | Column address bit count | 0000 : 1 column address<br>.....<br>1001: 10 column address<br>.....<br>1111 : 16 column address |
| 3 - 0   | Manufacturer             | 0011 (ISSI)                                                                                      |

## 7. ELECTRICAL CHARACTERISTICS

### 7.1 ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                   |                                 |
|-------------------------------------------------------------------|---------------------------------|
| Storage Temperature                                               | -65°C to +150°C                 |
| Input Voltage with Respect to Ground on All Pins                  | -0.5V to V <sub>CC</sub> + 0.5V |
| All Output Voltage with Respect to Ground                         | -0.5V to V <sub>CC</sub> + 0.5V |
| V <sub>CC</sub>                                                   | -0.5V to +4.0V                  |
| Electrostatic Discharge Voltage (Human Body Model) <sup>(2)</sup> | -2000V to +2000V                |

**Notes:**

1. Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. ANSI/ESDA/JEDEC JS-001

### 7.2 OPERATING RANGE

|                              |                     |                                                                  |
|------------------------------|---------------------|------------------------------------------------------------------|
| Operating Temperature        | Industrial Grade    | -40°C to 85°C                                                    |
|                              | Automotive Grade A1 | -40°C to 85°C                                                    |
|                              | Automotive Grade A2 | -40°C to 105°C                                                   |
| V <sub>CC</sub> Power Supply | IS66/67WVO32M8DALL  | 1.70V (V <sub>MIN</sub> ) –1.95V (V <sub>MAX</sub> ); 1.8V (Typ) |
|                              | IS66/67WVO32M8DBLL  | 2.7V (V <sub>MIN</sub> ) –3.6V (V <sub>MAX</sub> ); 3.0V (Typ)   |

**7.3 DC CHARACTERISTICS**

| Symbol         | Parameter                                                       | Min.           | Typ. | Max.           | Units   | Test Conditions                                                     |
|----------------|-----------------------------------------------------------------|----------------|------|----------------|---------|---------------------------------------------------------------------|
| $I_{LI}$       | Input Leakage Current<br>3V Device Reset Signal Only            | -              | -    | $\pm 10.0$     | $\mu A$ | $V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$<br>max            |
| $I_{LI}$       | Input Leakage Current<br>1.8V Device Reset Signal Only          | -              | -    | $\pm 5.0$      | $\mu A$ | $V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC}$<br>max            |
| $I_{CC1}$      | VCC Active Read Current                                         | -              | 25   | 30             | mA      | CS# = $V_{IL}$ , @200MHz, $V_{CC} = 1.9V$                           |
|                |                                                                 |                | 25   | 30             |         | CS# = $V_{IL}$ , @166MHz, $V_{CC} = 3.6V$                           |
| $I_{CC2}$      | VCC Active Write Current                                        | -              | 20   | 25             | mA      | CS# = $V_{IL}$ , @200MHz, $V_{CC} = 1.9V$                           |
|                |                                                                 |                | 20   | 25             |         | CS# = $V_{IL}$ , @166MHz, $V_{CC} = 3.6V$                           |
| $I_{CC4I}$     | VCC Standby Current for<br>Industrial (-40°C to +85°C)          | -              | 750  | 800            | $\mu A$ | CS#, $V_{CC} = V_{CC}$ max                                          |
| $I_{CC4IP}$    | VCC Standby Current for<br>Extended (-40°C to +105°C)           | -              | 750  | 1200           |         |                                                                     |
| $I_{CC5}$      | Reset Current                                                   | -              | 5    | 10             | mA      | CS# = $V_{IH}$ , RESET# = $V_{SS} \pm 0.3V$ , $V_{CC} = V_{CC}$ max |
| $I_{CC6I}$     | Active Clock Stop Current for<br>Industrial (-40°C to +85°C)    | -              | 5    | 10             | mA      | CS# = $V_{IL}$ , RESET# = $V_{CC} \pm 0.3V$ , $V_{CC} = V_{CC}$ max |
| $I_{CC6IP}$    | Active Clock Stop Current for<br>Extended (-40°C to +105°C)     | -              | 5    | 10             |         |                                                                     |
| $I_{CC7}$      | VCC Current during power up                                     | -              | -    | 40             | mA      | CS#, $V_{CC} = V_{CC}$ max, $V_{CC} = V_{CCQ} = 1.95V$ or 3.6V      |
| $I_{DPDI}$     | Deep Power Down Current 3V for<br>Industrial (-40°C to +85°C)   | -              | -    | 30             | $\mu A$ | CS#, $V_{CC} = 3.6V$                                                |
|                | Deep Power Down Current 1.8V for<br>Industrial (-40°C to +85°C) | -              | -    | 20             |         | CS#, $V_{CC} = 1.9V$                                                |
| $I_{DPDIP}$    | Deep Power Down Current 3V for<br>Extended (-40°C to +105°C)    | -              | -    | 50             | $\mu A$ | CS#, $V_{CC} = 3.6V$                                                |
|                | Deep Power Down Current 1.8V for<br>Extended (-40°C to +105°C)  | -              | -    | 30             |         | CS#, $V_{CC} = 1.9V$                                                |
| $V_{IL}^{(1)}$ | Input Low Voltage                                               | -0.5           | -    | $0.3V_{CC}$    | V       |                                                                     |
| $V_{IH}^{(1)}$ | Input High Voltage                                              | $0.7V_{CC}$    | -    | $V_{CC} + 0.3$ | V       |                                                                     |
| $V_{OL}$       | Output Low Voltage                                              |                | -    | 0.2            | V       | $I_{OL} = 100 \mu A$                                                |
| $V_{OH}$       | Output High Voltage                                             | $V_{CC} - 0.2$ | -    |                | V       | $I_{OH} = -100 \mu A$                                               |

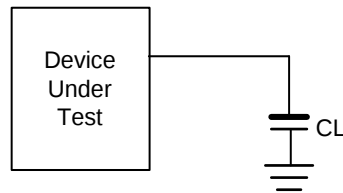
**Notes:**

- Maximum DC voltage on input or I/O pins is  $V_{CC} + 0.5V$ . During voltage transitions, input or I/O pins may overshoot  $V_{CC}$  by +2.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0V for a period of time not to exceed 20ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}$  (Typ).

## 7.4 AC MEASUREMENT CONDITIONS

| Symbol | Parameter                        | Min                    | Max | Units |
|--------|----------------------------------|------------------------|-----|-------|
| CL     | Output Load Capacitance          |                        | 20  | pF    |
| TR,TF  | Input Rise and Fall Times        | 2                      |     | V/ns  |
| VIN    | Input Pulse Voltages             | 0V to V <sub>CCQ</sub> |     | V     |
| VREFI  | Input Timing Reference Voltages  | V <sub>CCQ</sub> /2    |     | V     |
| VREFO  | Output Timing Reference Voltages | V <sub>CCQ</sub> /2    |     | V     |

Figure 7.1 Test Setup



## 7.5 PIN CAPACITANCE (TA = 25°C, VCC=1.8V/ 3V, 1MHZ)

| Symbol              | Parameter                            | Test Condition           | Min | Typ | Max | Units |
|---------------------|--------------------------------------|--------------------------|-----|-----|-----|-------|
| C <sub>IN</sub>     | Input Capacitance (CS#, SCLK)        | V <sub>IN</sub> = 0V     | 3   | -   | 4.5 | pF    |
| C <sub>IN/OUT</sub> | Input/Output Capacitance (SIO, DQSM) | V <sub>IN/OUT</sub> = 0V | 3   | -   | 4.0 | pF    |

**Note:**

1. These parameters are characterized and not 100% tested.

## 7.6 AC CHARACTERISTICS

### 7.6.1 Read Timing Parameters (1.8V)

| Symbol | Parameter                                | 200MHz       |      | 166MHz       |      | Unit  |
|--------|------------------------------------------|--------------|------|--------------|------|-------|
|        |                                          | Min.         | Max. | Min.         | Max. |       |
| LC     | Latency Counter ( No Refresh Collision)  | 7            | -    | 5            | -    | clock |
| tRWR   | Read-Write Recovery Time                 | 35           | -    | 30           | -    | ns    |
| tCK    | Clock(CLK) Period                        | 5            | -    | 6            | -    | ns    |
| tCH    | Clock High level width                   | 0.45         | -    | 0.45         | -    | tCKmi |
| tCL    | Clock Low level width                    | 0.45         | -    | 0.45         | -    | tCKmi |
| tHP    | Clock half period                        | Min(tCH,tCL) | -    | Min(tCH,tCL) | -    | ns    |
| tDQSV  | CS# Active to DQSM valid                 | -            | 12   | -            | 12   | ns    |
| tAC    | Clock transition to DQ valid             | 0.9          | 5    | 1            | 5.5  | ns    |
| tDQSCK | Clock transition to DQSM valid           | 0.9          | 5    | 1            | 5.5  | ns    |
| tCSP   | CS# High Between READ/WRITE              | 6            | -    | 6            | -    | ns    |
| tCSS   | CS# Setup to next CLK Rising Edge        | 3            | -    | 3            | -    | ns    |
| tCSH   | CS# Hold After CLK Falling Edge          | 2            | -    | 2            | -    | ns    |
| tIS    | Input Setup                              | 0.5          | -    | 0.6          | -    | ns    |
| tIH    | Input Hold                               | 0.5          | -    | 0.6          | -    | ns    |
| tDQSQ  | DQSM-DQ Skew                             | -            | 0.4  | -            | 0.45 | ns    |
| tQHS   | Data Hold Skew factor                    | -            | 0.8  | -            | 0.85 | ns    |
| tQH    | DQ hold time from DQSM                   | tHP-tQHS     | -    | tHP-tQHS     | -    | ns    |
| tLZ    | Clock to DQ Low-Z                        | 0            | -    | 0            | -    | ns    |
| tHZ    | CS# Inactive to DQSM and DQ High-Z       | -            | 5    | -            | 6    | ns    |
| tCSM   | Chip Select Maximum Low Time ( ~ 85°C )  | -            | 4.0  | -            | 4.0  | us    |
| tCSM   | Chip Select Maximum Low Time ( ~ 105°C ) | -            | 1.0  | -            | 1.0  | us    |

### 7.6.2 Read Timing Parameters (3.0V)

| Symbol | Parameter                                | 200MHz       |      | 166MHz       |      | Unit   |
|--------|------------------------------------------|--------------|------|--------------|------|--------|
|        |                                          | Min.         | Max. | Min.         | Max. |        |
| LC     | Latency Counter ( No Refresh Collision)  | 7            | -    | 6            | -    | clock  |
| tRWR   | Read-Write Recovery Time                 | 35           | -    | 36           | -    | ns     |
| tCK    | Clock(CLK) Period                        | 5            | -    | 6            | -    | ns     |
| tCH    | Clock High level width                   | 0.45         | -    | 0.45         | -    | tCKmin |
| tCL    | Clock Low level width                    | 0.45         | -    | 0.45         | -    | tCKmin |
| tHP    | Clock half period                        | Min(tCH,tCL) | -    | Min(tCH,tCL) | -    | ns     |
| tDQSV  | CS# Active to DQSM valid                 | -            | 12   | -            | 12   | ns     |
| tAC    | Clock transition to DQ valid             | 0.9          | 6.0  | 1            | 6.5  | ns     |
| tDQSC  | Clock transition to DQSM valid           | 0.9          | 6.0  | 1            | 6.5  | ns     |
| tCSP   | CS# High Between READ/WRITE              | 6            | -    | 6            | -    | ns     |
| tCSS   | CS# Setup to next CLK Rising Edge        | 3            | -    | 3            | -    | ns     |
| tCSH   | CS# Hold After CLK Falling Edge          | 2            | -    | 2            | -    | ns     |
| tIS    | Input Setup                              | 0.5          | -    | 0.6          | -    | ns     |
| tIH    | Input Hold                               | 0.5          | -    | 0.6          | -    | ns     |
| tDQSQ  | DQSM-DQ Skew                             | -            | 0.4  | -            | 0.7  | ns     |
| tQHS   | Data Hold Skew factor                    | -            | 0.8  | -            | 0.85 | ns     |
| tQH    | DQ hold time from DQSM                   | tHP-tQHS     | -    | tHP-tQHS     | -    | ns     |
| tLZ    | Clock to DQ Low-Z                        | 0            | -    | 0            | -    | ns     |
| tHZ    | CS# Inactive to DQSM and DQ High-Z       | -            | 5    | -            | 6    | ns     |
| tCSM   | Chip Select Maximum Low Time ( ~ 85°C )  | -            | 4.0  | -            | 4.0  | us     |
| tCSM   | Chip Select Maximum Low Time ( ~ 105°C ) | -            | 1.0  | -            | 1.0  | us     |

**7.6.3 WRITE Timing Parameters (1.8V)**

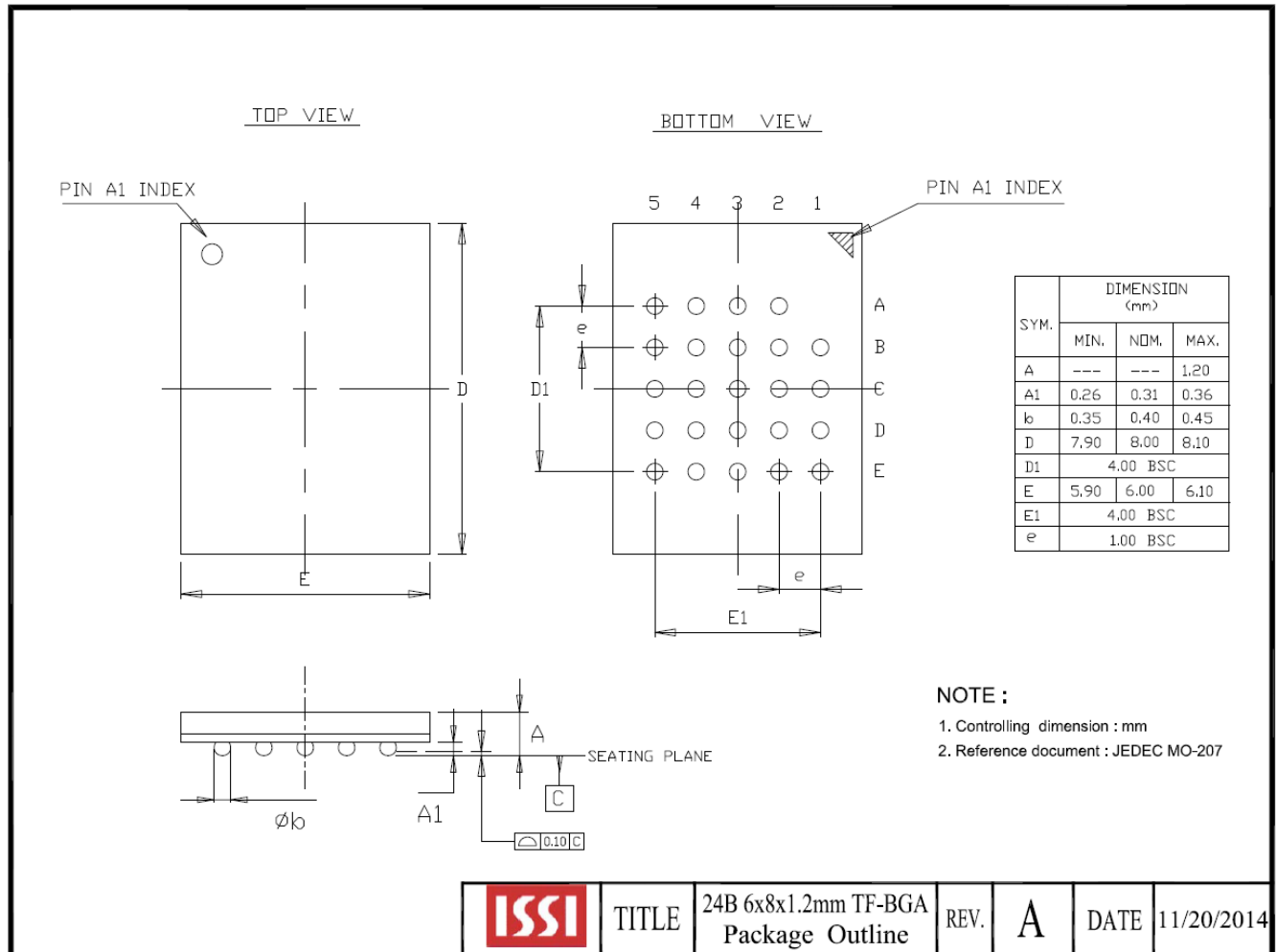
| Symbol | Parameter                                                 | 200MHz       |      | 166MHz       |      | Unit   |
|--------|-----------------------------------------------------------|--------------|------|--------------|------|--------|
|        |                                                           | Min.         | Max. | Min.         | Max. |        |
| LC     | Latency Counter ( No Refresh Collision)                   | 7            | -    | 5            | -    | clock  |
| tRWR   | Read-Write Recovery Time                                  | 35           | -    | 30           | -    | ns     |
| tCK    | Clock(CLK) Period                                         | 5            | -    | 6            | -    | ns     |
| tCH    | Clock High level width                                    | 0.45         | -    | 0.45         | -    | tCKmin |
| tCL    | Clock Low level width                                     | 0.45         | -    | 0.45         | -    | tCKmin |
| tHP    | Clock half period                                         | Min(tCH,tCL) | -    | Min(tCH,tCL) | -    | ns     |
| tDQSV  | CS# Active to DQSM valid                                  | -            | 12   | -            | 12   | ns     |
| tDQSC  | Clock transition to DQSM valid                            | 0.9          | 5    | 1            | 5.5  | ns     |
| tCSP   | CS# High Between READ/WRITE                               | 6            | -    | 6            | -    | ns     |
| tCSS   | CS# Setup to next CLK Rising Edge                         | 3            | -    | 3            | -    | ns     |
| tCSH   | CS# Hold After CLK Falling Edge                           | 2            | -    | 2            | -    | ns     |
| tIS    | Input Setup                                               | 0.5          | -    | 0.6          | -    | ns     |
| tIH    | Input Hold                                                | 0.5          | -    | 0.6          | -    | ns     |
| tDMV   | Data Mask Valid<br>(DQSM setup to end of initial latency) | 0            | -    | 0            | -    | ns     |
| tCSM   | Chip Select Maximum Low Time ( ~ 85°C )                   | -            | 4.0  | -            | 4.0  | us     |
| tCSM   | Chip Select Maximum Low Time ( ~ 105°C )                  | -            | 1.0  | -            | 1.0  | us     |

**7.6.4 WRITE Timing Parameters (3.0V)**

| Symbol | Parameter                                                 | 200MHz       |      | 166MHz       |      | Unit   |
|--------|-----------------------------------------------------------|--------------|------|--------------|------|--------|
|        |                                                           | Min.         | Max. | Min.         | Max. |        |
| LC     | Latency Counter ( No Refresh Collision)                   | 7            | -    | 6            | -    | clock  |
| tRWR   | Read-Write Recovery Time                                  | 35           | -    | 36           | -    | ns     |
| tCK    | Clock(CLK) Period                                         | 5            | -    | 6            | -    | ns     |
| tCH    | Clock High level width                                    | 0.45         | -    | 0.45         | -    | tCKmin |
| tCL    | Clock Low level width                                     | 0.45         | -    | 0.45         | -    | tCKmin |
| tHP    | Clock half period                                         | Min(tCH,tCL) | -    | Min(tCH,tCL) | -    | ns     |
| tDQSV  | CS# Active to DQSM valid                                  | -            | 12   | -            | 12   | ns     |
| tDQSC  | Clock transition to DQSM valid                            | 0.9          | 6.0  | 1            | 6.5  | ns     |
| tCSP   | CS# High Between READ/WRITE                               | 6            | -    | 6            | -    | ns     |
| tCSS   | CS# Setup to next CLK Rising Edge                         | 3            | -    | 3            | -    | ns     |
| tCSH   | CS# Hold After CLK Falling Edge                           | 2            | -    | 2            | -    | ns     |
| tIS    | Input Setup                                               | 0.5          | -    | 0.6          | -    | ns     |
| tIH    | Input Hold                                                | 0.5          | -    | 0.6          | -    | ns     |
| tDMV   | Data Mask Valid<br>(DQSM setup to end of initial latency) | 0            | -    | 0            | -    | ns     |
| tCSM   | Chip Select Maximum Low Time ( ~ 85°C )                   | -            | 4.0  | -            | 4.0  | us     |
| tCSM   | Chip Select Maximum Low Time ( ~ 125°C )                  | -            | 1.0  | -            | 1.0  | us     |

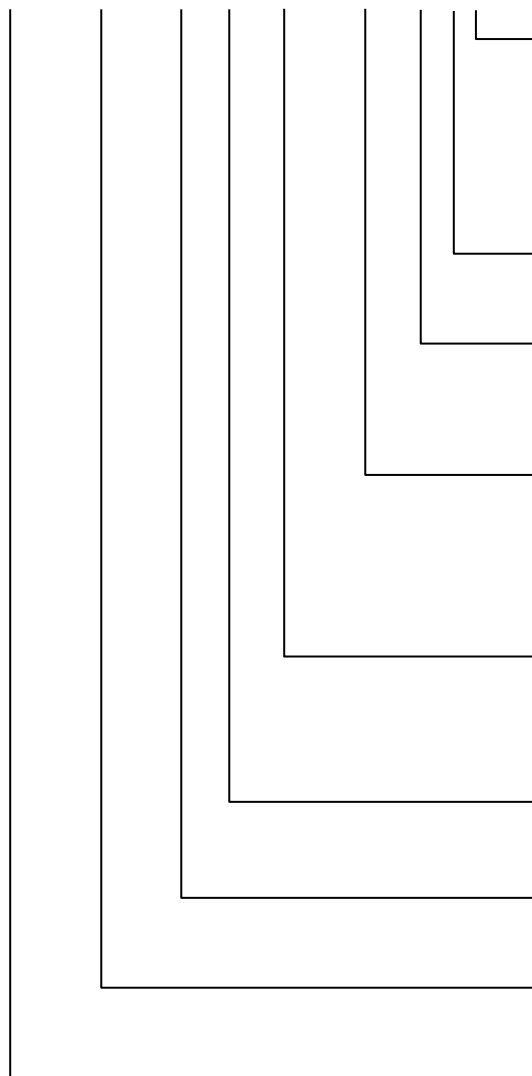
## 8. PACKAGE TYPE INFORMATION

### 8.1 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (B)



## 9. ORDERING INFORMATION – Valid Part Numbers

**IS66 WVO 32M8 D ALL - 200 B L I**



### TEMPERATURE RANGE

I = Extended (-40°C to +85°C)  
 A1 = Automotive Grade (-40°C to +85°C)  
 A2 = Automotive Grade (-40°C to +105°C)

### PACKAGING CONTENT

L = RoHS compliant

### PACKAGE Type <sup>(1)</sup>

B = 24-ball TFBGA 6x8mm 5x5 ball array  
 W = KGD (Call Factory)

### Maximum Frequency

200 = 200MHz  
 166 = 166MHz  
 133 = 133MHz

### VDD

ALL = 1.8V  
 BLL = 3.0V

### Die Revision

D = die rev D

### Density/Org.

32M8 = 32Mbx8=256Mb

### PSRAM Product Type.

WVO = OctalRAM

### BASE PART NUMBER

IS = Integrated Silicon Solution Inc.  
 66 = PSRAM  
 67 = PSRAM for Automotive

**Industrial Temperature Range (-40°C to +85°C)**

| Config. | Voltage | Max. Frequency (MHz) | Order Part Number <sup>(1)</sup> | Package                            |
|---------|---------|----------------------|----------------------------------|------------------------------------|
| 32Mbx8  | 1.8V    | 200                  | IS66WVO32M8DALL-200BLI           | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS66WVO32M8DALL-166BLI           | 24-ball TFBGA 6x8mm 5x5 ball array |
|         | 3.0V    | 200                  | IS66WVO32M8DBLL-200BLI           | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS66WVO32M8DBLL-166BLI           | 24-ball TFBGA 6x8mm 5x5 ball array |

**Automotive A1 Temperature Range (-40°C to +105°C)**

| Config. | Voltage | Max. Frequency (MHz) | Order Part Number <sup>(1)</sup> | Package                            |
|---------|---------|----------------------|----------------------------------|------------------------------------|
| 32Mbx8  | 1.8V    | 200                  | IS67WVO32M8DALL-200BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS67WVO32M8DALL-166BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         | 3.0V    | 200                  | IS67WVO32M8DBLL-200BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS67WVO32M8DBLL-166BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |

**Automotive A2 Temperature Range (-40°C to +105°C)**

| Config. | Voltage | Max. Frequency (MHz) | Order Part Number <sup>(1)</sup> | Package                            |
|---------|---------|----------------------|----------------------------------|------------------------------------|
| 32Mbx8  | 1.8V    | 200                  | IS67WVO32M8DALL-200BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS67WVO32M8DALL-166BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         | 3.0V    | 200                  | IS67WVO32M8DBLL-200BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |
|         |         | 166                  | IS67WVO32M8DBLL-166BLA2          | 24-ball TFBGA 6x8mm 5x5 ball array |