



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



SUPPLEMENT

FS512S-102 MHz DDR

512 Mb, 1.8 V Serial Peripheral Interface with Multi-I/O Flash

General Description

This supplementary document contains information for the FS512S-102 MHz DDR. Specifications contained in this supplement supersede those in the S25FS512S datasheet. The maximum DDR clock rate was increased from 80 MHz to 102 MHz. Refer to the latest S25FS512S datasheet for full electrical specifications.

Affected Documents/Related Documents

Title	Publication Number
S25FS512S, 512 Mbit, 1.8 V Serial Peripheral Interface with Multi-I/O Flash	002-00488

1. DDR AC Characteristics

Table 1. DDR AC Characteristics Operation

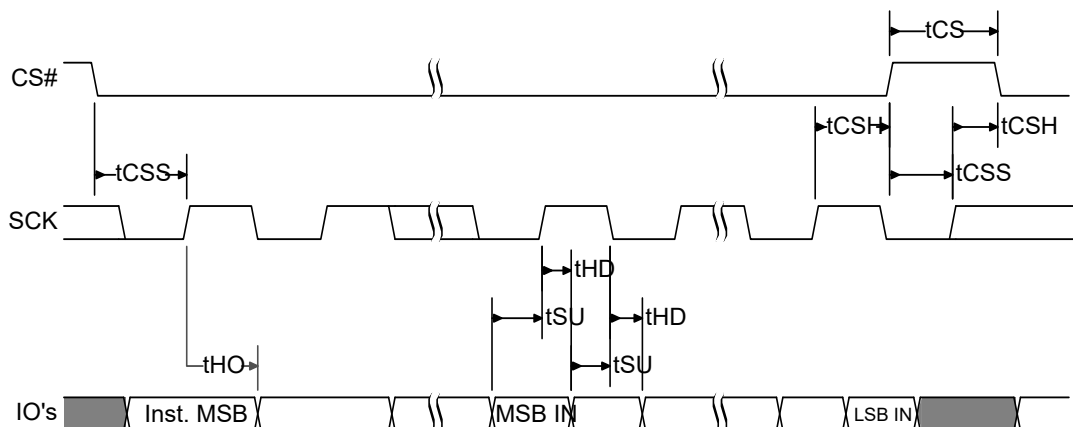
Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	–	102	MHz
$P_{SCK, R}$	SCK clock period for DDR READ instruction	$1/F_{SCK}$	–	∞	
t_{WH}, t_{CH}	Clock High time	$50\% P_{SCK} - 5\%$	–	$50\% P_{SCK} + 5\%$	ns
t_{WL}, t_{CL}	Clock Low time	$50\% P_{SCK} - 5\%$	–	$50\% P_{SCK} + 5\%$	
t_{CS}	CS# High time (Read instructions) CS# High time (Read instructions when Reset feature is enabled)	10 20	–	–	
t_{CSS}	CS# Active Setup time (Relative to SCK)	2	–	–	
t_{CSH}	CS# Active Hold time (Relative to SCK)	3	–	–	
t_{SU}	IO in Setup time	1.5	–	–	
t_{HD}	IO in Hold time	1.5	–	–	
t_V	Clock Low to Output valid	1.5	–	$5^{[1]}$	
t_{HO}	Output Hold time	1	–	–	
t_{DIS}	Output Disable time Output Disable time (When Reset feature is enabled)	–	–	8 20	
t_{IO_skew}	First IO to last IO data valid time	–	–	400	ps
t_{DPD}	CS# High to Power-down mode	–	–	3	μs
t_{RES}	CS# High to Standby mode without Electronic Signature Read	–	–	30	

Note

1. CL = 15 pF.

1.1 DDR Input Timing

Figure 1. SPI DDR Input Timing



1.2 DDR Output Timing

Figure 2. SPI DDR Output Timing

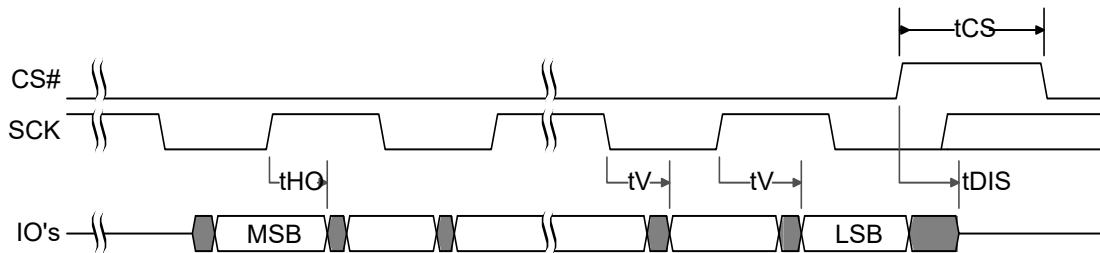
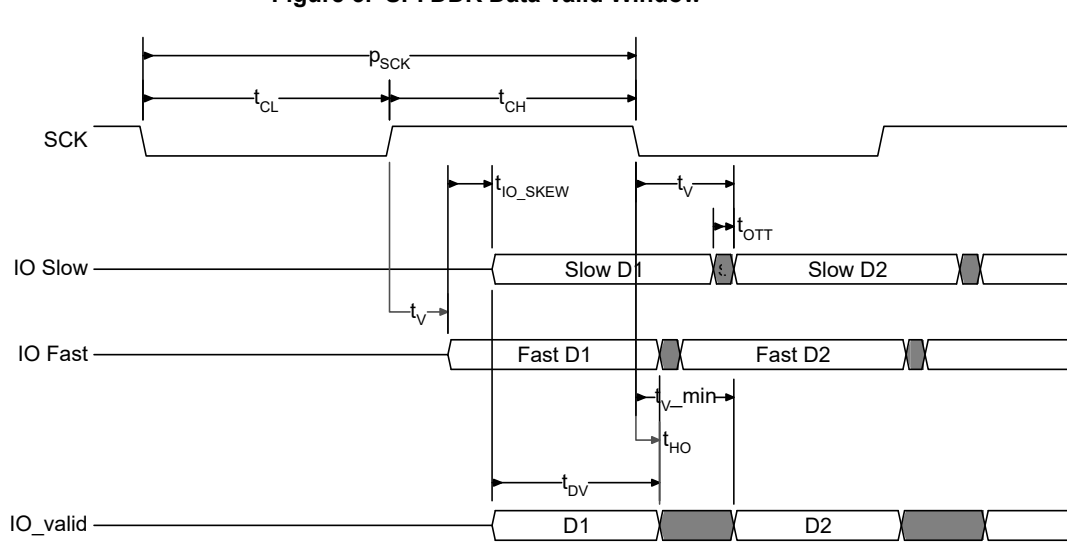


Figure 3. SPI DDR Data Valid Window^[2, 3, 4, 5]



The minimum data valid window (t_{DV}) can be calculated as follows:

As an example, assuming: 102 MHz clock frequency = 9.8 ns clock period with DDR operations are specified to have a duty cycle of 45% or higher.

■ $t_{CLH} = 0.45 \cdot p_{SCK} = 0.45 \times 9.8 \text{ ns} = 4.41 \text{ ns}$

■ $t_{IO_SKEW} = 400 \text{ ps}$

■ $t_{OTT} = 1.0 \text{ ns}$

■ $t_{DV} = t_{CLH} - t_{IO_SKEW} - t_{OTT}$

$t_{DV} = 4.41 \text{ ns} - 400 \text{ ps} - 1.0 \text{ ns} = 3.01 \text{ ns}$

■ $t_{V_min} = t_{HO} + t_{IO_SKEW} + t_{OTT}$

$t_{V_min} = 1.0 \text{ ns} + 400 \text{ ps} + 1.0 \text{ ns} = 2.4 \text{ ns}$

Notes

2. t_{CLH} is the shorter duration of t_{CL} or t_{CH} .
3. t_{IO_SKEW} is the maximum difference (Δ) between the minimum and maximum t_V (output valid) across all IO signals.
4. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO.
5. t_{OTT} is dependent on system level considerations including:
 - a. Memory device output impedance (drive strength).
 - b. System level parasitics on the IOs (primarily bus capacitance).
 - c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
 - d. As an example, assuming that the above considerations result in a memory output slew rate of 2 V/ns and a 3V transition (from 1 to 0 or 0 to 1) is required by the host, the t_{OTT} would be: $t_{OTT} = 2V / (2 \text{ V/ns}) = 1.0 \text{ ns}$.
 - e. t_{OTT} is not a specification tested by Cypress, it is system dependent and must be derived by the system designer based on the above considerations.

2. Latency Code

Table 2. Latency Code (Cycles) Versus Frequency^[6, 7]

Latency Cycles	Read Command Maximum Frequency (MHz)			
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	Dual I/O (1-2-2)	Quad I/O (1-4-4) QPI (4-4-4)	DDR Quad I/O (1-4-4) DDR QPI (4-4-4) ^[8]
	Mode Cycles = 0	Mode Cycles = 4	Mode Cycles = 2	Mode Cycles = 1
0	50	80	40	N/A
1	66	92	53	22
2	80	104	66	34
3	92	116	80	45
4	104	129	92	57
5	116	133	104	68
6	129	133	116	80
7	133	133	129	92
8	133	133	133	102
9	133	133	133	102
10	133	133	133	102
11	133	133	133	102
12	133	133	133	102
13	133	133	133	102
14	133	133	133	102
15	133	133	133	102

Notes

6. The Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI, command protocols include Continuous Read mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency.
7. Other read commands have fixed latency, e.g., Read always has zero read latency. RSFDP always has eight cycles of latency.
8. DDR QPI is only supported for Latency Cycles 1 through 7 and for clock frequency of up to 92 MHz.

3. DC Characteristics

Table 3. DC Characteristics (-40 °C to +85 °C range)

Symbol	Parameter	Test Conditions	Min	Typ ^[9]	Max	Unit
I _{CC1}	Active power supply current (READ) ^[10]	Quad DDR at 102 MHz	–	70	100	mA
I _{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	200	μA
I _{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	120	

Table 4. DC Characteristics (-40 °C to +105 °C range)

Symbol	Parameter	Test Conditions	Min	Typ ^[9]	Max	Unit
I _{CC1}	Active power supply current (READ) ^[10]	Quad DDR at 102 MHz	–	70	100	mA
I _{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	300	μA
I _{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	150	

Table 5. DC Characteristics (-40 °C to +125 °C range)

Symbol	Parameter	Test Conditions	Min	Typ ^[9]	Max	Unit
I _{CC1}	Active power supply current (READ) ^[10]	Quad DDR at 102 MHz	–	70	100	mA
I _{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	450	μA
I _{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	350	

Notes

9. Typical values are at TA = 25 °C and VCC = 1.8 V.

10. Outputs unconnected during read data return. Output switching current is not included.

4. Ordering Part Number

The ordering part number is formed by a valid combination of the following:

S25FS	512	S	FA	B	H	V	21	0	
									Packing Type 0 = Tray 3 = 13" Tape and Reel
									Model Number 21 = 5 × 5 ball BGA footprint, 256-KB Physical Sector
									Temperature Range V = Industrial Plus (-40 °C to + 105 °C) A = Automotive, AEC-Q100 Grade 3(-40 °C to + 85 °C) B = Automotive, AEC-Q100 Grade 2 (-40 °C to + 105 °C) M = Automotive, AEC-Q100 Grade 1(-40 °C to + 125 °C)
									Package Materials H = Low-Halogen, Lead (Pb)-free
									Package Type B = 24-ball BGA 6 × 8 mm package, 1.00 mm pitch
									Speed FA = 102 MHz DDR
									Device Technology S = 65-nm MirrorBit Process Technology
									Density 512 = 512 Mb
									Device Family S25FS Cypress Memory 1.8 V-only, Serial Peripheral Interface (SPI) Flash Memory

4.1 Valid Combinations — Standard

Valid combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 6. S25FS512S Valid Combinations: Standard

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
S25FS512S	FA	BHV	21	0, 3	FS512SFVH21

4.2 Valid Combinations — Automotive Grade / AEC-Q100

Table 7 lists the configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non-AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 7. S25FS512S Valid Combinations: Automotive Grade / AEC-Q100

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
S25FS512S	FA	BHB	21	0, 3	FS512SFBH21
S25FS512S	FA	BHA	21	0, 3	FS512SFAH21
S25FS512S	FA	BHM	21	0, 3	FS512SFMH21

Document History Page

Document Title: FS512S-102 MHz DDR, 512 Mb, 1.8 V Serial Peripheral Interface with Multi-I/O Flash Document Number: 002-11269			
Rev.	ECN No.	Submission Date	Description of Change
**	5153521	03/01/2016	Initial release
*A	5608199	02/07/2017	Max DDR clock rate changed from 100 MHz to 102 MHz. Updated Note 3 in Latency Code . Updated Ordering Part Number : Added support for Automotive, AEC-Q100 Grade 2 (–40°C to + 105°C). Added Valid Combinations — Standard . Added Valid Combinations — Automotive Grade / AEC-Q100 . Updated Sales and Copyright information.
*B	5944243	12/08/2017	Updated the Cypress logo. Changed datasheet status to Final. Updated t_V max value to 5. Updated Latency Code .
*C	6277137	08/10/2017	Updated Table 2 .
*D	7249502	08/25/2021	Added Temperature range and grades (A and M) in Ordering Part Number . Added Table 3 and Table 5 in DC Characteristics . Added OPNs in Table 7 .

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2016-2021. This document is the property of Cypress Semiconductor Corporation, an Infineon Technologies company, and its affiliates ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, including its affiliates, and its directors, officers, employees, agents, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement with Cypress, the Cypress logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, Traveo, WICED, and ModusToolbox are trademarks or registered trademarks of Cypress or a subsidiary of Cypress in the United States or in other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.