

MOSFET – N-Channel, UniFET™

500 V, 18 A, 265 mΩ

**FDP18N50 / FDPF18N50 /
FDPF18N50T**

Description

UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

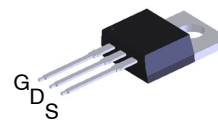
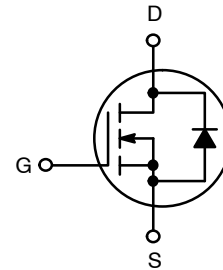
Features

- $R_{DS(on)} = 220 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 9 \text{ A}$
- Low Gate Charge (Typ. 45 nC)
- Low C_{rss} (Typ. 25 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

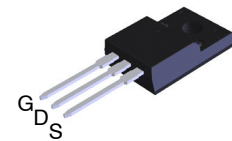
Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
500 V	265 mΩ @ 9 V	18 A

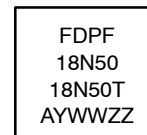
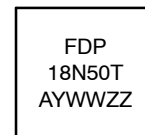


TO-220-3LD
CASE 340AT



TO-220 Fullpack, 3-Lead
/ TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



FDP18N50,
FDPF18N50
FDPF18N50T = Specific Device Code
A = Assembly Location
YWW = Date Code (Year and Week)
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping
FDP18N50	TO-220	1000 Units / Tube
FDPF18N50	TO-220F	1000 Units / Tube
FDPF18N50T	TO-220F	1000 Units / Tube

FDP18N50 / FDPF18N50 / FDPF18N50T

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
V_{DSS}	Drain to Source Voltage	500		V
I_D	Drain Current – – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	18 10.8	18* 10.8*	A
I_{DM}	Drain Current – Pulsed (Note 1)	72	72*	A
V_{GSS}	Gate to Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	945		mJ
I_{AR}	Avalanche Current (Note 1)	18		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	23.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) – Derate Above 25°C	235 1.88	38.5 0.3	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Second	300		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. $L = 5.2\text{ mH}$, $I_{AS} = 18\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

3. $I_{SD} \leq 18\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.53	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$, $I_D = 250\ \mu\text{A}$,	500	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	0.5	–	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	1	μA
		$V_{DS} = 400\text{ V}$, $T_C = 125^\circ\text{C}$	–	–	10	
I_{GSSF}	Gate–Body Leakage Current, Forward	$V_{GS} = 30\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate–Body Leakage Current, Reserve	$V_{GS} = -30\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	–100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$	–	0.220	0.265	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}$, $I_D = 9\text{ A}$	–	25	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	–	2200	2860	pF
C_{oss}	Output Capacitance		–	330	430	pF
C_{rss}	Reverse Transfer Capacitance		–	25	40	pF

FDP18N50 / FDPF18N50 / FDPF18N50T

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$ (Note 4)	–	55	120	ns
t_r	Turn-On Rise Time		–	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		–	95	200	ns
t_f	Turn-Off Fall Time		–	90	190	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	–	45	60	nC
Q_{gs}	Gate-Source Charge		–	12.5	–	nC
Q_{gd}	Gate-Drain Charge		–	19	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current		–	–	18	A
I_{SM}	Maximum Pulsed Drain- Source Diode Forward Current		–	–	72	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 18\text{ A}$	–	–	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 18\text{ A}$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	–	500	–	ns
Q_{rr}	Reverse Recovery Charge		–	5.4	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics



TYPICAL PERFORMANCE CHARACTERISTICS

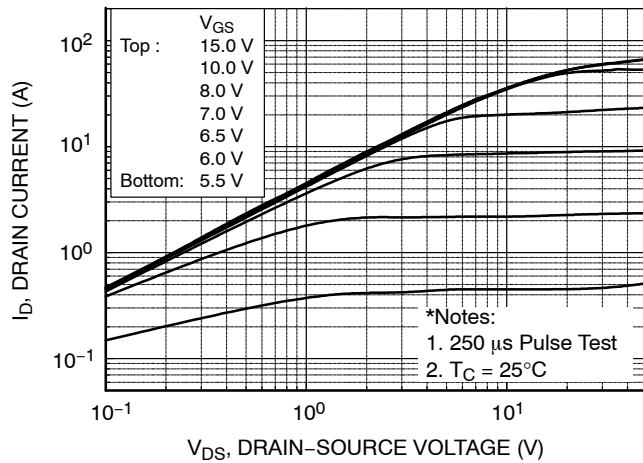


Figure 1. On-Resistance Characteristics

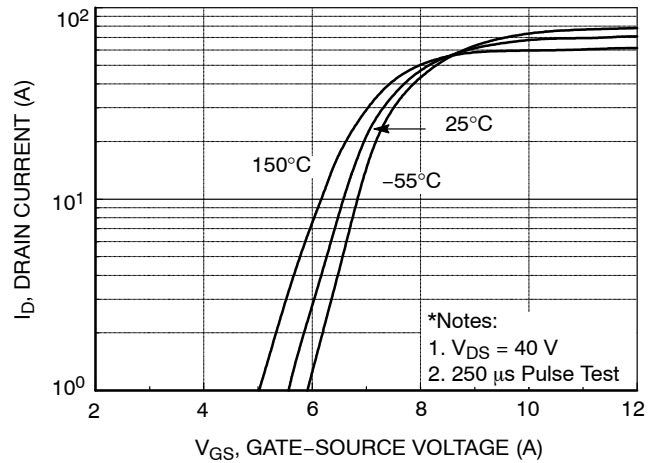


Figure 2. Transfer Characteristics

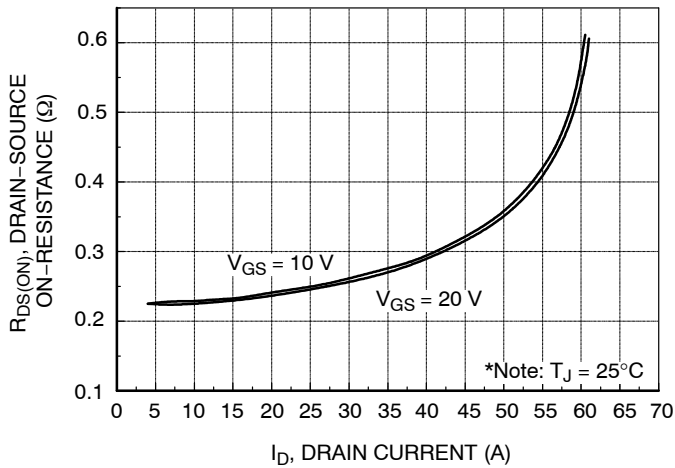


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

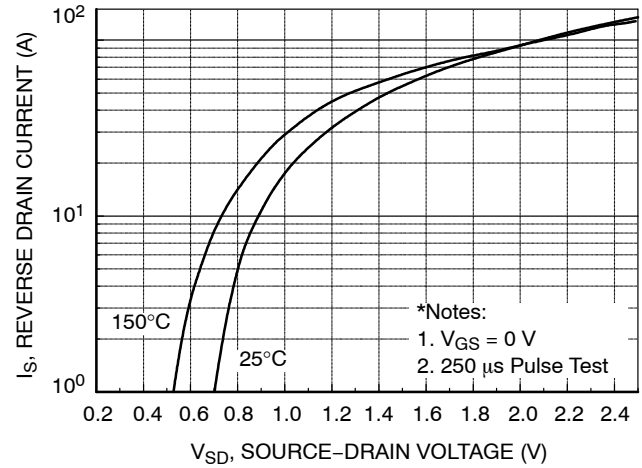


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

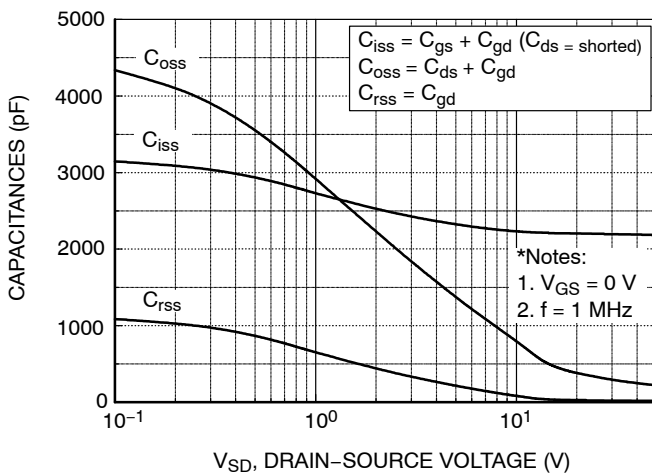


Figure 5. Capacitance Characteristics

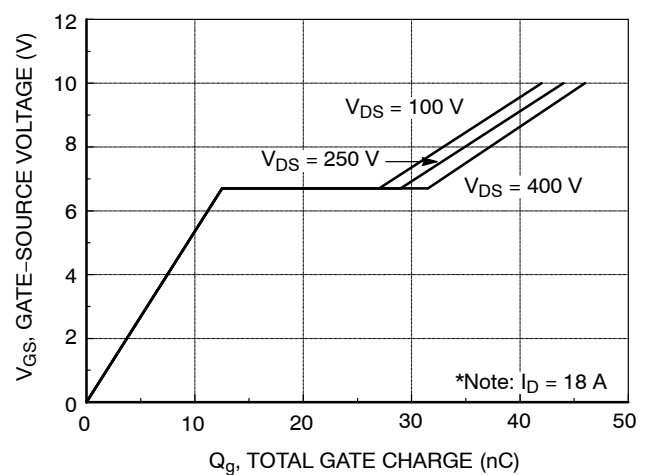


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

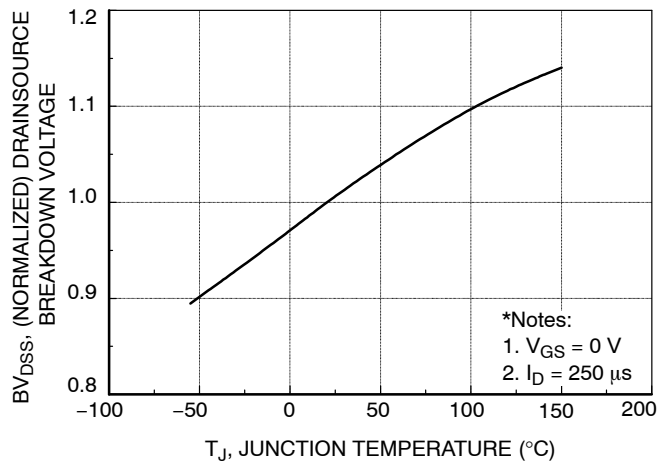


Figure 7. Breakdown Voltage Variation vs. Temperature

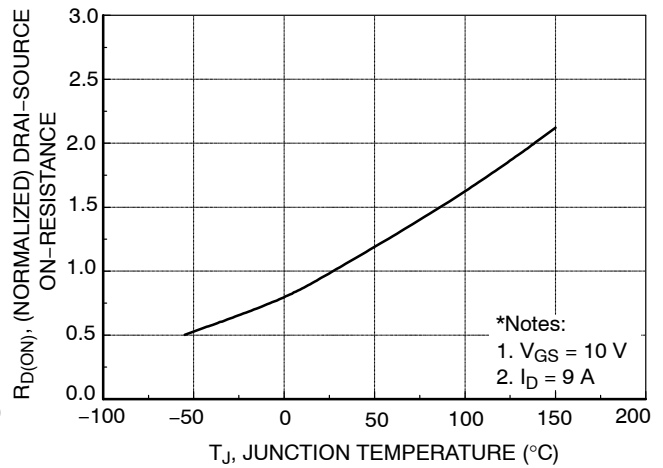


Figure 8. On-Resistance Variation vs. Temperature

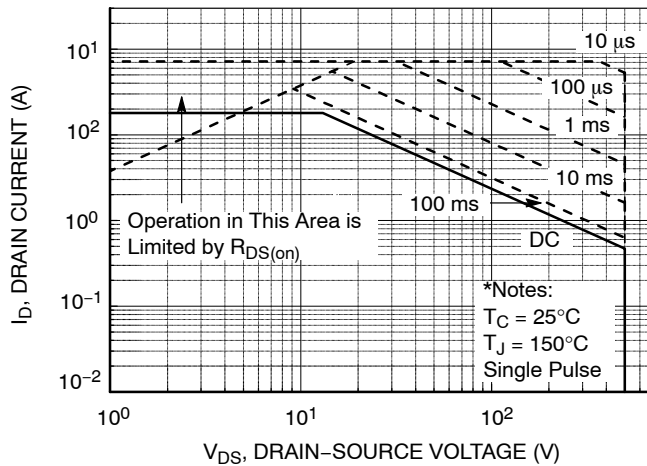


Figure 9-1. Maximum Safe Operating Area for FDP18N50

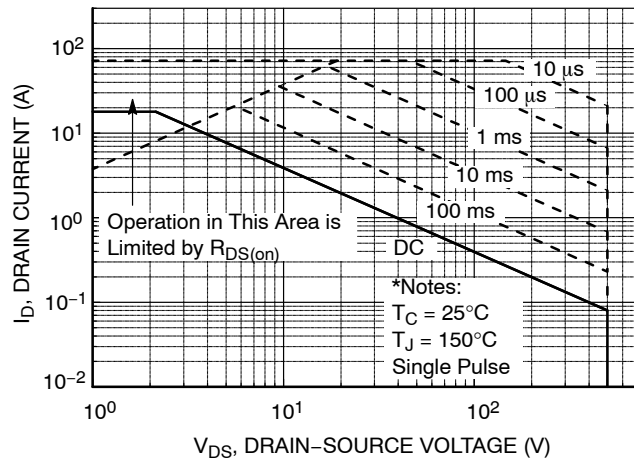


Figure 9-2. Maximum Safe Operating Area for FDPF18N50 / FDPF18N50T

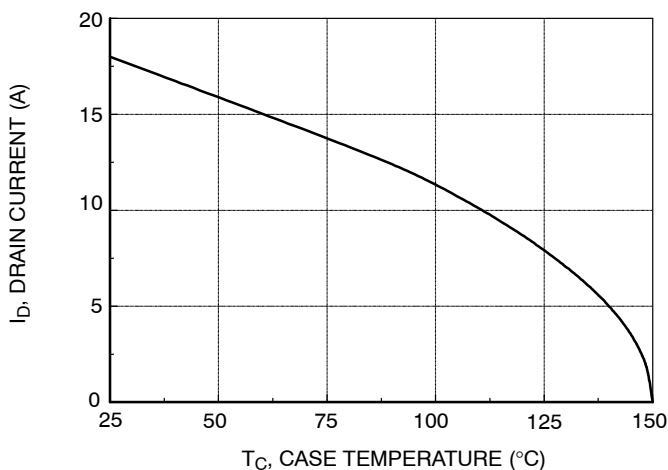
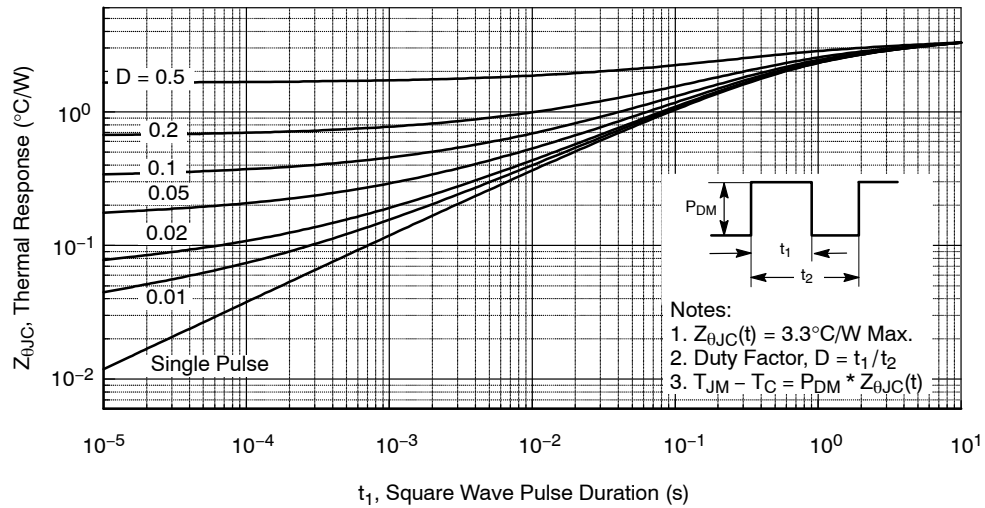
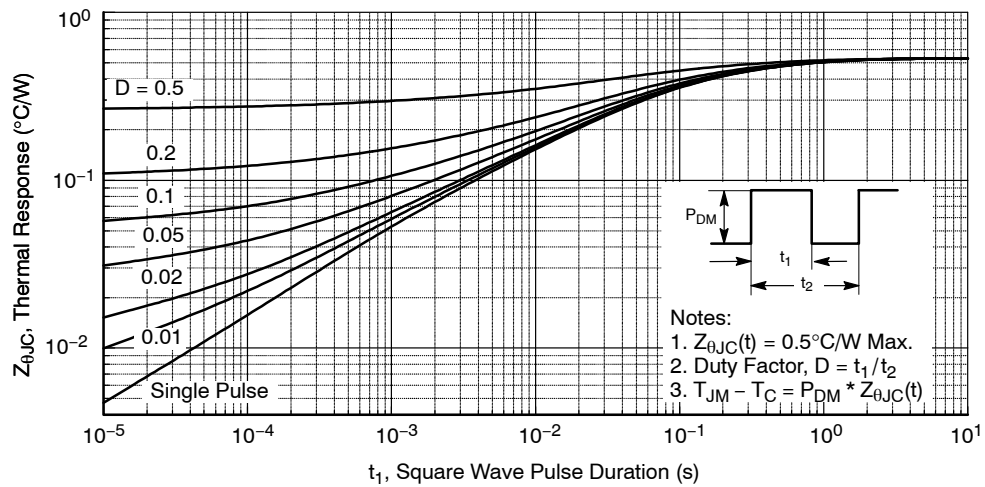


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



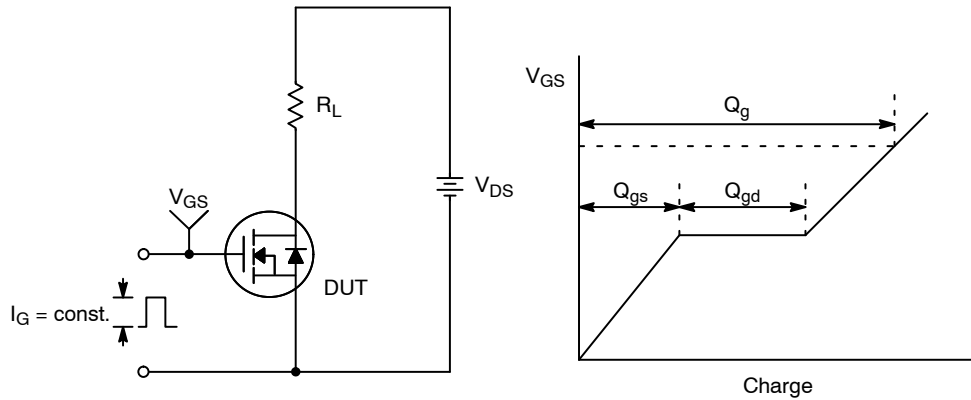


Figure 12. Gate Charge Test Circuit & Waveform

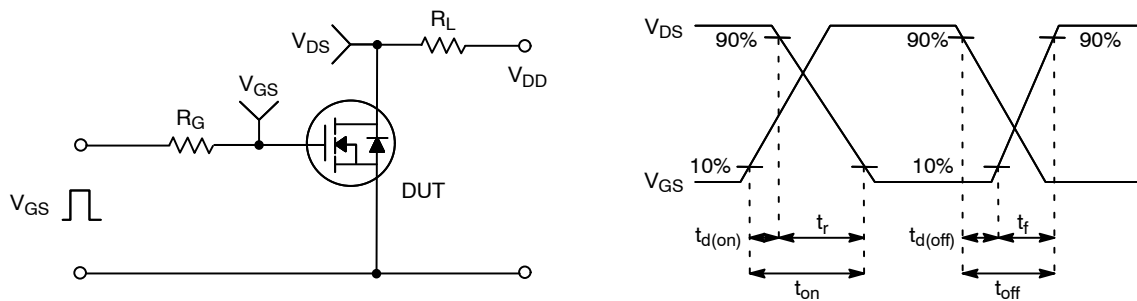


Figure 13. Resistive Switching Test Circuit & Waveforms

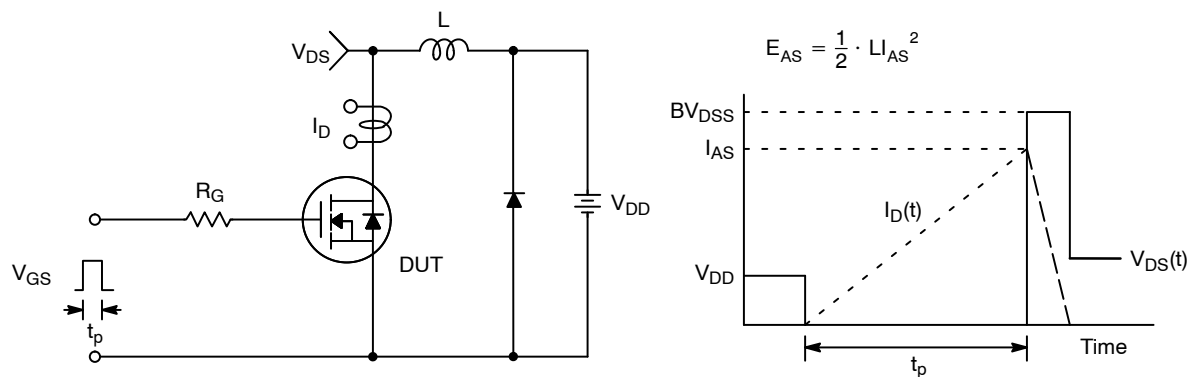


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FDP18N50 / FDPF18N50 / FDPF18N50T

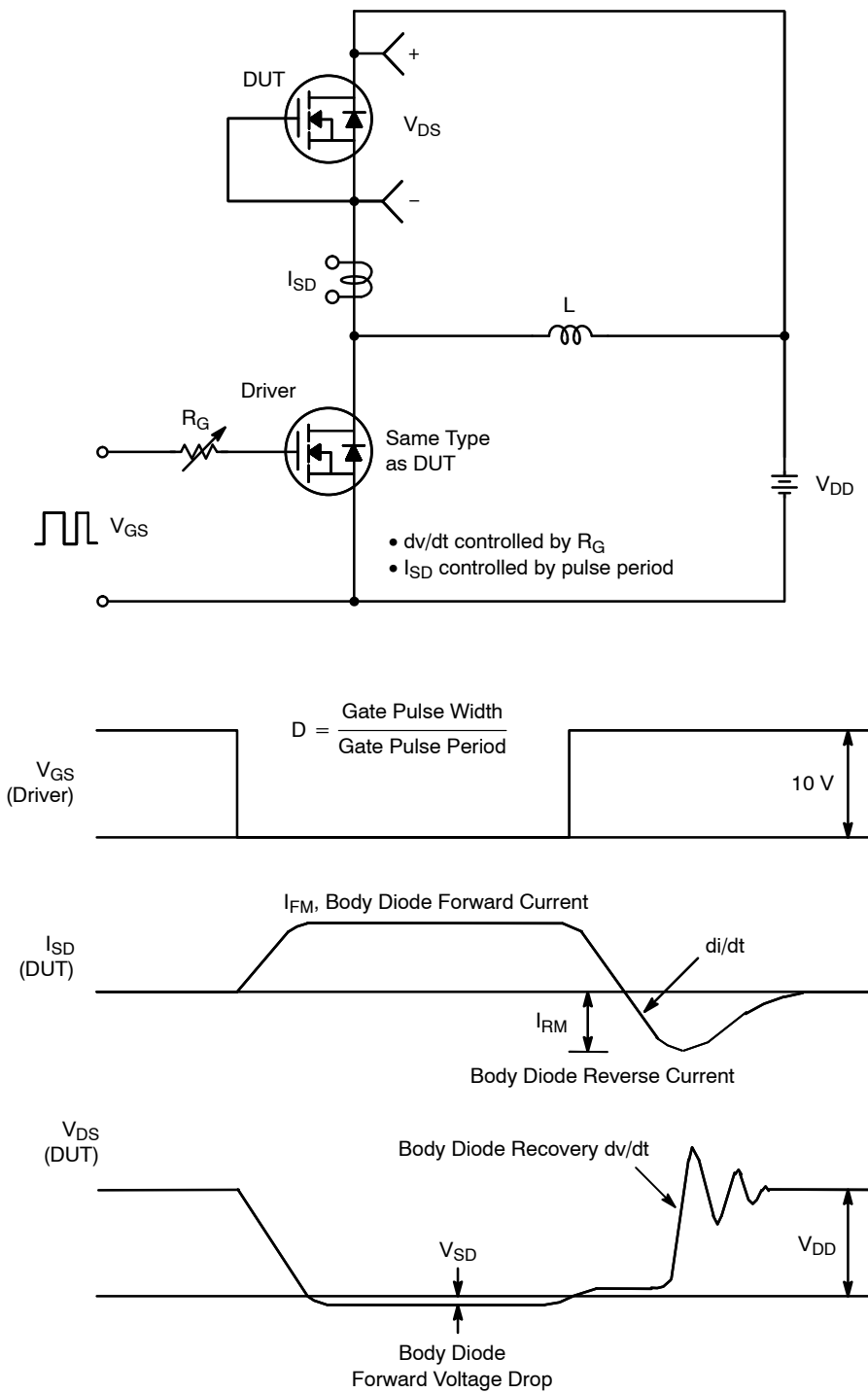
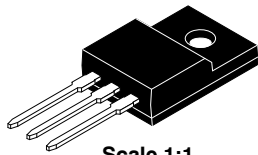


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

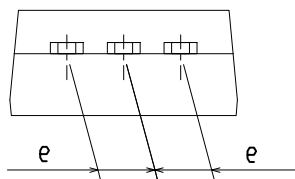
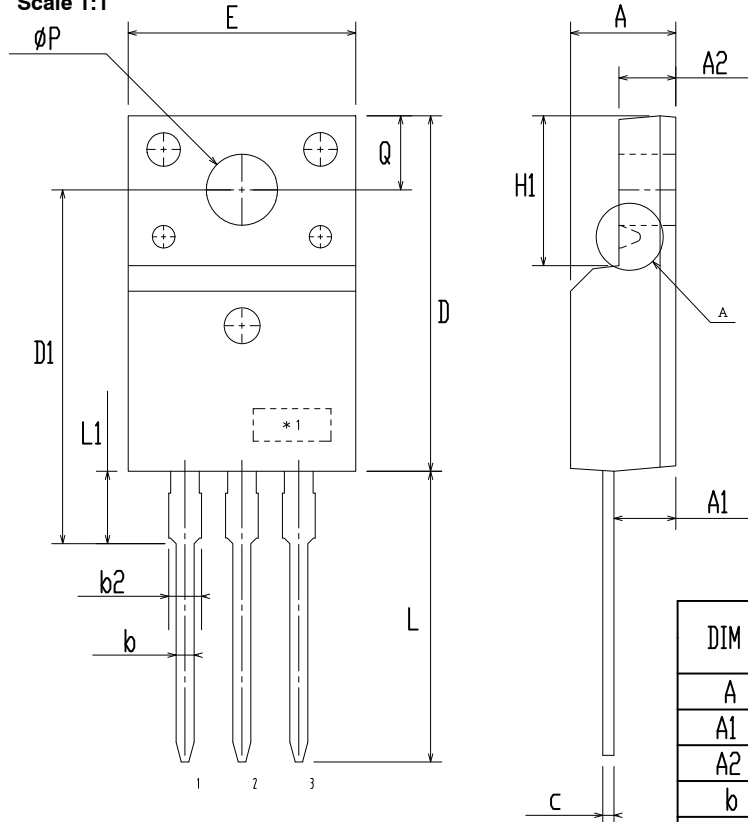
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TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE B

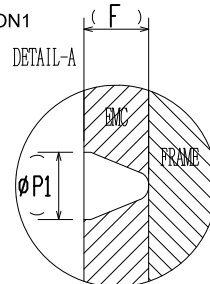
DATE 19 JAN 2021



Scale 1:1



OPTION1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Ø P	2.98	3.18	3.38
Ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009

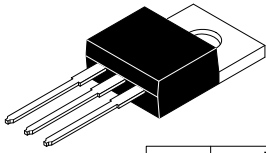
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.

C. OPTION 1 - WITH SUPPORT PIN HOLE

OPTION 2 - NO SUPPORT PIN HOLE

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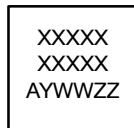
TO-220-3LD CASE 340AT ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

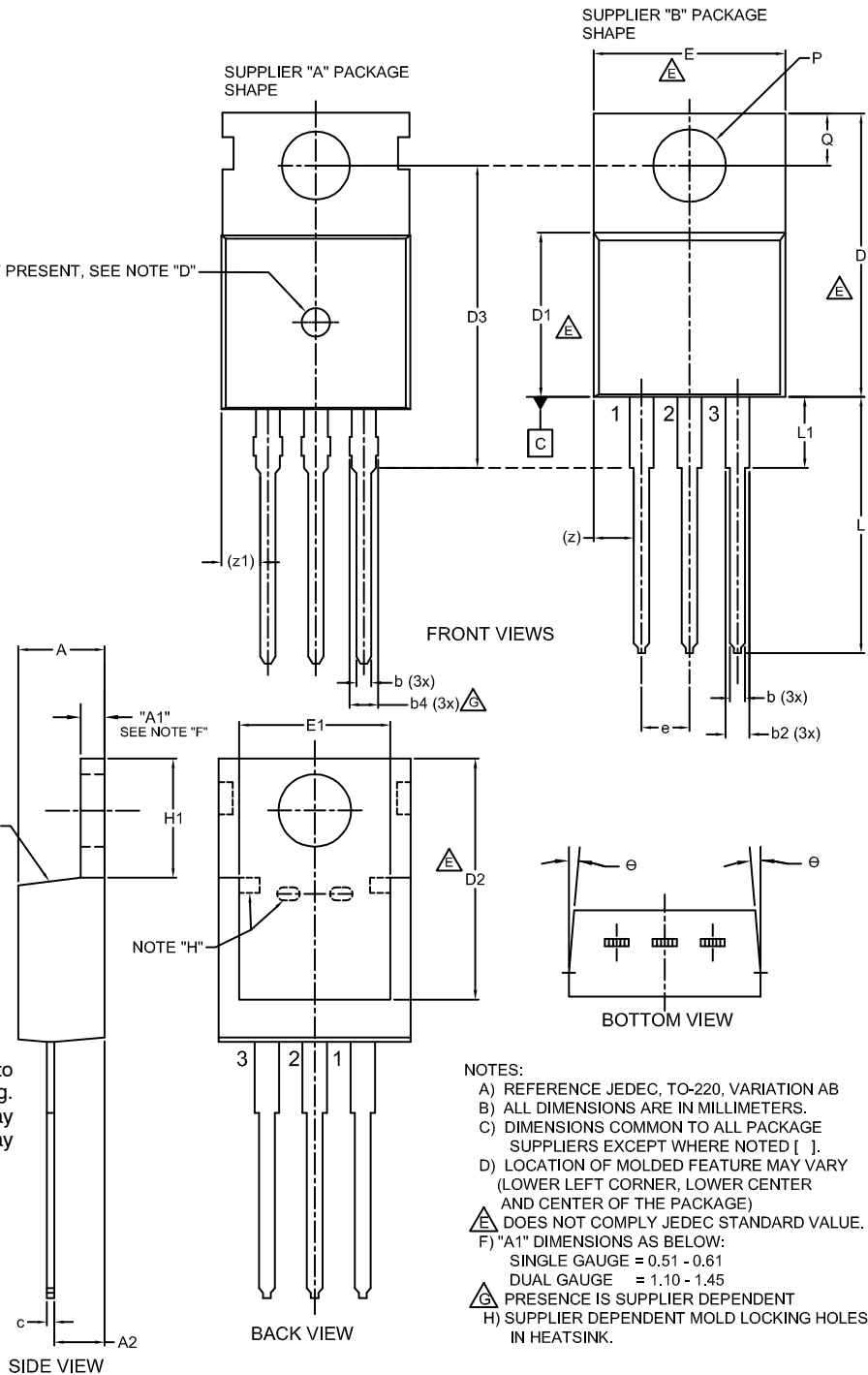
IF PRESENT, SEE NOTE "D"

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- △ DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
- △ PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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