

RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

Check for Samples: [TRS3253E-EP](#)

FEATURES

- V_L Pin for Compatibility With Mixed-Voltage Systems Down to 1.8 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
 - ± 8 kV IEC 61000-4-2 Air-Gap Discharge
 - ± 8 kV IEC 61000-4-2 Contact Discharge
 - ± 15 kV Human-Body Model
- Low 300- μ A Supply Current
- Specified 1000-kbps Data Rate
- Auto Powerdown Plus Feature

APPLICATIONS

- Hand-Held Equipment
- PDAs
- Cell Phones
- Battery-Powered Equipment
- Data Cables

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

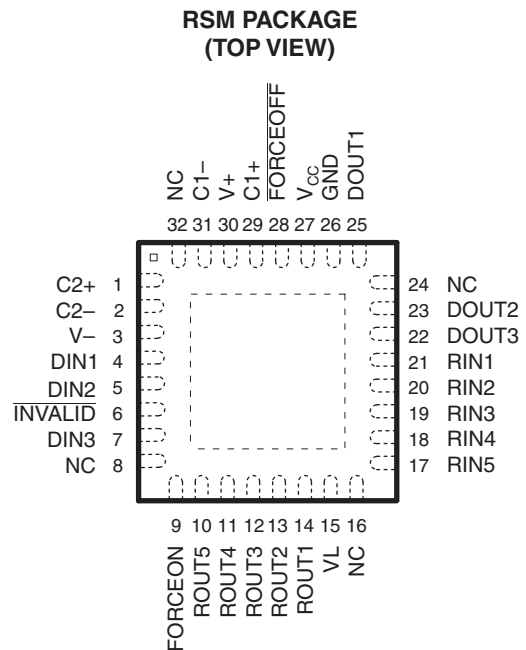
- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DESCRIPTION

The TRS3253E is a three-driver and five-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ± 8 kV using the IEC 61000-4-2 Air-Gap Discharge method, ± 8 kV using the IEC 61000-4-2 Contact Discharge method, and ± 15 kV using the Human-Body Model.

The charge pump requires only four small 0.1- μ F capacitors for operation from a 3.3-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232-compliant output levels.

The TRS3253E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. This eliminates the need for additional voltage level shifter while interfacing with low-voltage microcontroller or UARTs. The TRS3253E is available in a space-saving QFN package (4 mm $\times$ 4 mm RSM).



NC – No internal connection



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DESCRIPTION (CONTINUED)

Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal is applied to any receiver or driver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 μs . INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 μs . Refer to [Figure 6](#) for receiver input levels.

ORDERING INFORMATION⁽¹⁾

T _J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	QFN - RSM	TRS3253EMRSMREP	RS53EP	V62/13621-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 μs	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 μs	L	
L	L	H	>30 μs	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 μs	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

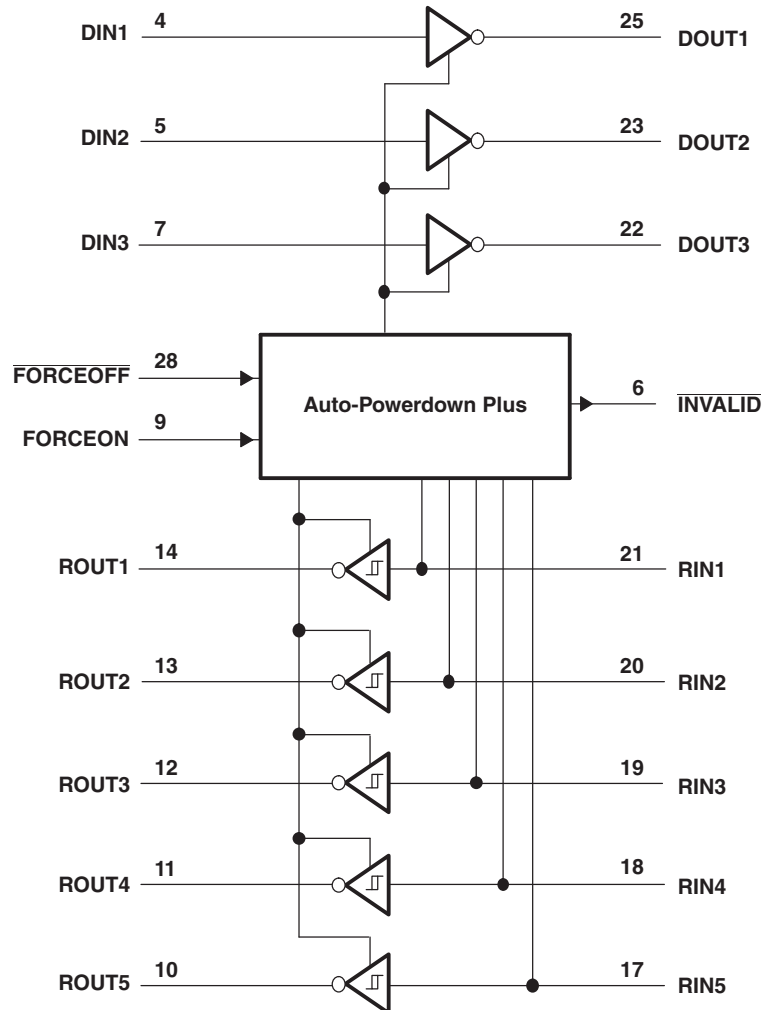
INPUTS			OUTPUTS	RECEIVER STATUS
RIN1–RIN5	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1-ROUT5	
X	L	X	Z	Powered off
L	H	<30 μs	H	Normal operation with auto-powerdown plus disabled/enabled
H	H	<30 μs	L	
Open	H	<30 μs	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	RSM	
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	30	5.5-V supply generated by the charge pump
C1–, C2–	31, 2	Negative terminal of the voltage-doubler charge-pump capacitor
INVALID	6	Invalid Output Pin
V–	3	–5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	4 5 7	Driver inputs
ROUT5 - ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V_L .
V_L	15	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN5-RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	22 23 25	RS-232 driver outputs
GND	26	Ground
V_{CC}	27	3-V to 5.5-V supply voltage
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to Truth Table)
FORCEON	9	Powerdown Control input (Refer to Truth Table)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} to GND			–0.3	6	V
V_L to GND			–0.3	$V_{CC} + 0.3$	V
$V+$ to GND			–0.3	7	V
$V-$ to GND			0.3	–7	V
$V+ + V- ^{(2)}$				13	V
V_I Input voltage	DIN, $\overline{\text{FORCEOFF}}$ to GND, FORCEON to GND		–0.3	6	V
	RIN to GND			± 25	
V_O Output voltage	DOUT to GND			± 13.2	V
	ROUT		–0.3	$V_L + 0.3$	
T_J Junction temperature				150	°C
T_{stg} Storage temperature range			–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- (2) $V+$ and $V-$ can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TRS3253E-EP	UNITS
		RSM	
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	37.2	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	30.1	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	7.8	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.4	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	7.6	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	2.4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{CC}	Supply voltage		3	5.5	V
V _L	Supply voltage		1.65	V _{CC}	V
Input logic threshold low	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V _L = 3 V or 5.5 V	0.8		V
		V _L = 2.3 V	0.6		
		V _L = 1.65 V	0.5		
Input logic threshold high	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V _L = 5.5 V	2.4		V
		V _L = 3 V	2.0		
		V _L = 2.7 V	1.4		
		V _L = 1.95 V	1.25		
Junction temperature			−55	125	°C
Receiver input voltage			−25	25	V

ELECTRICAL CHARACTERISTICS⁽¹⁾

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON		±0.01	±2.9	μA
I _{CC}	Supply current (T _J = 25°C)	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V _{CC}	0.5	1.11	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND	1	10	
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V _{CC} , FORCEON at GND, All RIN are open or grounded	1	10	μA

(1) Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_J = 25°C.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±8	
	IEC 61000-4-2 Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over junction temperature range, $V_{CC} = V_L = 3\text{ V}$ to 5.5 V , $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I_{off}	Output leakage current	ROUT, receivers disabled			± 0.05	± 25	μA
V_{OL}	Output voltage low	$I_{OUT} = 1.6\text{ mA}$				0.4	V
V_{OH}	Output voltage high	$I_{OUT} = -1\text{ mA}$		$V_L - 0.6$	$V_L - 0.1$		V
V_{IT-}	Input threshold low	$T_J = 25^\circ\text{C}$	$V_L = 5\text{ V}$	0.8	1.2		V
			$V_L = 3.3\text{ V}$	0.6	1.5		
V_{IT+}	Input threshold high	$T_J = 25^\circ\text{C}$	$V_L = 5\text{ V}$		1.8	2.4	V
			$V_L = 3.3\text{ V}$		1.5	2.4	
V_{hys}	Input hysteresis				0.5		V
	Input resistance	$T_J = 25^\circ\text{C}$		3	5	7	k Ω

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$

Switching Characteristics

over junction temperature range, $V_{CC} = V_L = 3\text{ V}$ to 5.5 V , $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_J = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, $C_L = 150\text{ pF}$	0.15	μs
t_{PLH}			0.15	
$t_{PHL} - t_{PLH}$	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{\text{FORCEOFF}}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{\text{FORCEOFF}}$	200	ns

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$.

DRIVER SECTION

Electrical Characteristics

over junction temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_J = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH} Output voltage swing	All driver outputs loaded with $3\text{ k}\Omega$ to ground, $V_{CC} = 3.1\text{ V to }5.5\text{ V}$	± 5	± 5.4		V
r_O Output resistance	$V_{CC} = V_+ = V_- = 0$, Driver output = $\pm 2\text{ V}$	300	10M		Ω
I_{OS} Output short-circuit current	$V_{T_OUT} = 0$			± 60	mA
I_{OZ} Output leakage current	$V_{T_OUT} = \pm 12\text{ V}$, $\overline{\text{FORCEOFF}} = \text{GND}$, $V_{CC} = 3\text{ V to }3.6\text{ V}$			± 25	μA
	$V_{T_OUT} = \pm 12\text{ V}$, $\overline{\text{FORCEOFF}} = \text{GND}$, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$				
Driver input hysteresis				0.5	V
Input leakage current	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		± 0.01	± 2.9	μA

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$

Timing Requirements

over junction temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_J = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER				MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate		R _L = 3 kΩ, C _L = 200 pF, One driver switching		1000			kbps
Time-to-exit powerdown		V _{T_OUT} > 3.7 V		100			μs
t _{PHL} – t _{PLH}	Driver skew ⁽²⁾			100			ns
Transition-region slew rate		V _{CC} = 3.3 V, T _J = 25°C, R _L = 3 kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V	C _L = 150 pF to 1000 pF	15		150	V/μs

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$.

(2) Driver skew is measured at the driver zero crosspoint.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see [Figure 7](#))

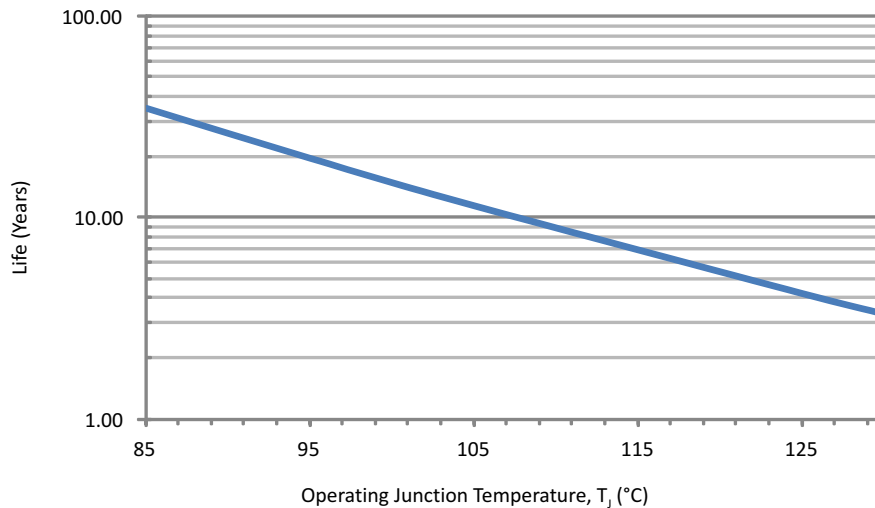
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_L		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_L	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V_L	-0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = -1\text{ mA}$, FORCEON = GND, FORCEOFF = V_L	$V_L - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6\text{ mA}$, FORCEON = GND, FORCEOFF = V_L		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see [Figure 7](#))

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		μs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		μs
t_{en}	Supply enable time		25		μs
t_{dis}	Receiver or driver edge to auto-powerdown plus		30		μs

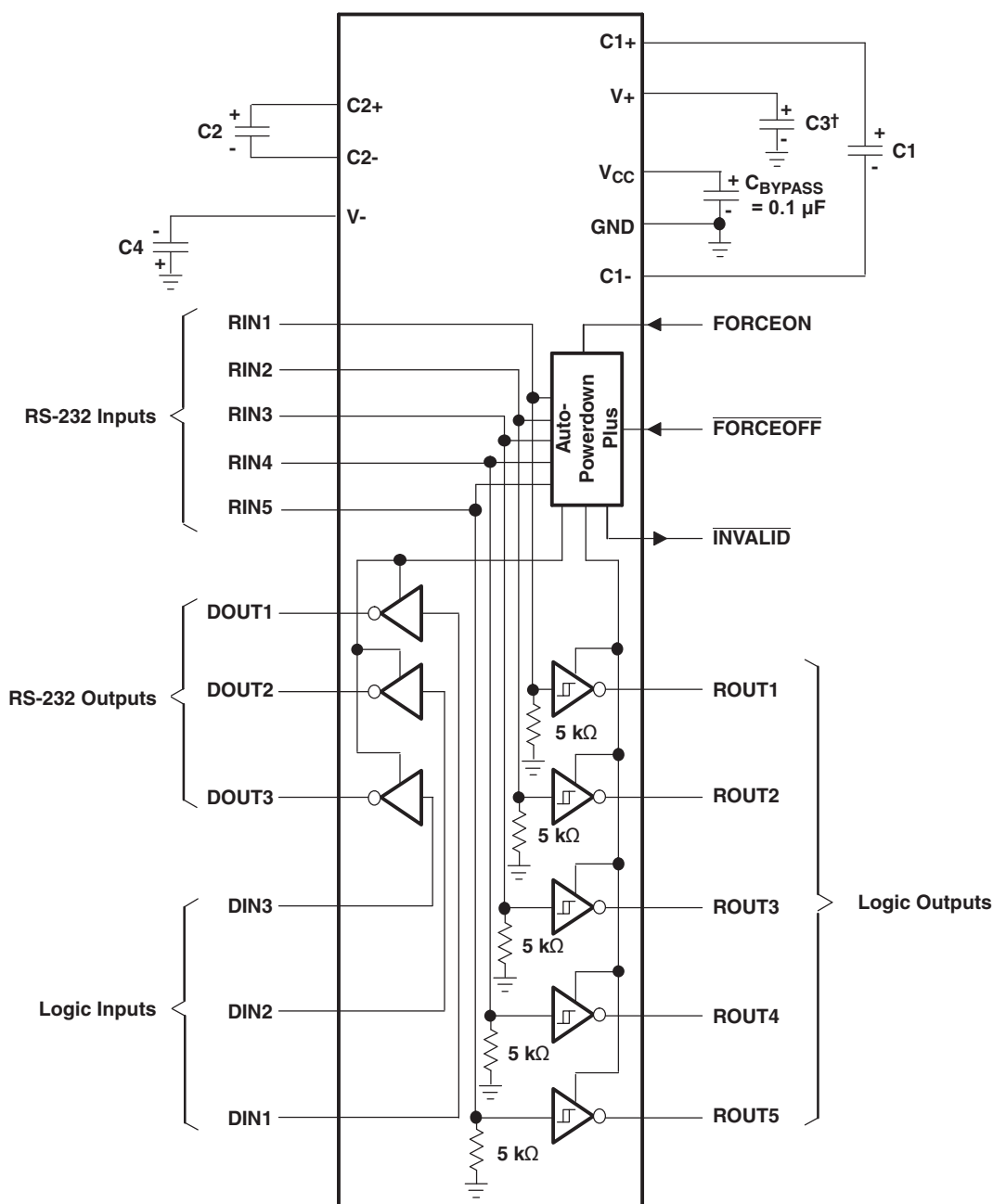
(1) All typical values are at $V_{CC} = V_L = 3.3\text{ V}$ and $T_J = 25^\circ\text{C}$.



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

Figure 1. TRS3253E-EP Operating Life Derating Chart

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 2. Typical Operating Circuit and Capacitor Values

PARAMETER MEASUREMENT INFORMATION

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

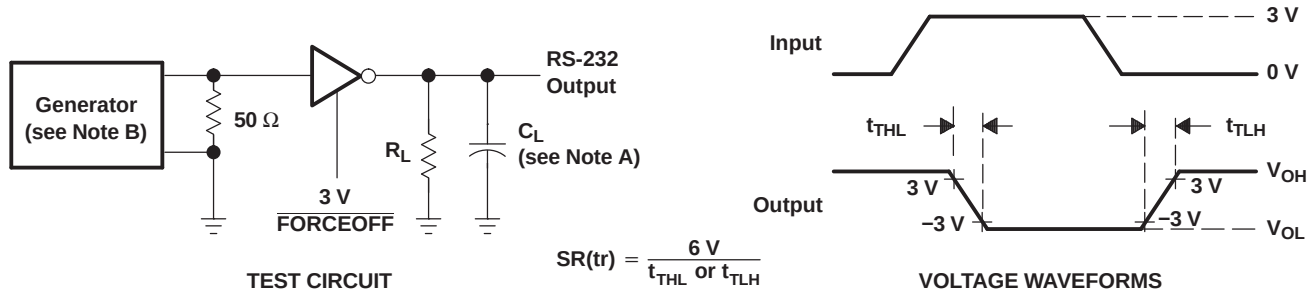


Figure 3. Driver Slew Rate

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

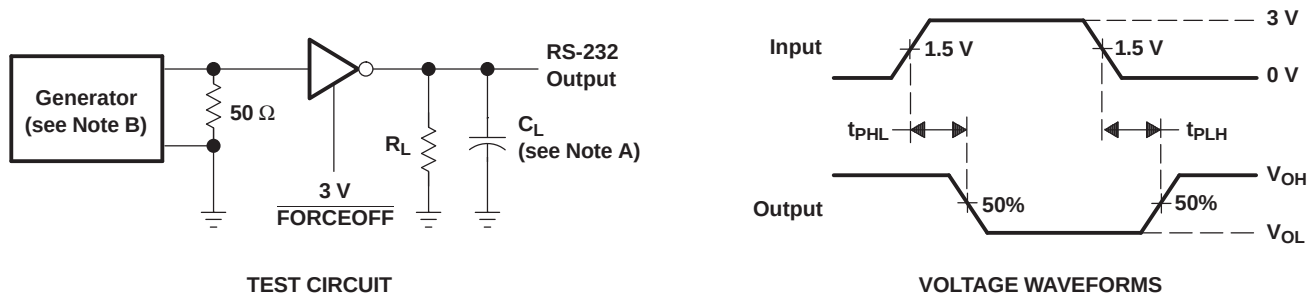


Figure 4. Driver Pulse Skew

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

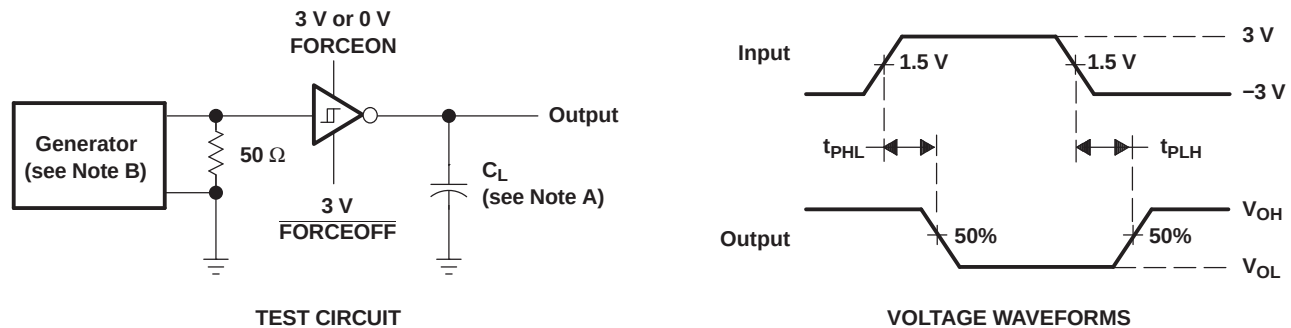


Figure 5. Receiver Propagation Delay Times

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

PARAMETER MEASUREMENT INFORMATION (continued)

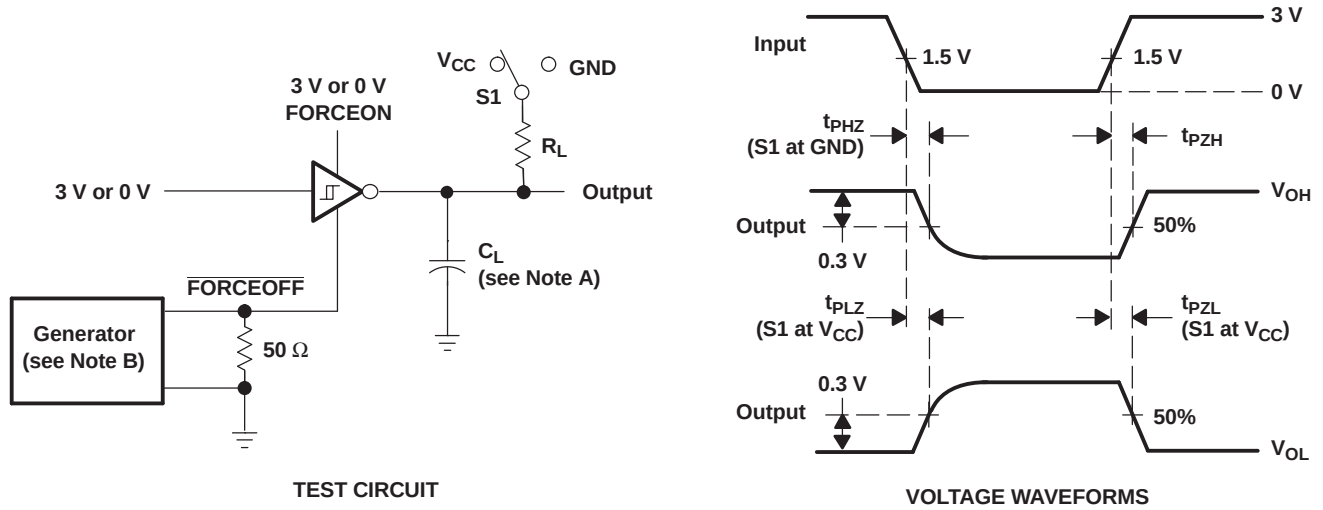
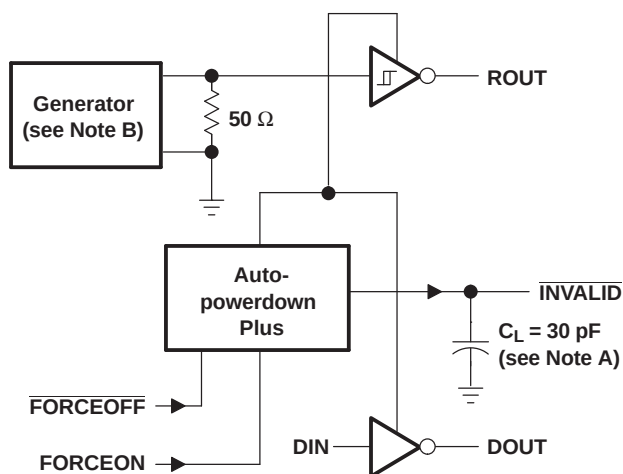


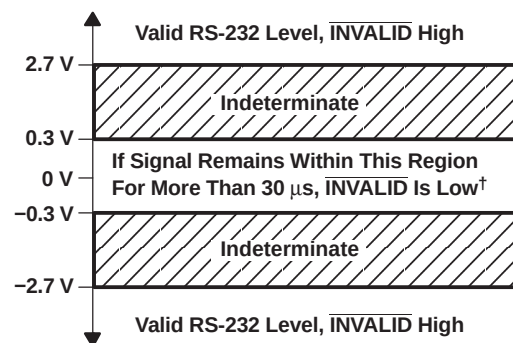
Figure 6. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.



† Auto-powerdown plus disables drivers and reduces supply current to 1 μA .

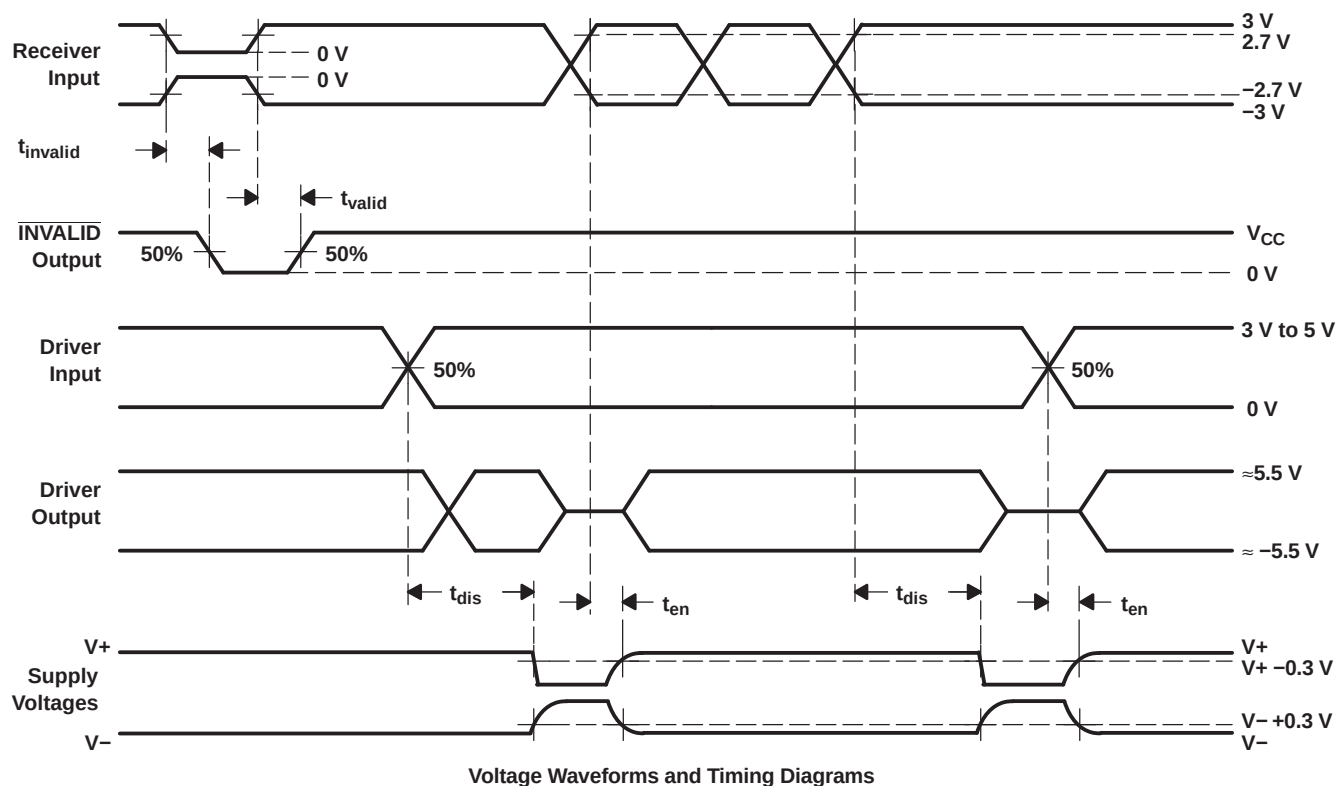


Figure 7. $\overline{\text{INVALID}}$ Propagation-Delay Times and Supply-Enabling Time

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3253EMRSMREP	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples
V62/13621-01XE	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TRS3253E-EP :

- Catalog: [TRS3253E](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

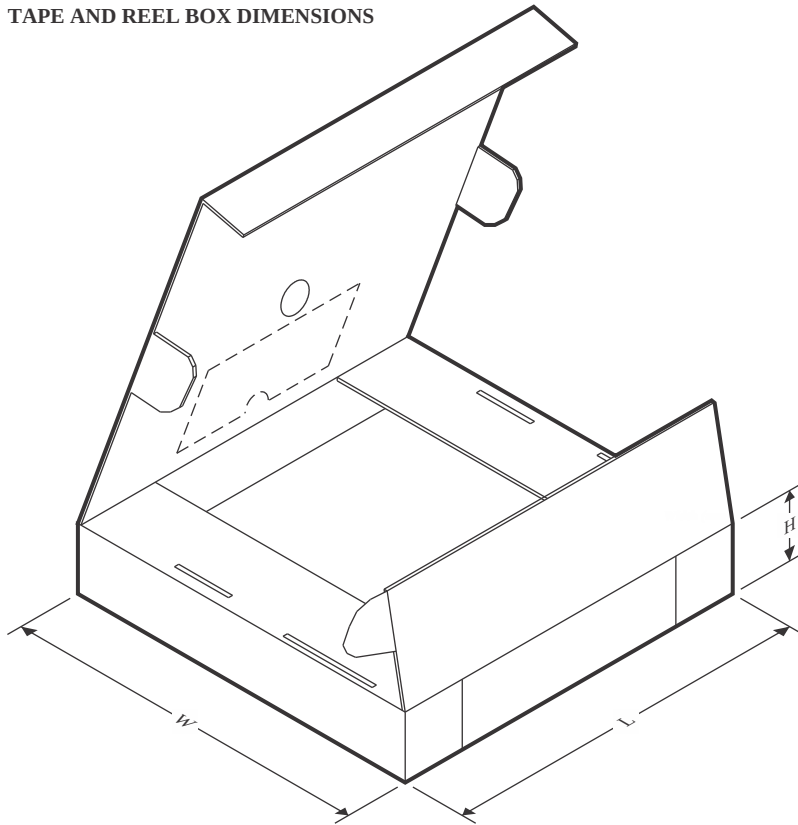
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3253EMRSMREP	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3253EMRSMREP	VQFN	RSM	32	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

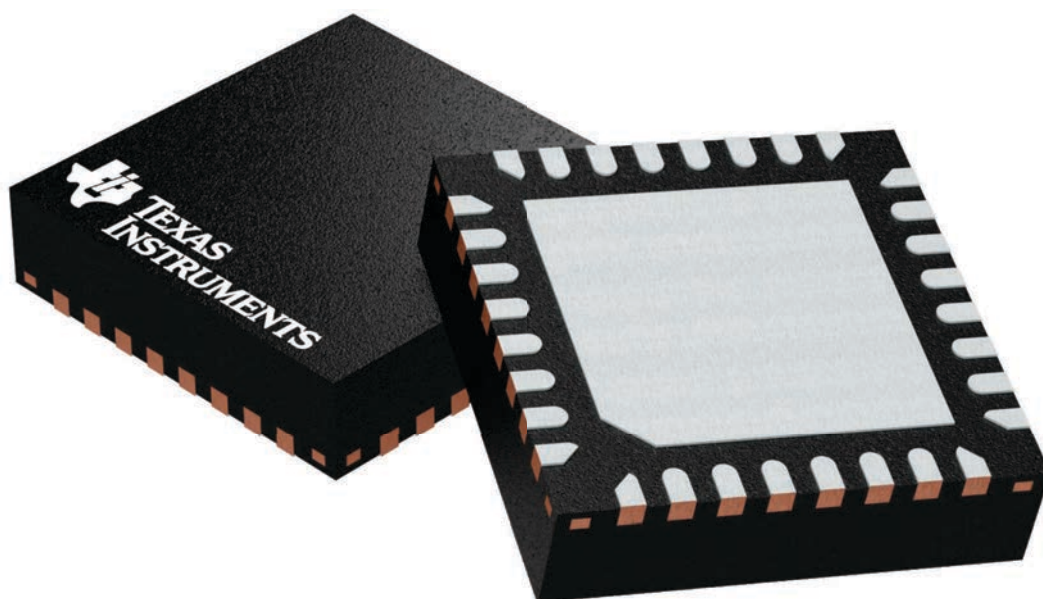
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



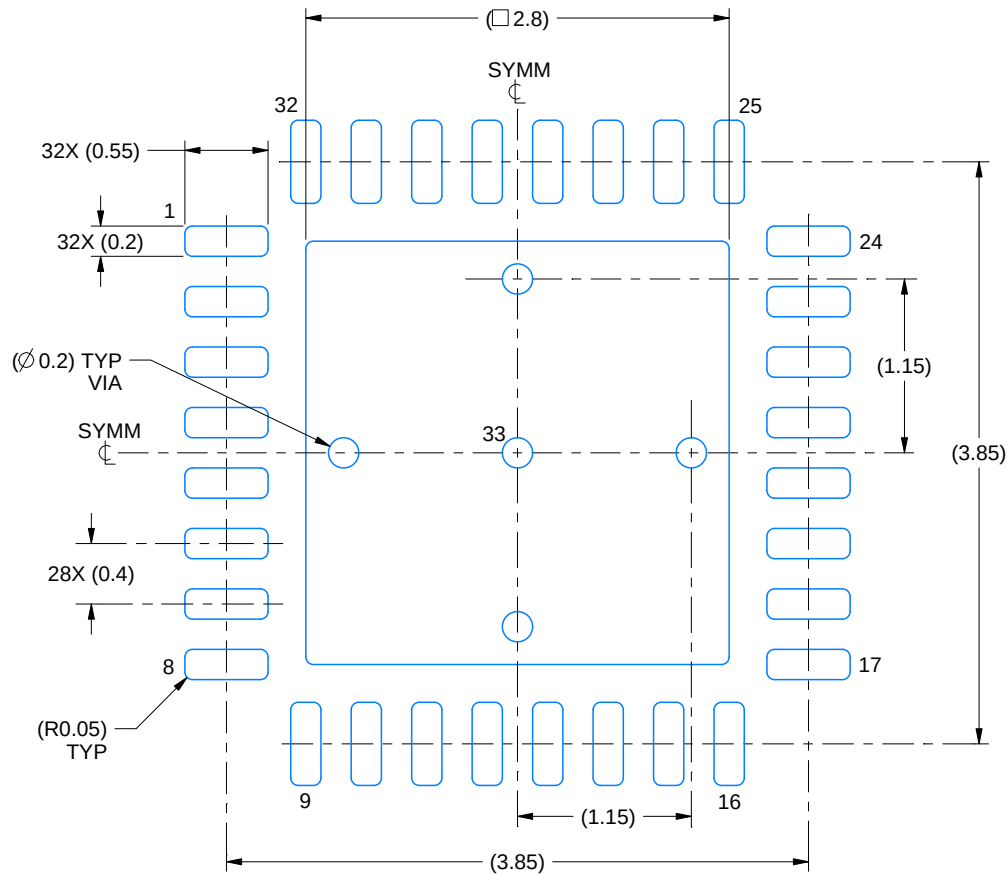
4224982/A

EXAMPLE BOARD LAYOUT

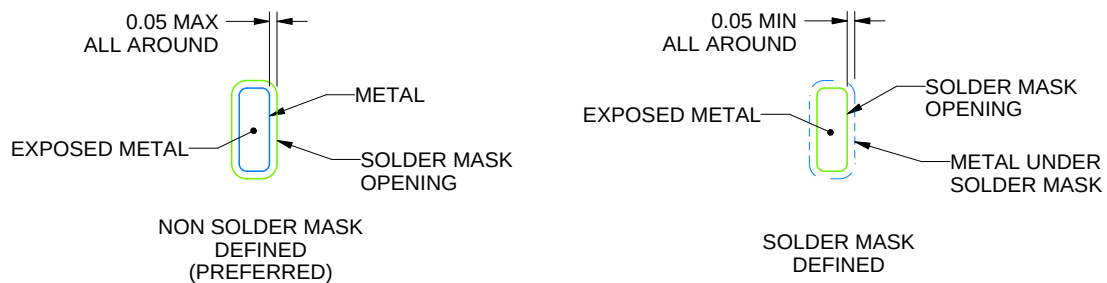
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

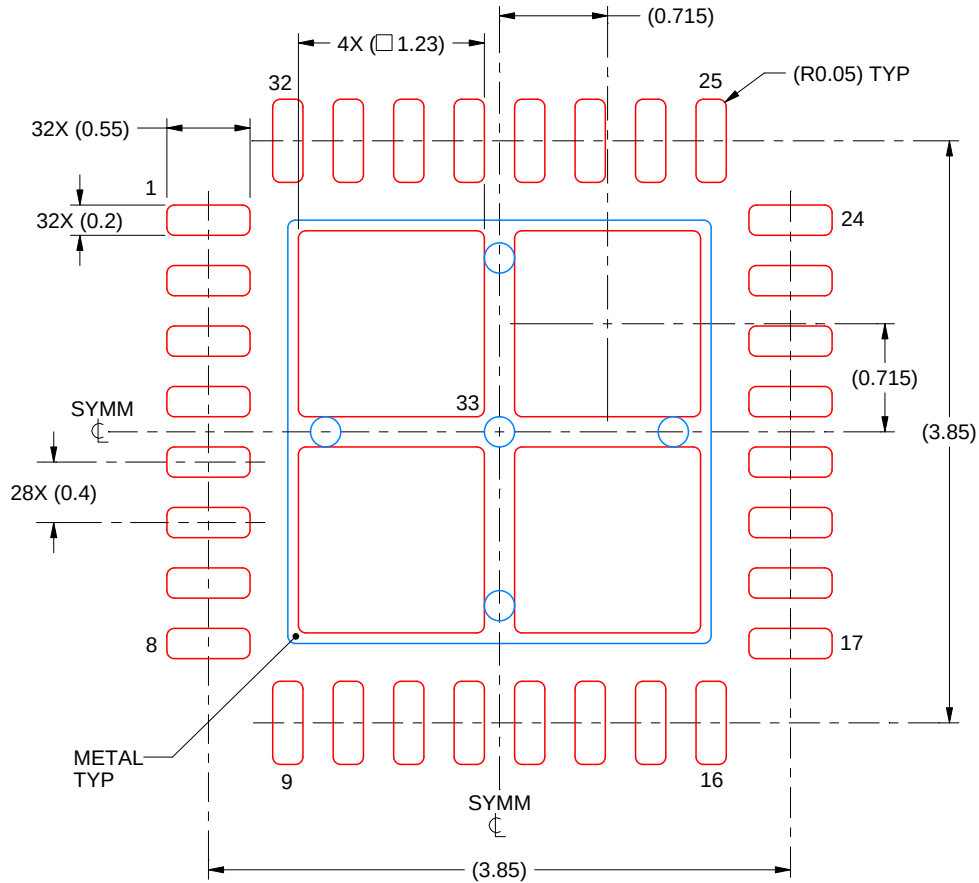
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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