Qorivva MPC5748G Family for Body Control/Gateway Applications

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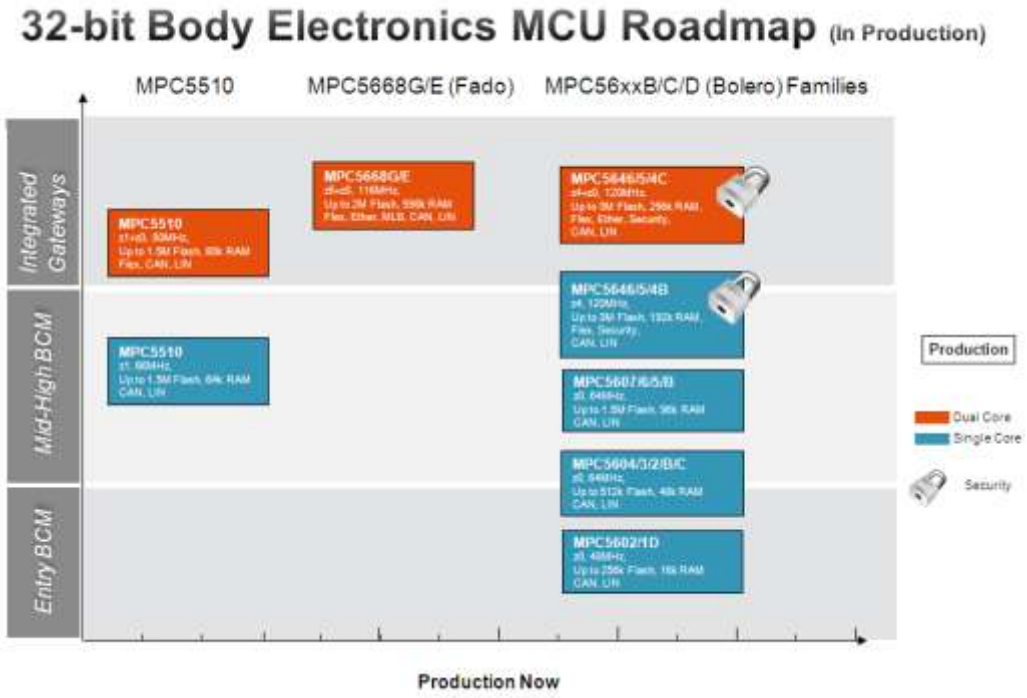
Agenda

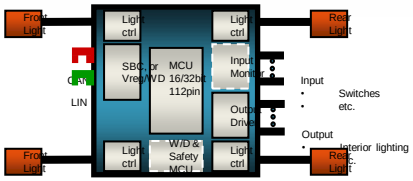
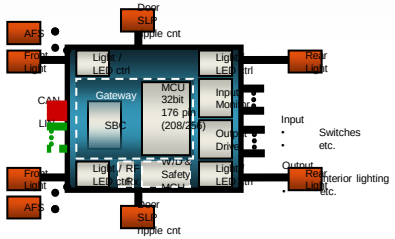
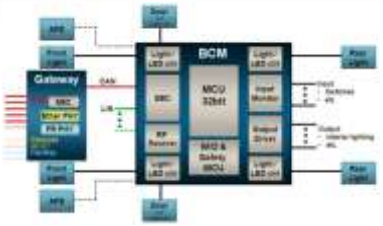
- Freescale 32-bit Body Legacy
- MPC5510/Fado/Bolero Family of Products
- Next Gen Body Market Trends and Challenges
- MPC5748G Body Control Module/Gateway Family

Freescale 32-bit Body Legacy and Current Product Families

- Freescale is a Leader in the 32-bit body MCU space
  - Three generations of products in production today.
  - First targeted body product launch was the dual core MPC5510 family nearly 5 years go.
  - Fado offered one of the first integrated single chip solutions for gateway applications.
  - Bolero family offers a broad family feature set offering for a range of BCM/Gateway applications.

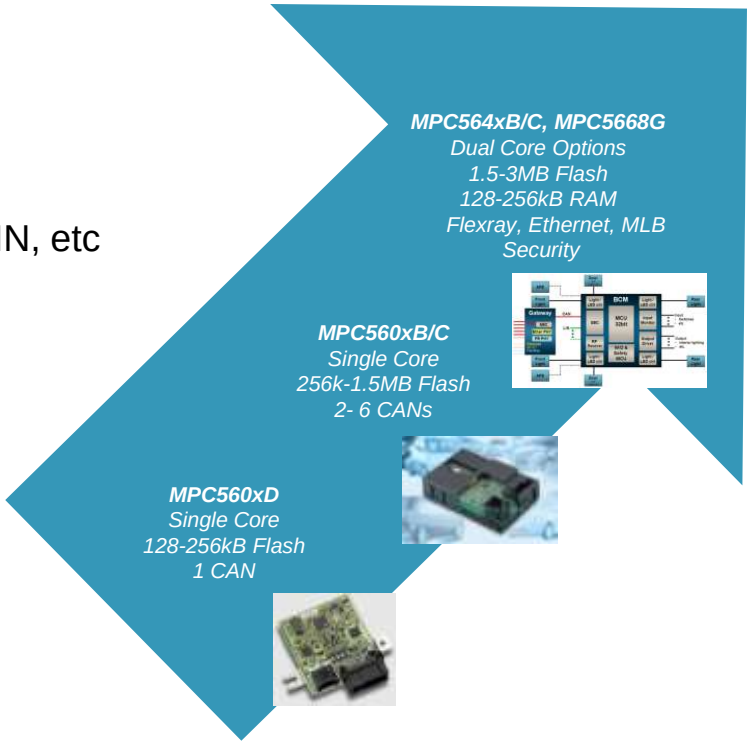


Bolero Family Product Offering

	Entry Level BCM	Mid-Range BCM	High-End BCM/GTWY
			
Applications	Basic functions, e.g. lighting, immobilizer, power management	+ Multiple CAN + other peripheral Functions - doors, seats	+ Extended comfort and lighting functions + Ethernet//CAN GTWY
Feature Needs	16-/32-bit MCU <512k Flash 1-2 CAN 1-2 LIN <112 LQFP	1 x 16-/32-bit MCU <1.5MB Flash 3-4 CAN 7 LIN 144/176 LQFP	2 x 32-bit MCU >2MB Flash 3-5 CAN 8+ LIN Potential Flexray, Ethernet 176 LQFP – 256 BGA
Freescale Solution	MPC5604/3/2B/C/D z0 48-64MHz Up to 512KB Flash, Up to 48KB RAM Up to 6 CAN, 4 LIN, 3 SPI 64-100-144 Pin	MPC5607/6/5B z0 64MHz Up to 1.5M Flash, Up to 96KB RAM Up to 6 CAN, 10 LIN, 6 SPI 100-176 Pin	MPC5646/5/4B/C z4 + z0 120+60MHz Up to 3M Flash, Up to 256KB RAM Up to 6 CAN, 10 LIN, 8 SPI Flexray, Ethernet, Security 176-256 Pin

Existing FSL MCUs for 32-bit Automotive Networking

- **Family Concept**
  - Completely scalable family of Qorivva BCM/gateway solutions ranging from CAN/LIN only BCMs to advanced Gateway solutions integrating LIN, CAN, Ethernet, MLB, FlexRay on a single chip
  - From 128k to 3M Flash options
- **Performance**
  - High-performance cores with optimized system architecture
  - From single-core to multi-core MCUs
  - 48MHz to 120MHz with Crossbar architecture
- **Advanced Peripherals**
  - Ethernet, FlexRay, MOST, Security Modules, CAN, LIN, etc
- **Power Consumption**
  - Aggressive run, stop, standby values
- **Acceptance**
  - Widely utilized by major Tier 1s/OEMs
- **Availability**
  - Qualed today, in mass production now



Body Market Trends and Challenges

- Personalization options driving **LIN** nodes
- **Ethernet** and **wireless** communication
- **More complex Gateways** with higher performance and multi-core usage (Expanding memory)

- Functional Safety - **ISO26262**
  Several body-apps need **ASIL A/B** (some C/D)
- **Security/Cryptography** for Gateway and BCM modules

- **Power management** in stop and run modes
- Autosar SW management of partial/pretended networking
- EC-motors, LED-lighting

- Cost reduction via **ECU integration**
- Electrification of the car replacing mech. components
- **Scalability** of hardware and software
- **Auto generated code** to decrease dev costs

Software Integration:

- Autosar:
  - Multicore-support
  - OS
  - MCAL
- Safety:
  - SW-routines supporting self-test (Core/Memory)
- Security:
  - Cryptography algorithmic support
- Application-support
  - Motor Control-library
  - Reference designs

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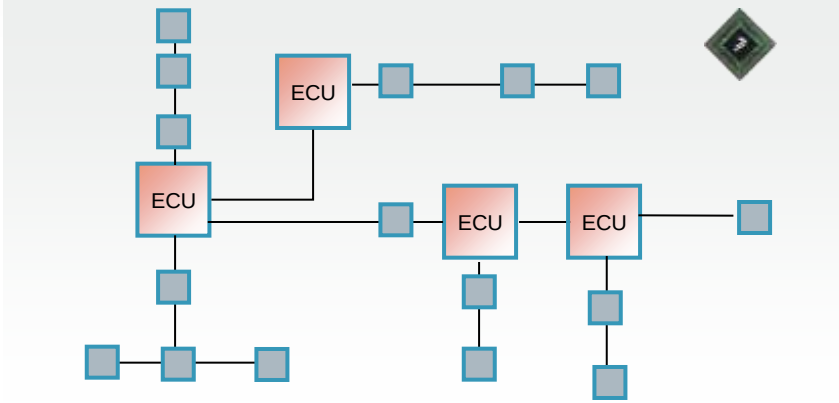
Vehicle Architectural Trends

Today

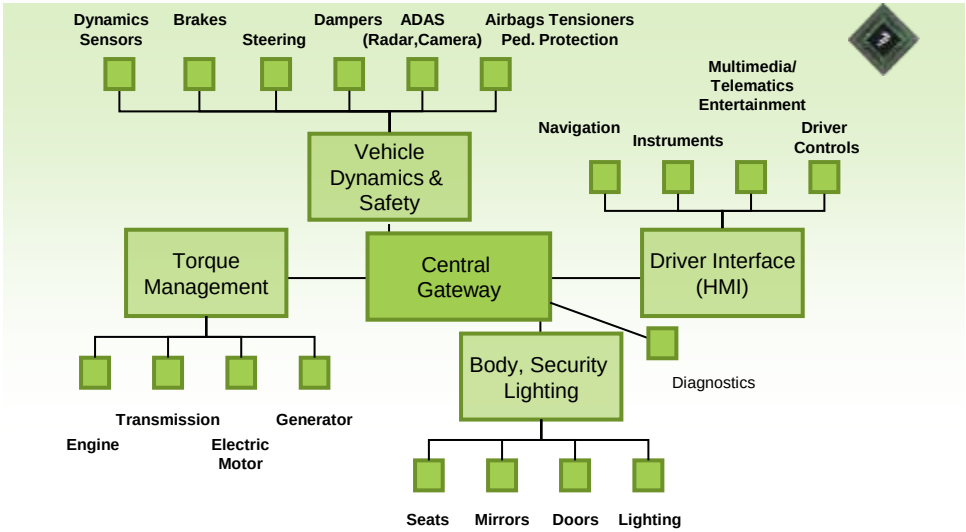


Distributed Electronic Control Units

One ECU per mechanical function- Connected by multiple CAN and LIN interfaces

- Up to 80 individual ECUs
- Local and proprietary network structures
- Increasing software complexity
- Increasing cabling weight
- Increasing ... everything

Future



Distributed Computing

Major computing nodes on a high performance network organized by "domains" which control "zones"

- Increasing data traffic
- Ethernet as potential backbone
- Lower power: Partial/pretended networking
- Autosar 4.0

Introducing the *New* Qorivva MPC5748G Body Control Module/Gateway MCUs

Integration, Low Power, Security & Safety

Unprecedented Integration

Single-chip solution offering multicore architecture and advanced networking protocols for next generation communication requirements while reducing the quantity of body control/gateway ECUs

Low Power Management

New low-power modes, analog comparators, and pretended networking support help meet stringent next generation power budgets and ensure greener vehicles

Functional Safety and Security

Security modules protect ECUs against various attack scenarios and Safety modules ensure robust operation per ISO 26262

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Highly Integrated Body Control/Gateway MCU

- **Performance through Multicore**
  - Up to three e200 cores built on Power Architecture technology, with up to 160 MHz performance allows for easy division of tasks in an integrated BCM/gateway system
- **Most Diverse Set of Networking Communication**
  - Ethernet with AVB support, FlexRay™, MLB, USB, up to eight CAN with CAN Flexible Data Rate (FD) up to 18 LIN, SDIO interface, I^2S all supported on a single-chip solution
- **Flexible Memory Options**
  - Up to 6 MB Flash and 768 KB of embedded SRAM provide suitable storage to maintain the local BCM/gateway application functionality, handle message buffering, and also store additional Flash images for other nodes in the vehicle

MPC5748G Platform : Next Gen e200 CPUs

Features	z4 (Calypso)	z4 (Bolero)	z2 (Calypso)	z0 (Bolero)
Frequency (in platform)	160	120	80	64
Pipeline depth	5 stage	5 stage	4 stage	4 stage
Multiply	2 cycle latency	2 cycle latency	1 cycle latency	1 - 4 cycles latency
Divide	4 - 14 clocks	4 - 14 clocks	4 - 14 clocks	5 - 34 clocks
VLE	Yes	Optional	Yes	Yes
E2E-ECC	Yes	No	Yes	No
ICACHE	8k	4k	No	No
DCACHE	4k	No	No	No
Prefetch Buffer	8 x 32 bit, fetched as 64 bit double word	8 x 32 bit, fetched as 64 bit double word	4 x 32 bit, fetched as 64 bit double word	4 x 32 bit, fetched as 32 bit word
FPU	Scalar	Vector	No	No
Nexus level	3+	3+	3+	2+

- MPC5748G offers similar Power Architecture based e200 cores as Bolero
- Enhancements in frequency, Multiply/Divide, ECC, Buffers, etc

CAN FD Support

- **CAN FD** stands for **CAN with Flexible Data-Rate**
- CAN FD is a variant of CAN proposed by Bosch to:
  - Increase the bit rate of the data portion of a CAN message (Up to 1-8Mbps)
  - Increase the number of data bytes that can be sent in a single CAN message to up to 64 bytes (vs standard 8 bytes)
- CAN FD initial use case will be for end of line programming. As memory sizes in the car are increasing, a faster means of programming the car is needed to reduce end of line programming costs.
- Freescale will support CAN FD on the initial MPC5748G umbrella device as well as other subsequent smaller members of the family.

MPC5748G Communication Enhancements

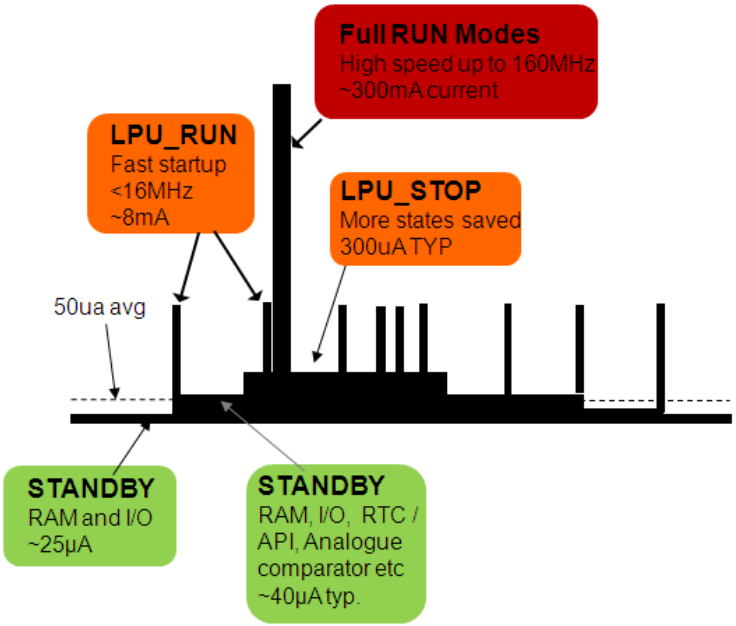
- **Enhanced Ethernet module**
  - 1588 support
  - RMII, MII interfaces
- **Includes separate USB Host and USB Device modules**
  - Allows MPC5748G to interface to wireless modules as well as to connect to infotainment domain
  - Supports low pin count ULPI interface (12 signals)
- **Includes MLB150**
  - Supports all MOST data types
  - Support for 6pin(differential) and 3pin interface
    - Support for multiple speed grades (up to 2048xFs)
- **Enhanced FlexCAN**
  - Added PN support
  - Added CAN FD support
  - Added DMA requests
- **Support for I2S interface via SAI module**

Driving Low Power Consumption

- **New Low-Power Unit**
  - Allows for increased functionality in a lower power monitoring state
  - Bypasses entire platform thereby providing very low power execution modes
- **Analog Comparator**
  - Typical periodic monitoring routines can be fully handled in Standby mode
- **Pretended Networking Support**
  - Advanced filtering, wakeup capabilities and CAN availability in low power modes

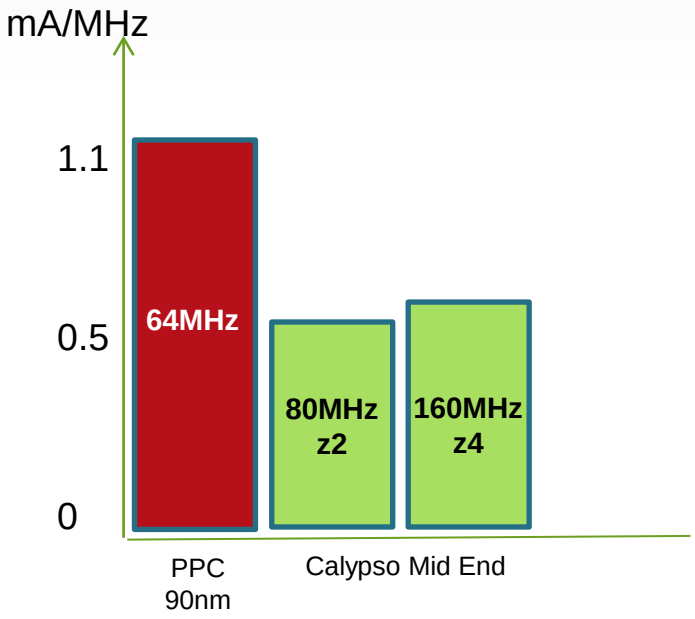
Driving Low Power Consumption – New Low Power Unit (LPU)

- Unique Low Power Unit
  - Provides a mechanism to bypass entire platform including main z4 CPUs, while Interconnects & NVM arrays can remain completely power gated
  - Low Power Unit (LPU) processor is a z2 CPU.
  - The LPU mode supports a smaller set of peripherals (1x CAN, LIN, SPI, ADC, timer, etc.), and provides very low power (single digit mA) execution modes
  - LPU allows for increased functionality in a lower power state, reducing current consumption by over 30% for a typical cyclic wake-up application over previous generation device



Low RUN current with Higher Performance Options

- MPC5748G Family Flexibility
  - The CPU core of z2 was designed to achieve lower power consumption and is capable of operating at 80 MHz.
  - The z4 is designed for higher performance, particularly at 160MHz
  - The combination allows a ***completely scalable power / performance*** trade-off, from 0.5 mA / MHz through to an impressive performance of ***more than 4DMIPS/MHz!***
  - You decide how far to press the accelerator!!!



Device Mode	MHz	Calypso Mid End	mA / MHz
RUN	160	95mA	0.6
	80	45mA	0.5

Analogue Comparator / RTC / API interaction

- Full STANDBY mode autonomous behaviour
- Example:
  - Configure the RTC / API to generate a ‘wakeup’ output every 200ms
  - Configure the RTC / API to have a ‘free-running’ clock output of 1ms period
  - Configure the 8 inputs to be read inside the ANL logic
  - Software enters the low power STANDBY mode
  - API is free-running
  - After 200ms API asserts a ‘trigger enable’ to the comparator
  - Read all inputs
  - If different, wake-up else wait for next 200ms time interval

Addressing Functional Safety and Security

- **Designed with the ISO26262 process in mind**
- **Safe Assure functional safety program:**
  - **Safety Process** - integrating functional safety into dev process
  - **Safety Hardware** - built in self tests, error code correction, etc
  - **Safety Software** - AUTOSAR MCAL, OS, core self tests, etc
  - **Safety Support** - training, documentation and tech support
- **Designed to support next generation security needs**: Security gatekeeper, immobilizers, component protection, protection of data sets
- **Hardware Security Module (HSM) option**

MPC5748G Safety Measures

Single Point Fault Metric

- Platform End to End ECC
- RAM ECC
- Flash ECC
- Undervoltage monitoring
- Clock Monitoring
- Temporal protection – Software Watch dog
- MPU – execution control
- Register protection
- CRC

Latent Fault Metric measures

- Self Tests
  - LBIST – Logic build in test
    - SW triggerable
  - MBIST - Memory build in self test

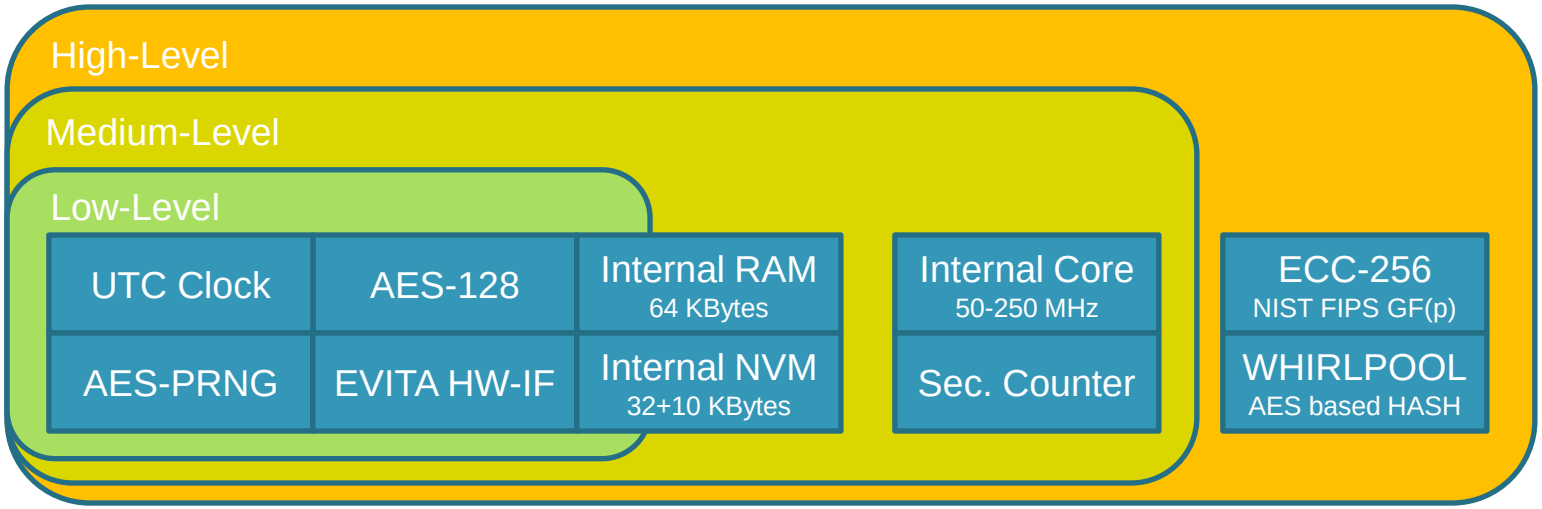
Error Management Modules

- FCCU
  - Fault Collection & Control Unit
- Error Management Unit
  - Error address capturing
  - Interface for error managemen of ECC errors, E2E ECC, etc.

CSE, HSM and the Security Standards

Security Standards	Evita Low	HIS-SHE	HIS-Medium (EVIT-Medium)	EVIT-High
Main features	UID Crypto engine	NVM is mandatory Fix function set	Programmable by customer	PublicKey HASH
CSE Module	supported by MPC564xB/C			
HSM Module	supported by MPC5748G			

EVITA Security Modules



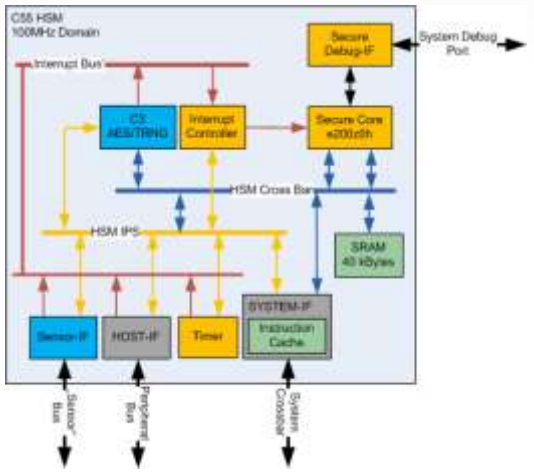
Robust Security Solutions - HSM

Overview:

- Hardware security module (HSM) was developed by FSL to address the HIS-SHE and EVITA low/medium security specs.
- Security module that is freely programmable by the customer, additional security algorithm could be implemented in software

Features:

- PowerArchitecture e200z0h core
- Secure Debugger Interface
- Cryptographic Modules with AES-128, Random Number Generator, DMA
- Sensor Interface – monitor for voltage, temperature and clock
- Secure Flash and RAM Memory for key and code storage



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MPC5748G Family Development Device

- MPC5748G will be the first device available in the our next gen BCM/Gateway family.
- This is the development or “umbrella” device for the entire family
- The MPC5748G is fully compatible with the entire Calypso family:
  - Pin Compatible
  - SW Compatible
  - Uses same enablement tools, HW tools, SW tools
- The MPC5748G is as pin compatible as possible with the Bolero family of products
- Easy migration from the MPC5748G to other members of the Calypso family

…PC5748G Key Features and Block Diagram

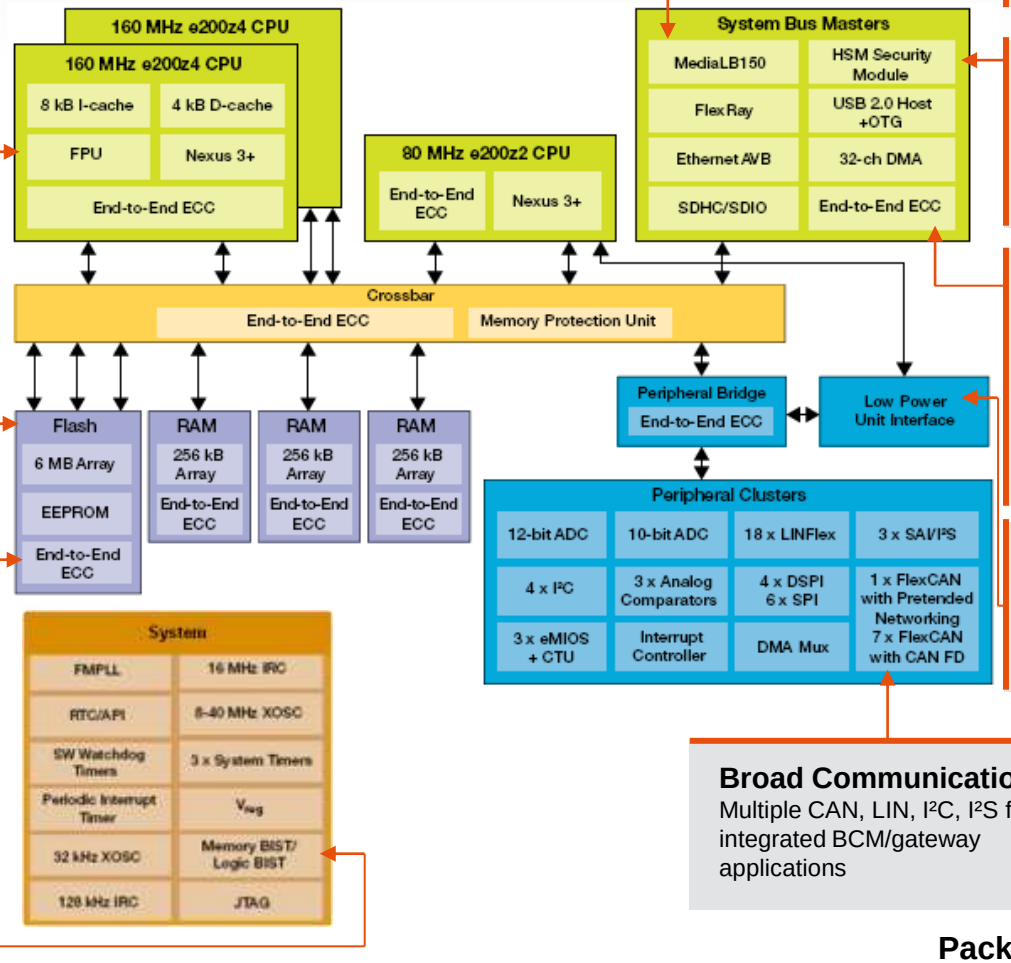
Multicore architecture:
2x e200z4 + 1x z2 Power Architecture® cores

Floating Point Unit (FPU) on z4 cores for additional computational algorithm support

High performance:
160 MHz max for z4s and 80 MHz on z2

Triple ported flash
and multiple RAM minimize access time to memory

Part of SafeAssure
functional safety program: Designed for ISO 26262 ASIL B systems



Media local bus supports MOST for infotainment domain networking

Robust security:
Hardware security module (HSM) option supports both SHE and EVITA low/medium security specs

USB 2.0 (OTG and host module) support interfacing to both wireless modems and infotainment domain

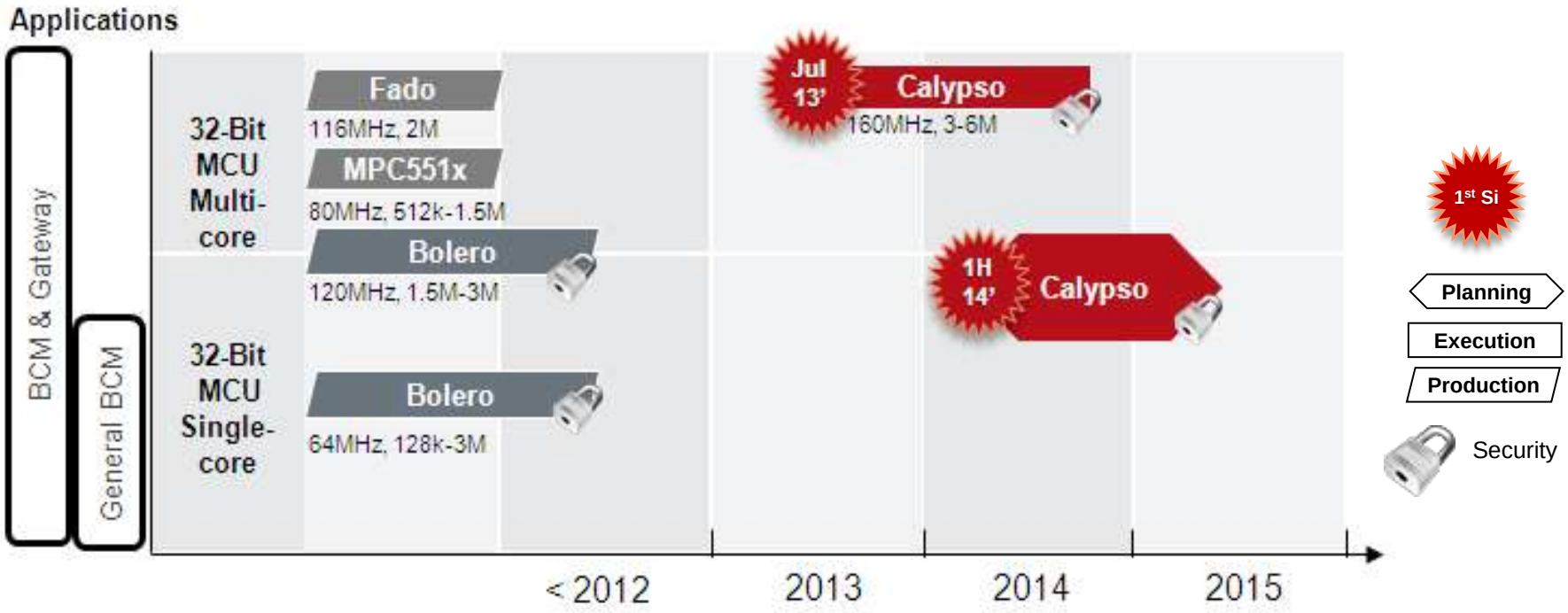
Ethernet 10/100 Mb/s for diagnostics, backbone and audio video bridging (AVB) applications

Innovative **Low-Power Unit** (LPU) provides CAN, LIN, SPI, ADC functionality in a new low power state

Broad Communications:
Multiple CAN, LIN, I²C, I²S for integrated BCM/gateway applications

Package Options:
- 176 LQFP
- 256 MAPBGA
- 324 MAPBGA

32-bit Body/Gateway MCU Roadmap



MPC5748G Family Enablement Support

- **Autosar 4.0 MCAL and OS** – Early Access Release available Sept 13'

- **Compilers**
  - Green Hills – Available Now
  - Wind River – Available in Sept 13'

- **Debuggers**
  - Lauterbach – Available Now
  - iSystem – Available in Sept 13'
  - P&E – Available Now
  - PLS – Available in Sept 13'

- **HW Development Boards**
  - Motherboard MPC574XG-MB $375
  - Daughterboards:
    - 256 BGA MPC574XG-256DS $120
    - 176 LQFP MPC574XG-176DS $120
    - 324 BGA MPC574XG-324DS $120

- **Flash Programming Tools**
  - P&E Cyclone Pro
  - Promik

Summary

- FSL has a **continued commitment** in developing **leading automotive body/gateway MCU** solutions

- **Qorivva MPC574xG MCUs** provide a highly integrated, low power, safe and secure single-chip solution for central body control and gateway applications.

- **Builds upon** the market standard **Bolero family** and **helps address next generation body/gateway needs**

Want to Learn More –

Other DwF Classes on Body Products

- AUT-T0502 - **Advanced Vehicle Networking** – Wed 4pm
- AUT-T0526 - **Brushless DC Motor Control** – Thurs 9am
- AUT-T0503 - **Functional Safety and ASIL Compliance** – Thurs 10am
- AUT-T1015 - **S12 MagniV Overview** – Thurs 2:30pm
- AUT-T1059 - **Getting Started with Multicore MCUs** – Thurs 2:30pm