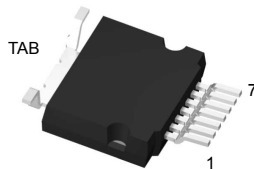
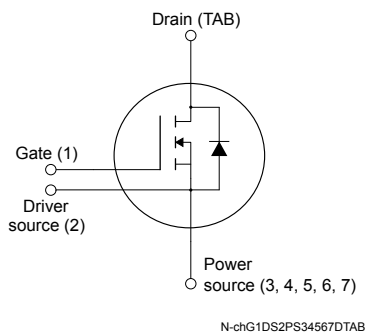


Automotive-grade N-channel 600 V, 37 mΩ typ., 54 A MDmesh DM9 Power MOSFET in an HU3PAK package



HU3PAK



Product status link

[STHU60N046DM9AG](#)

Product summary

Order code	STHU60N046DM9AG
Marking	60A046DM9
Package	HU3PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STHU60N046DM9AG	600 V	46 mΩ	54 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Worldwide best R_{DS(on)} per area among silicon-based fast recovery devices
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Excellent switching performance thanks to the extra driving source pin

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and R_{DS(on)} makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	54	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	34	
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	245	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1300	A/ μ s
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 27\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.51	$^\circ\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C/W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	775	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$		37	46	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	4698	-	pF
C_{oss}	Output capacitance		-	89	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	1058	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, open drain	-	1	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 27\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	77	-	nC
Q_{gs}	Gate-source charge		-	28	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 27\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	27	-	ns
t_r	Rise time		-	6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	68	-	ns
t_f	Fall time		-	5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		54	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		220	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 54\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 54\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	162		ns
Q_{rr}	Reverse recovery charge		-	1.1		μC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	$I_{SD} = 54\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	220		ns
Q_{rr}	Reverse recovery charge		-	2.1		μC
I_{RRM}	Reverse recovery current		-	18		A

1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

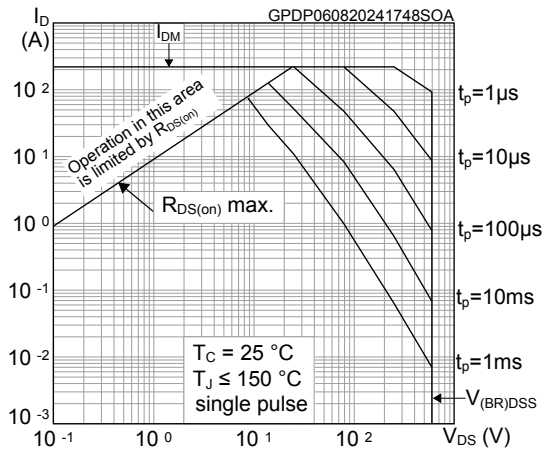


Figure 2. Maximum transient thermal impedance

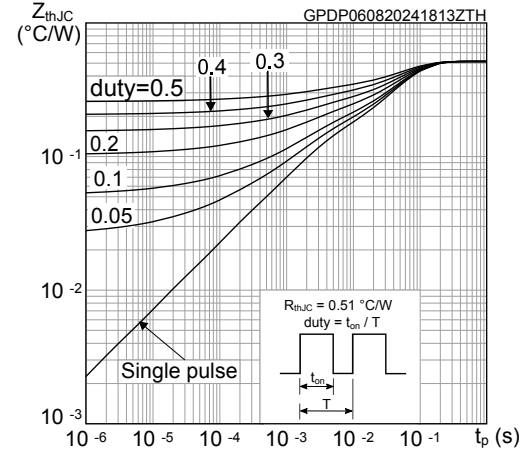


Figure 3. Typical output characteristics

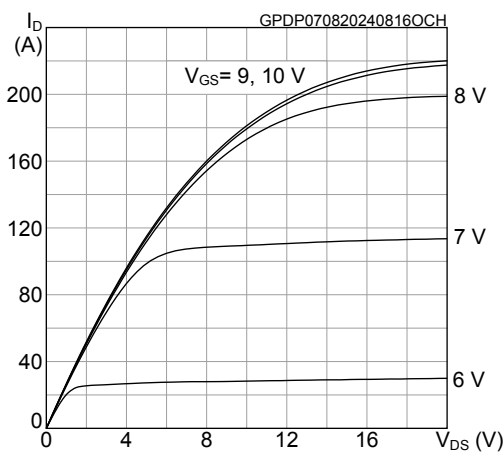


Figure 4. Typical transfer characteristics

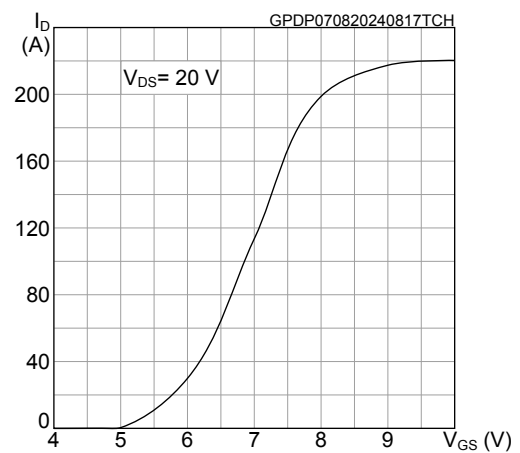


Figure 5. Typical gate charge characteristics

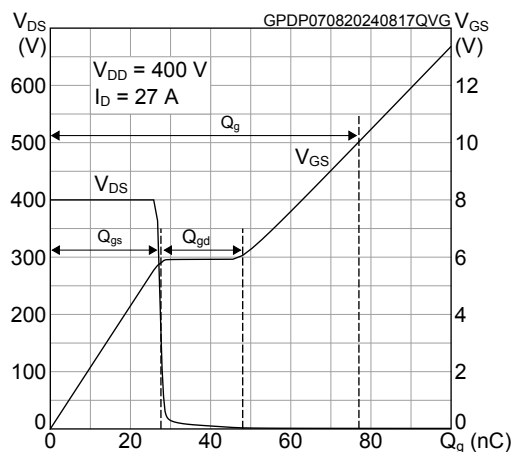


Figure 6. Typical capacitance characteristics

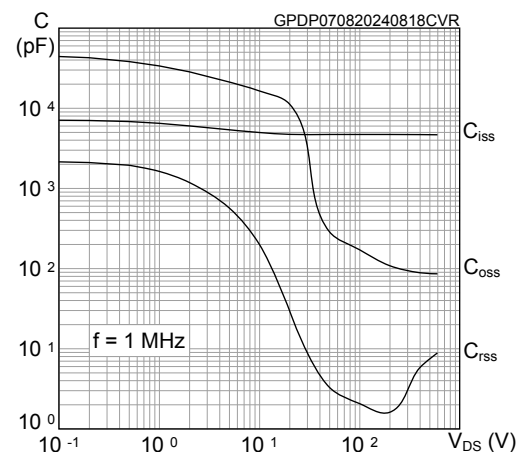


Figure 7. Typical drain-source on-resistance

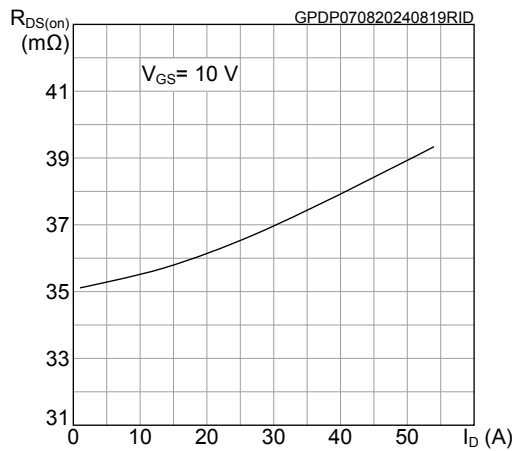


Figure 8. Normalized on-resistance vs temperature

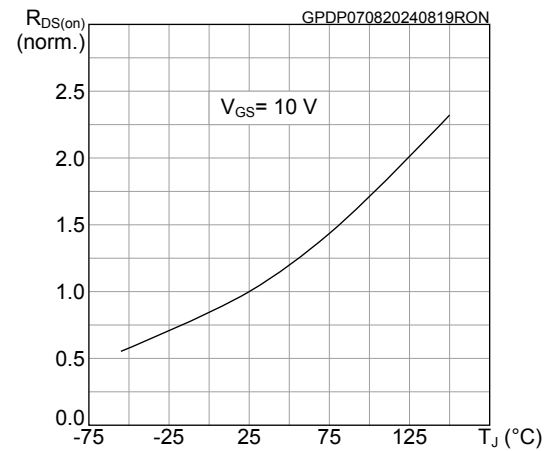


Figure 9. Normalized gate threshold vs temperature

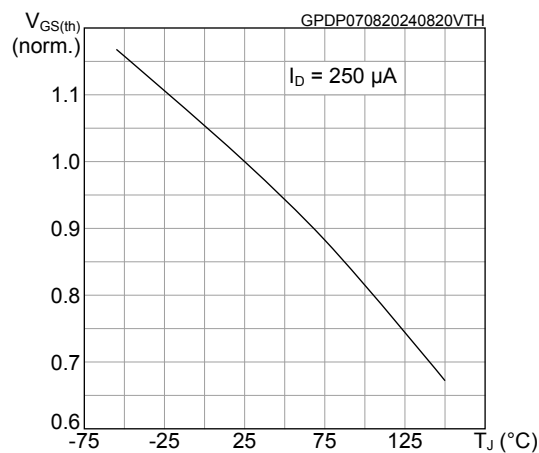


Figure 10. Normalized breakdown voltage vs temperature

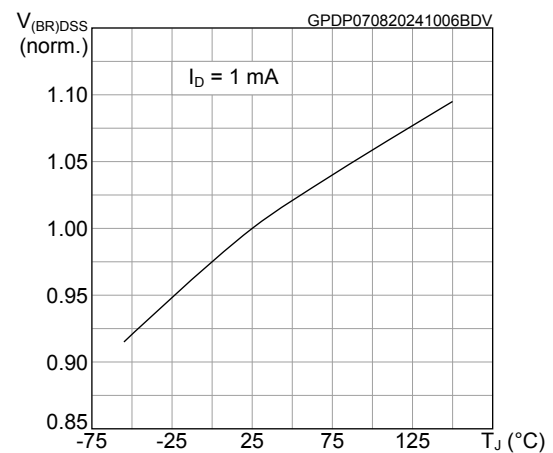


Figure 11. Typical reverse diode forward characteristics

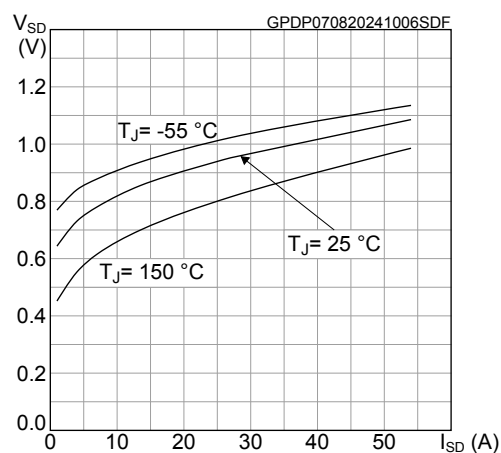
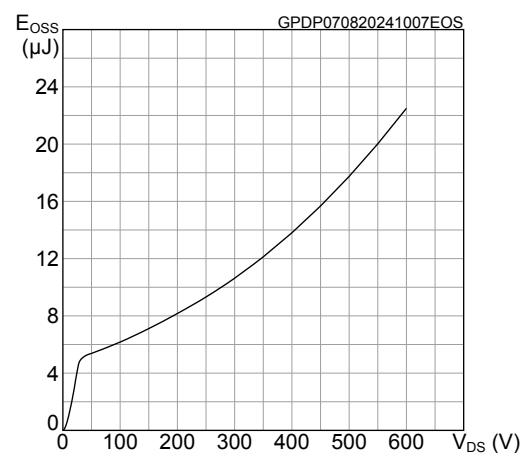
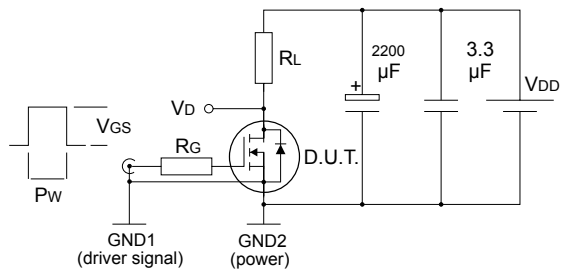


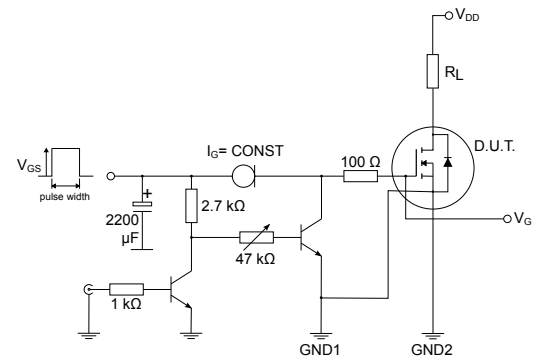
Figure 12. Typical output capacitance stored energy



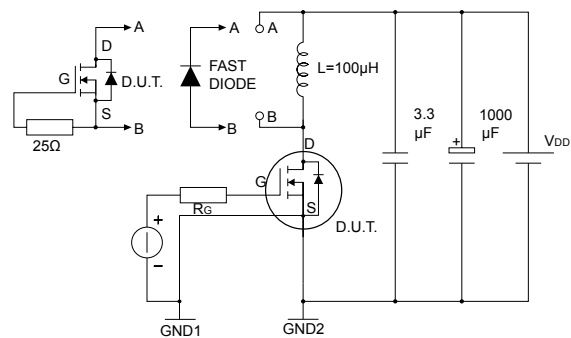
3 Test circuits

Figure 13. Switching times test circuit for resistive load


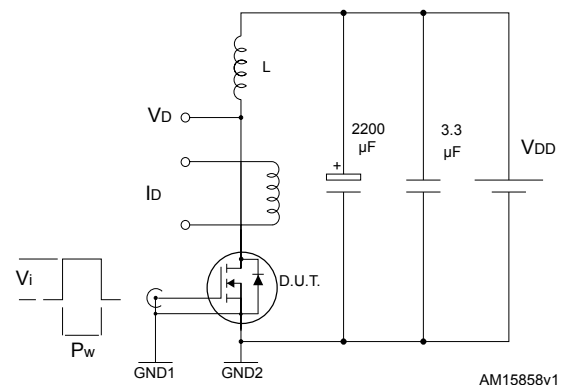
AM15855v1

Figure 14. Test circuit for gate charge behavior


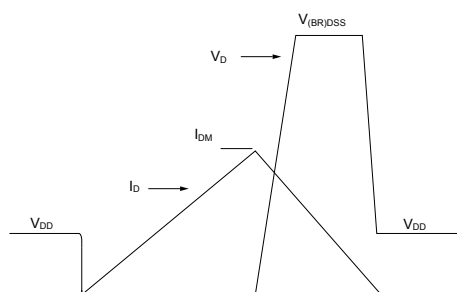
GADG180720181011SA

Figure 15. Test circuit for inductive load switching and diode recovery times


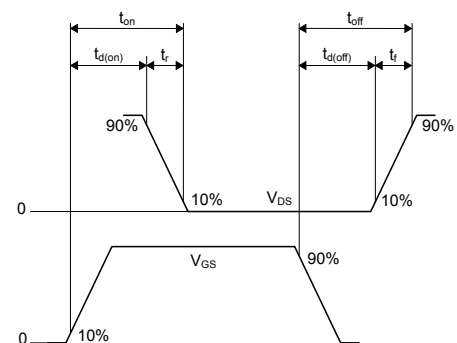
AM15857v1

Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


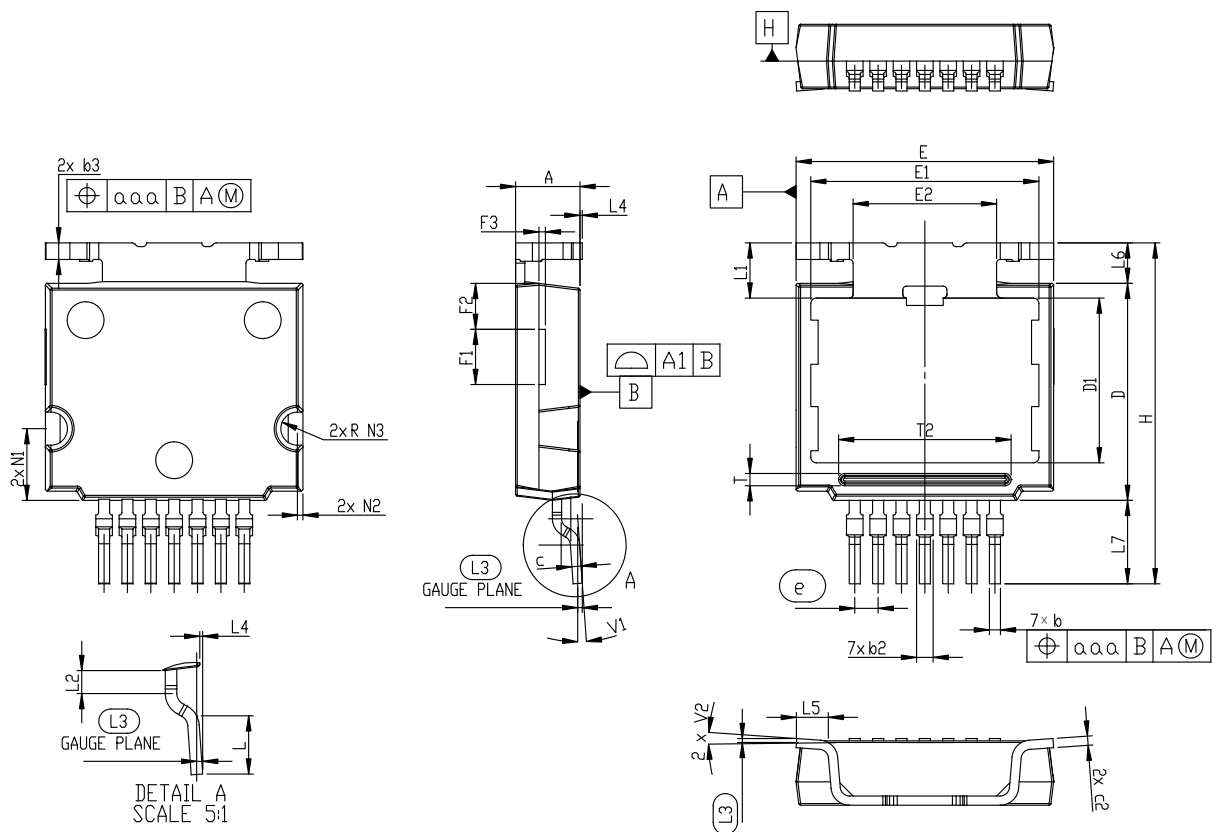
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 HU3PAK package information

Figure 19. HU3PAK package outline



DM00674007_2

Table 8. HU3PAK package mechanical data

Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
V1		0 °	8 °
V2		0 °	8 °

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions in millimeters (mm). The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 14.70
- Distance from left edge to centerline: 2.45
- Distance from centerline to right edge: 19.00

Side View Dimensions:

- Overall height: 19.00
- Distance from bottom edge to top of the main body: 1.50
- Distance from bottom edge to top of the mounting flange: 3.00
- Distance from centerline to the start of the mounting flange: 6 × 1.27
- Distance from centerline to the end of the mounting flange: 7 × 0.90

The drawing shows a central vertical axis (centerline) and a horizontal axis (top edge). The part consists of a main body with a mounting flange at the bottom and a support structure on the right side.

Figure 21. HU3PAK carrier tape outline

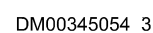
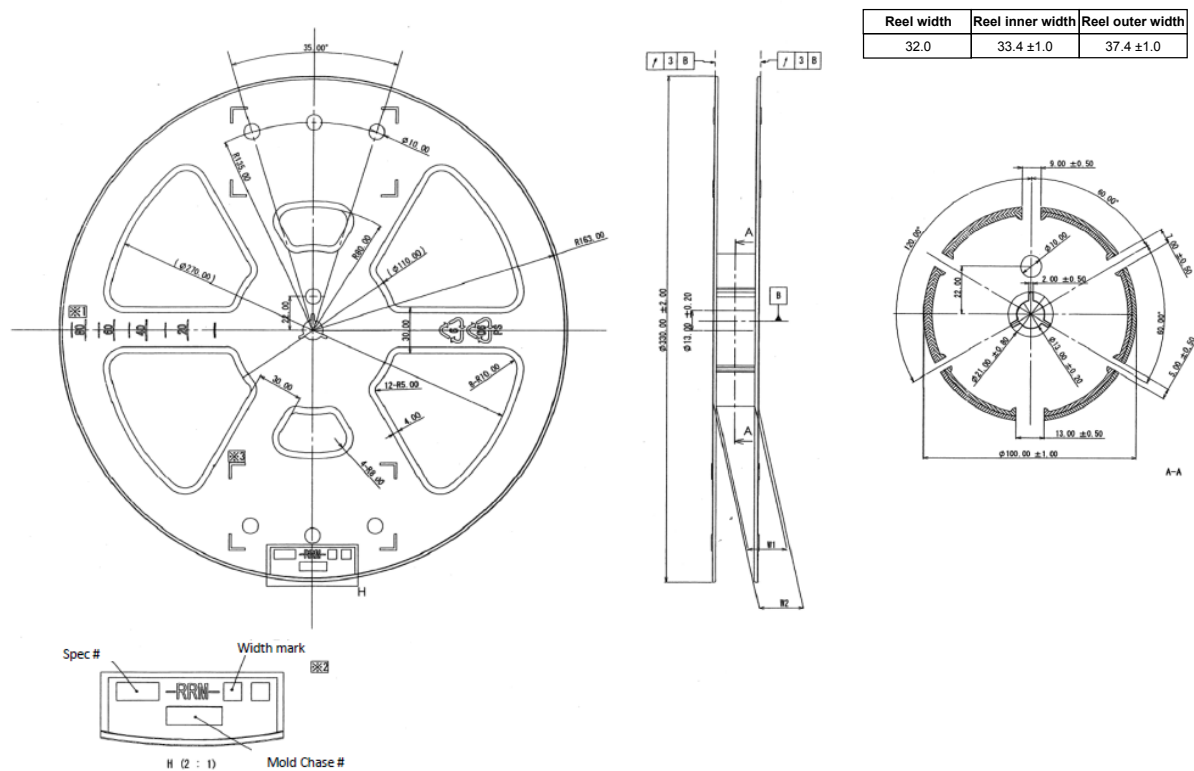


Table 9. HU3PAK tape mechanical data

Dimension	Value
	mm
A0	14.40 ±0.10
B0	19.70
D	1.50 ±0.10
E	1.75 ±0.10
F	15.65 ±0.10
I0	11.00
I1	11.60 ±0.10
I2	8.00
I3	7.00
K0	4.20
P0	4.00 ±0.10
P1	20.00 ±0.10
P2	2.00 ±0.10
T	0.40 ±0.50
W	32.00 ±0.30

Figure 22. HU3PAK reel outline (dimensions are in mm)



DM00345054_3_reel



Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Aug-2024	1	First release.

Contents

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