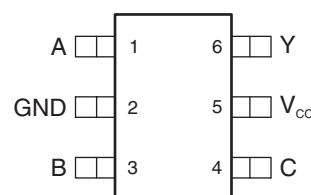


# LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE 2-INPUT SCHMITT-TRIGGER BUFFER MULTIPLEXER (NONINVERTED)

Check for Samples: [SN74AUP1T157](#)

## FEATURES

- Single-Supply Voltage Translator
- Output Level Up to Supply  $V_{CC}$  CMOS Level
  - 1.8 V to 3.3 V (at  $V_{CC} = 3.3$  V)
  - 2.5 V to 3.3 V (at  $V_{CC} = 3.3$  V)
  - 1.8 V to 2.5 V (at  $V_{CC} = 2.5$  V)
  - 3.3 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- $I_{off}$  Supports Partial Power Down ( $V_{CC} = 0$  V)
- Very Low Static Power Consumption: 0.1  $\mu$ A
- Very Low Dynamic Power Consumption: 0.9  $\mu$ A
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Pb-Free Packages Available: SC-70 (DCK) 2 x 2.1 x 0.65 mm (Height 1.1 mm)
- More Gate Options Available at [www.ti.com/littlelogic](http://www.ti.com/littlelogic)
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

DCK PACKAGE  
(TOP VIEW)


## DESCRIPTION/ORDERING INFORMATION

The SN74AUP1T157 is a single 2-input multiplexer that selects data from two data inputs (A and B) under control of a common data select input (C). The state of the common data select input determines the particular register from which the data comes. The output (Y) presents the selected data in the true (non-inverted) form.

AUP technology is the industry's lowest-power logic technology designed for use in extending battery-life in operating. All input levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V  $V_{CC}$  supply. This product also maintains excellent signal integrity (see [Figure 2](#) and [Figure 3](#)).

The wide  $V_{CC}$  range of 2.3 V to 3.6 V allows the possibility of switching output level to connect to external controllers or processors.

Schmitt-trigger inputs ( $\Delta V_T = 210$  mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

$I_{off}$  is a feature that allows for powered-down conditions ( $V_{CC} = 0$  V) and is important in portable and mobile applications. When  $V_{CC} = 0$  V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T157 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

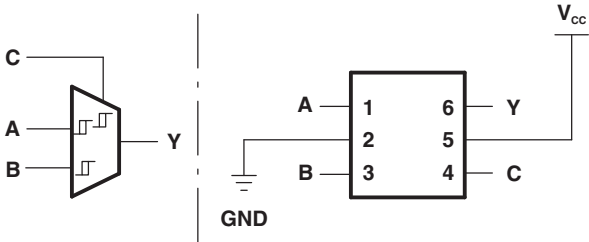
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**ORDERING INFORMATION<sup>(1)</sup>**

<b>T<sub>A</sub></b>	<b>PACKAGE<sup>(2)</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING<sup>(3)</sup></b>
–40°C to 85°C	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1T157DCKR	6L__
		Reel of 250	SN74AUP1T157DCKT	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
(3) The actual top-side marking has one additional character that designates the wafer fab/assembly site.



**Figure 1. 2-to-1 Data Selector/Multiplexer**  
**When C is L, Y = B**  
**When C is H, Y = A**

**FUNCTION TABLE**

<b>INPUTS (Lower Level Input)</b>		<b>INPUT (Select)</b>	<b>OUTPUT (V<sub>CC</sub> CMOS)</b>
<b>A</b>	<b>B</b>	<b>C</b>	<b>Y</b>
X	L	L	L
X	H	L	H
L	X	H	L
H	X	H	H

**Supply V<sub>CC</sub> = 2.3 V to 2.7 V (2.5 V)**

<b>INPUTS V<sub>T+</sub> max = V<sub>IH</sub> min V<sub>T-</sub> min = V<sub>IL</sub> max</b>		<b>OUTPUT CMOS</b>
<b>A</b>	<b>B</b>	<b>Y</b>
V <sub>IH</sub> = 1.1 V V <sub>IL</sub> = 0.35 V		V <sub>OH</sub> = 1.85 V V <sub>OL</sub> = 0.45 V

**Supply V<sub>CC</sub> = 3 V to 3.6 V (3.3 V)**

<b>INPUTS V<sub>T+</sub> max = V<sub>IH</sub> min V<sub>T-</sub> min = V<sub>IL</sub> max</b>		<b>OUTPUT CMOS</b>
<b>A</b>	<b>B</b>	<b>Y</b>
V <sub>IH</sub> = 1.19 V V <sub>IL</sub> = 0.5 V		V <sub>OH</sub> = 2.55 V V <sub>OL</sub> = 0.45 V

### LOGIC DIAGRAM (BUFFER MULTIPLEXER)

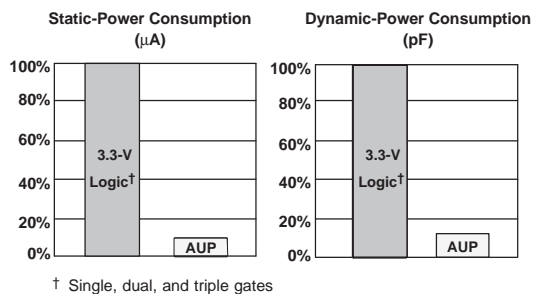
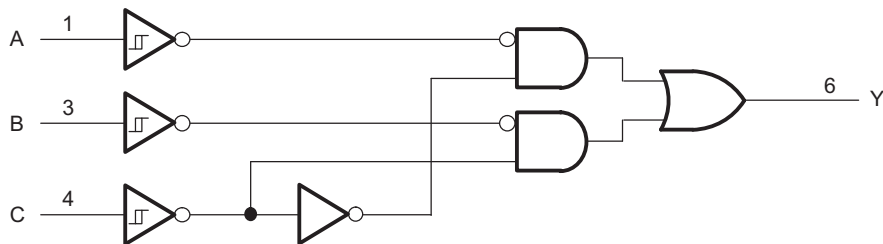


Figure 2. AUP – The Lowest-Power Family

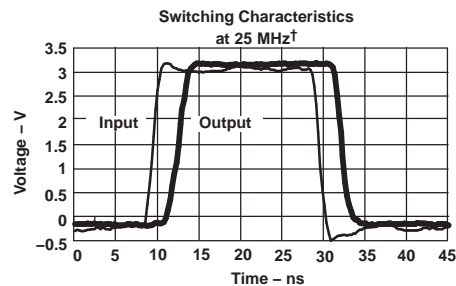


Figure 3. Excellent Signal Integrity

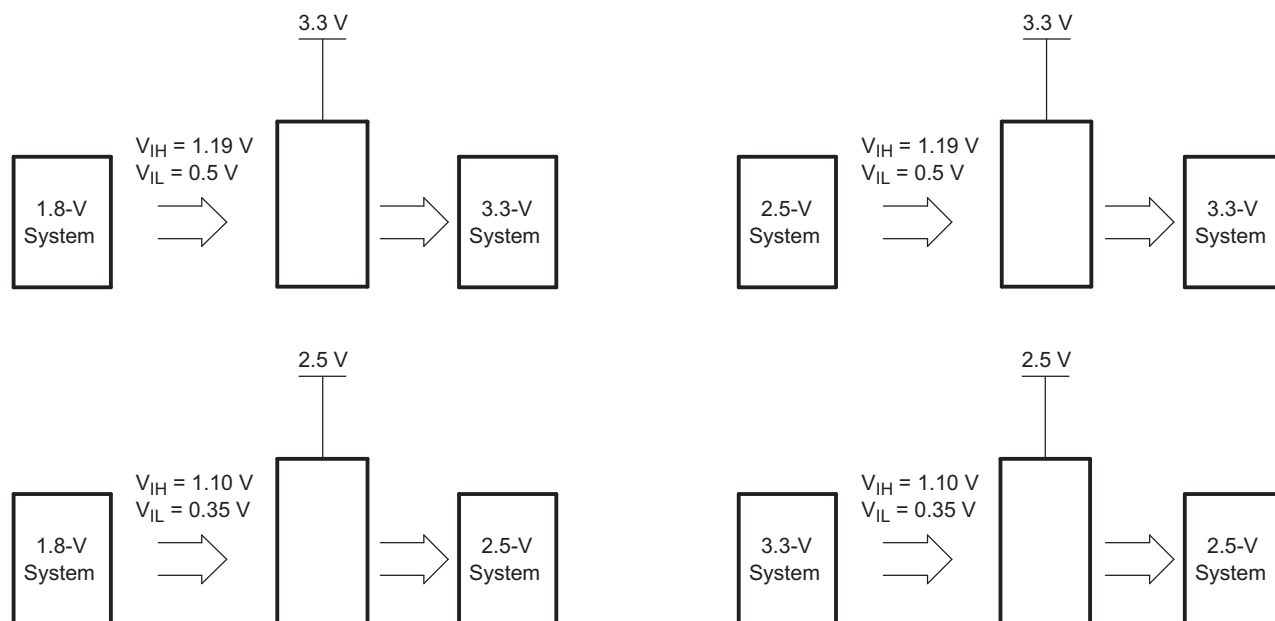
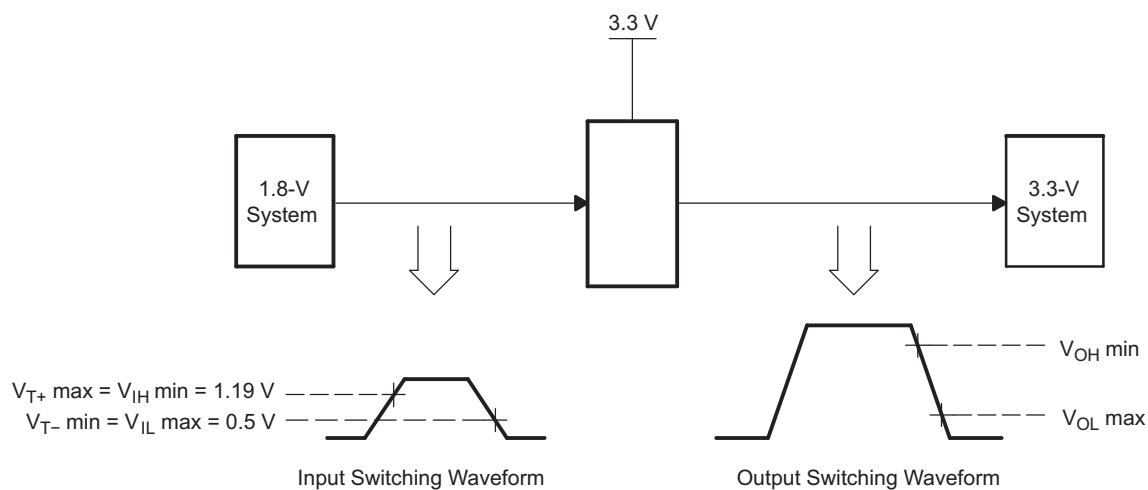


Figure 4. Typical Design Examples



**Figure 5. Switching Thresholds for 1.8-V to 3.3-V Translation**

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	4.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	4.6	V
V <sub>O</sub>	Output voltage range in the high or low state <sup>(2)</sup>	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50 mA
I <sub>O</sub>	Continuous output current		±20	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DCK package		259 °C/W
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	−3.1		mA
		V <sub>CC</sub> = 3 V	−4		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	3.1		mA
		V <sub>CC</sub> = 3 V	4		
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage			2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
			3 V to 3.6 V	0.75		1.16	0.75	1.19	
V <sub>T–</sub> Negative-going input threshold voltage			2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
			3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )			2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
			3 V to 3.6 V	0.25		0.56	0.15	0.56	
V <sub>OH</sub>		I <sub>OH</sub> = –20 μA	2.3 V to 3.6 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V
		I <sub>OH</sub> = –2.3 mA	2.3 V	2.05			1.97		
		I <sub>OH</sub> = –3.1 mA		1.9			1.85		
		I <sub>OH</sub> = –2.7 mA	3 V	2.72			2.67		
		I <sub>OH</sub> = –4 mA		2.6			2.55		
V <sub>OL</sub>		I <sub>OL</sub> = 20 μA	2.3 V to 3.6 V	0.1			0.1		V
		I <sub>OL</sub> = 2.3 mA	2.3 V	0.31			0.33		
		I <sub>OL</sub> = 3.1 mA		0.44			0.45		
		I <sub>OL</sub> = 2.7 mA	3 V	0.31			0.33		
		I <sub>OL</sub> = 4 mA		0.44			0.45		
I <sub>I</sub>	All inputs	V <sub>I</sub> = 3.6 V or GND	0 V to 3.6 V			0.1	0.5		μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.1	0.5		μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0 V to 0.2 V			0.2	0.5		μA
I <sub>CC</sub>		V <sub>I</sub> = 3.6 V or GND, I <sub>O</sub> = 0	2.3 V to 3.6 V			0.5	0.9		μA
ΔI <sub>CC</sub>		One input at 0.3 V or 1.1 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	2.3 V to 2.7 V				4		μA
		One input at 0.45 V or 1.2 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	3 V to 3.6 V				12		
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			1.5			pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			3			pF

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)  
(see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_I = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)  
(see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)  
(see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)  
(see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

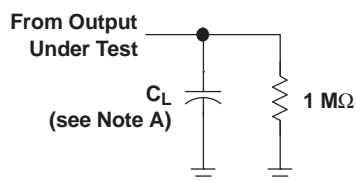
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
			TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10 \text{ MHz}$	4	5	pF

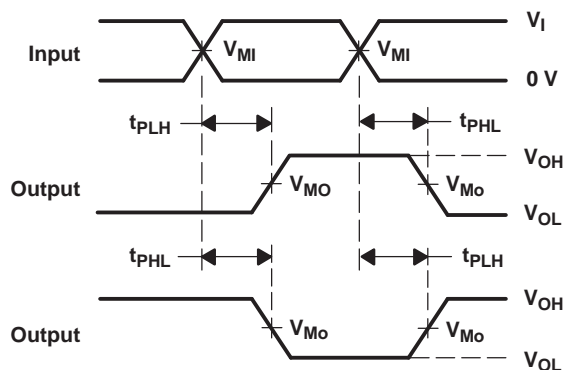


## PARAMETER MEASUREMENT INFORMATION



**LOAD CIRCUIT**

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_{MI}$	$V_I/2$	$V_I/2$
$V_{MO}$	$V_{CC}/2$	$V_{CC}/2$



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ , slew rate  $\geq 1\text{ V/ns}$ .  
 C. The outputs are measured one at a time, with one transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 6. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1T157DCKR	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6L5, 6LF)

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T157DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T157DCKR	SC70	DCK	6	3000	210.0	185.0	35.0





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

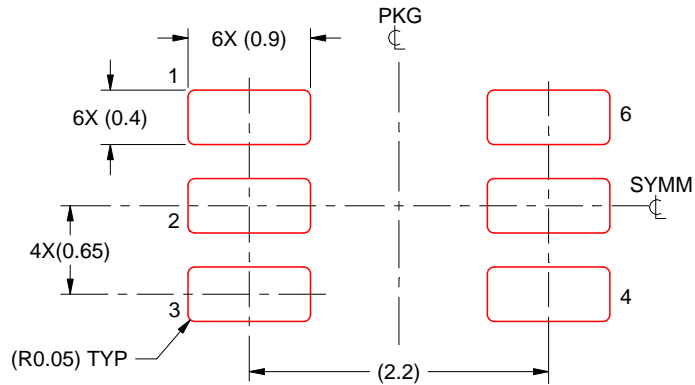


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214835/D 11/2024

#### NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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