Image Recognition Processor

TMPV760 Series

Technical Datasheet

Summary

Revision 1.1.0

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TOSHIBA CORPORATION

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Preface

The TMPV760 Series are image recognition processors that process input video images in real-time. They detect target objects such as persons, faces, hands, vehicles, traffic lanes, and so on. The series can be used for camera vision systems utilizing various image-recognition technologies such as the Advanced Driver Assistance System (ADAS), the Intelligent Transport System (ITS), surveillance cameras, gaming devices, and energy control systems for air conditioning and lighting, etc.

This document describes the specifications Summary of the TMPV760 Series.

Intended Audience

This document is intended for the following users.

- Driver software developers.
- System designers

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Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal numbers: 0xABC
  Decimal numbers: 123 or 0d123 (only when it needs to be explicitly shown that they are decimal numbers)
  Binary numbers: 0b111 (It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.)
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" when a signal moves to its active level and "deassert" to its inactive level.
- When two or more signal names are referred to, they are described as [m:n].
  Example: [3:0] shows four signal names 3, 2, 1, and 0 together.
- The characters surrounded by [] defines the register.
  Example: ***[ABCD]***
- "n" substitutes the suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written as [m:n].
  Example: Bit[3:0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit lengths.
  Byte: 8-bit
  Half word: 16-bit
  Word: 32-bit
  Double word: 64-bit
- Unless otherwise specified, the register access supports only word access.
- The registers defined as reserved must not be rewritten. Moreover, do not use the read value.
- The Properties of each bit in a register are expressed as follows.
  R: Read only
  W: Write only
  W1C: Write 1 Clear (The corresponding bit is cleared (=0) when "1" is written to this bit.)
  W1S: Write 1 Set (The corresponding bit is set (=1) when "1" is written to this bit.)
  R/W: Read and Write are possible.
  R/W0C: Read/Write 0 Clear
  R/W1C: Read/Write 1 Clear
  R/W1S: Read/Write 1 Set
  RS/WC: Read Set/Write Clear (Set after read operation, cleared after write operation)
- The value read from a bit having default value of "—" is unknown.
- When a register containing both writable bits and read-only bits is written, the read-only bits should be written with their default value. In the cases that the default is "—," follow the definition of each register.
- The reserved bits of the Write-only register should be written with their default value. In the cases in which the default is "—," follow the definition of each register.

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Terms and Acronyms

Describes some of the terms and acronyms used in this document.

- ADAS Advanced Driver Assistance System
- BCW Backward Collision Warning
- BIST Built-In Self Test
- CAN Controller Area Network
- CAN FD CAN Flexible Data-rate
- CoHOG Co-occurrence Histograms of Oriented Gradients
- CoHD Co-occurrence Histograms of color Differences
- CoHED Co-occurrence Histograms of pairs of Edge orientations and color Differences
- CPU Central Processing Unit
- CSI-2 Camera Serial Interface
- CTS Clear To Send
- CVBS Composite Video Blanking and Sync
- DMA Direct Memory Access
- DMAC DMA Controller
- DPG Delayed Pulse Generator
- DRAM Dynamic Random Access Memory
- D-Cache Data Cache
- D-RAM Data RAM
- FCW Forward Collision Warning
- FIFO First In First Out
- GT General Timer
- GTI General purpose Timed Input
- GTO General purpose Timed Output
- HOG Histograms of Oriented Gradients
- I^2C Inter-Integrated Circuit
- I^2S Inter-IC Sound
- ICE In-Circuit Emulator
- ITS Intelligent Transport Systems
- IVC2F Image recognition VLIW Coprocessor 2 with Floating-point unit
- I-Cache Instruction Cache
- I-RAM Instruction RAM
- JTAG Joint Test Action Group
- LCA Lane Change Assistance
- LDW Lane Departure Warning
- LPDDR2 Low Power Double Data Rate 2
- L2-Cache Level 2 Cache
- MeP Media embedded Processor
- MCU Micro Controller Unit
- MIPI® Mobile Industry Processor Interface
- MMU Memory Management Unit
- MPE Media Processing Engine
- NMI Non Maskable Interrupt
- P-FBGA Plastic Fine pitch Ball Grid Array
- P-LFBGA Plastic Low-profile Fine pitch Ball Grid Array
- PCM Pulse Code Modulation
- PHY Physical Layer

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- PLL Phase Locked Loop
- PWM Pulse Width Modulation
- QVGA Quarter Video Graphics Array
- RISC Reduced Instruction Set Computer
- RTS Request To Send
- SDK Software Development Kit
- SDRAM Synchronous Dynamic Random Access Memory
- SfM Structure from Motion
- SIMD Single Instruction stream, Multiple Data stream
- SPI Serial Peripheral Interface
- SRAM Static Random Access Memory
- SXGA Super eXtended Graphics Array
- TSR Traffic Sign Recognition
- UART Universal Asynchronous Receiver Transmitter
- VENEZIA Vision ENabling Engine / Zen-Inspired Architecture
- VLIW Very Long Instruction Word
- WVGA Wide Video Graphics Array

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1. Overview

1.1. Overview of TMPV760 Series

The TMPV760 Series is an image recognition processor that performs real-time image processing of input video image data from a camera or cameras, recognizes target objects such as humans, faces, hands, vehicles, traffic lanes, traffic signs, text and so on, or the movement of the above objects. The TMPV760 Series is suitable for camera-based vision systems such as the advanced driver assistance system (ADAS), intelligent transport systems (ITS), surveillance camera, air-conditioner / light control system and so on.

TMPV760 Series provide a lineup of products in different configuration. (For details about a configuration of each product, refer to “1.3. Product List”).

The TMPV760 Series is a Heterogeneous multi-core architecture consisting of “control CPU(s)," multi-core sub-system “VENEZIA (Vision Enabling Engine / Zen-Inspired Architecture)” which has multiple sets of “MPE (Media Processing Engine)” suitable for image processing and multiple image processing accelerators. The TMPV760 Series deliver high image processing performance under low power consumption. Up to eight image recognition application can be executed in parallel by having two “VENEZIA.”

The control CPU consists of two Toshiba original 32-bit RISC cores “MeP (Media embedded Processor).”

VENEZIA has four MPE sets that implement a “MeP” core and an “IVC2F (the 2nd generation of Image recognition VLIW Coprocessor with FPU),” enabling parallel execution of up to four image recognition applications per one multi-core sub system. The IVC2 enables SIMD (Single Instruction stream, Multiple Data stream) technology for simultaneous operations on multiple sets of data with a single instruction required for image processing and VLIW (Very Long Instruction Word) technology to issue multiple instructions as a combined instruction. In addition, a double-precision floating point number is supported.

The TMPV760 Series has the following eight types of "image processing accelerators."

(1) **Affine Transformation Accelerator**
Correction of lens distortion of input image data from a camera, geometric transformation such as rotation, expansion/dilation, translation, and shear.

(2) **Pyramid Accelerator**
Generation of a reduction image by reducing image data at an arbitrary ratio.

(3) **Histogram Accelerator**
Histogram calculation, brightness conversion of image data are performed using lookup table.

(4) **HOG (Histograms of Oriented Gradients) Accelerator**
Calculation of HOG or Toshiba CoHOG (Co-occurrence Histograms of Oriented Gradients) features and likelihood score output by using LSVM (Linear Support Vector Machine) with templates for human recognition

(5) **Enhanced CoHOG Accelerator**
Determination whether a person or not is processed by the linear support vector machine based on the histogram of the feature amount using color information, in addition to luminance gradient orientation.

(6) **Filter Accelerator**
Various types of filtering processing such as noise reduction and edge detection, and color space conversion are performed.

(7) **Matching Accelerator**
Performs parallax calculation of the left/right image data of a stereo camera, and tracks and detects movement of a template.

(8) **SfM (Structure from Motion) Accelerator**
The three-dimensional coordinate of a still object is calculated from an input image of a plurality of consecutive frames of a single-lens camera.

The TMPV760 Series has a huge on-chip memory for image data processing. There are six sets of 256 KB working RAMs, which enables it to access simultaneously image data from up to six bus masters (processors, accelerators, video input/output interfaces, etc.).

In addition, The TMPV760 Series offers video input interface, video output interface, external memory interface such as SRAM/NOR memory controller and DDR SDRAM controller, system RAM for control CPU (MeP), system ROM for booting of MeP, interrupt controller, general-purpose I/O, timer, serial interface (UART, I2C and

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SPI), PCM interface, CAN interface, and MCU interface for connecting to external MCU through a parallel bus.

1.2. Highlights

The key points of the TMPV760 Series are high image processing performance, low power consumption, and easy software development.

Heterogeneous multi-core architecture: The TMPV760 Series is a Heterogeneous multi-core architecture that combines different type of engines such as control CPU(s) designed for easy software development, a multi-core sub-system designed for executing multiple image processing applications and solving various image recognition algorithms by software, and image processing accelerators designed for helping real-time image processing. This architecture delivers a high image processing performance under low power consumption, along with easy software development.

- **Control CPU**
  The TMPV760 Series has a two 32-bit RISC CPU core (Toshiba original MeP-c5) as the control CPU.
- **Multi-grain parallelism architecture Multi-core Sub-system**
  The TMPV760 Series has two Toshiba original multi-core sub-system "VENEZIAs." The VENEZIA is a multi-grain parallelism architecture – application level (multi-core), instruction level (VLIW) and data level (SIMD).
  The VENEZIA includes 4 sets of Toshiba original media processing engines "MPE" that enable simultaneous execution of up to four image recognition applications. Each MPE has a Toshiba original 32-bit RISC CPU core MeP-c5 and an image recognition coprocessor IVC2F. The MPE is a 3-way VLIW machine that can issue up to 3 instructions (one CPU instruction and up to 2 coprocessor instructions). The IVC2 provides SIMD instructions for simultaneous operations on eight sets of 8-bit data, four sets of 16-bit data, two sets of 32-bit data, and a double-precision floating point number. The IVC2 can execute simultaneously up to 2 SIMD instructions. Since parallel processing of two instructions is enabled, operations on a maximum of 16 sets of 8-bit data can be processed simultaneously.
- **Accelerators to help real-time image processing**
  The TMPV760 Series is included with a maximum of eight types of image processing accelerators. (A type of a built-in image processing accelerator and the number of channels are different for each of the product.) Toshiba provides the TMPV760 Series Software Development Kit (SDK) including various image processing libraries and drivers for easy use of these image processing accelerators.

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1.3. Product List

The TMPV760 Series provide a lineup of products in different configuration. For details about a configuration of each product, refer to “Table 1.1 Product List.”

Table 1.1 Product List

Module Name	TMPV760 Series	
	TMPV7608XBG	TMPV7602XBG
Control MeP	CPU × 2	
VENEZIA	(MPE × 4) × 2	(MPE × 4) × 1
Affine Transformation Accelerator	3ch	2ch
Pyramid Accelerator	2ch	
Histogram Accelerator	1ch	2ch
HOG Accelerator	1ch	2ch
Enhanced CoHOG Accelerator	2ch	1ch
Filter Accelerator	2ch	
Matching Accelerator	2ch	
SfM Accelerator	1ch	—
Video Input Interface	4ch (Inputs are selected from the parallel input 4ch max and MIPI CSI-2 input 4ch max.)	1ch (Inputs are selected from the parallel input and MIPI CSI-2 input)
Video Output Interface	2ch	1ch
SRAM/NOR Memory Controller	16-bit bus, 24-bit address × 2 chip select	16-bit bus, 8-bit address × 1 chip select
Serial NOR Memory Controller	4-bit SPI, 2 chip select	4-bit SPI, 1 chip select
DDR SDRAM Controller	LPDDR2-800 32-bit × 2 × 2ch	LPDDR2-800 32-bit × 2 × 1ch
Working RAM	256 Kbytes × 6	
System RAM	96 Kbytes × 1	
System ROM	80 Kbytes × 1	
Global DMA Controller (between memory and memory)	2 channels	
Peripheral DMA Controller (between peripheral and memory)	3 channels	
General-purpose I/O	max 24 bits	max 16 bits
Timer	max 4 channels	
UART interface	max 4 channels + 1 channel (for debugging)	
I2C interface	max 8 channels	max 4 channels
SPI interface	max 4 channels	
PCM interface	Input 1 channel and output 1 channel	
CAN interface	max 3 channels	max 2 channels
CAN FD interface	—	max 2 channels
MCU interface	8-bit bus	
CRC arithmetic unit	1 channel	
Power Management Unit	—	1 channel
Operating frequency	max 266.7 MHz (Control MeP, VENEZIA)	
Package	796-pin PBGA 27 × 27 mm Ball Pitch 0.8 mm	521-pin PBGA 17 × 17 mm Ball Pitch 0.65 mm

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1.4. Module Name Abbreviations

In this document, the following abbreviated expressions are used for the module name.

Table 1.2 Abbreviated Module Names

Module Name	Abbreviated Expression
Control MeP	CMEP (CMEP0, CMEP1)
VENEZIA	VENEZIA (VENEZIA0, VENEZIA1)
Media Processing Engine	MPE (MPE0, MPE1, MPE2, MPE3, MPE4, MPE5, MPE6, MPE7)
Affine Transformation Accelerator	AFFINE (AFFINE0, AFFINE1, AFFINE2)
Pyramid Accelerator	PYRAMID (PYRAMID0, PYRAMID1)
Histogram Accelerator	HIST (HIST0, HIST1)
HOG Accelerator	HOG (HOG0, HOG1)
Enhanced CoHOG Accelerator	Enhanced CoHOG (Enhanced CoHOG0, Enhanced CoHOG1)
Filter Accelerator	FILTER (FILTER0, FILTER1)
Matching Accelerator	MATCH (MATCH0, MATCH1)
SfM Accelerator	SFM
Video Input Interface	VIIF (VIIF0, VIIF1, VIIF2, VIIF3)
Video Output Interface	VOIF (VOIF0, VOIF1)
SRAM/NOR Memory Controller	MEMC
Serial NOR Memory Controller	NORC
DDR SDRAM Memory Controller	DDRC (DDRC0, DDRC1)
System ROM	SROM
System RAM	SRAM
Working RAM	WRAM (WRAM0, WRAM1, WRAM2, WRAM3, WRAM4, WRAM5)
Interrupt Controller	INTC
Global DMA Controller	GDMAC (GDMAC0, GDMAC1)
Peripheral DMA Controller	PDMAC (PDMAC0, PDMAC1, PDMAC2)
General-purpose I/O	GPIO
Timer	TIMER
UART Interface	UART (UART0, UART1, UART2, UART3, UART4 (DBGUART))
I2C Interface	I2C (I2C0, I2C1, I2C2, I2C3, I2C4, I2C5, I2C6, I2C7)
SPI Interface	SPI (SPI0, SPI1, SPI2, SPI3)
PCM Interface	PCMIF
CAN Interface	CAN (CAN0, CAN1, CAN2)
CAN FD Interface	CANFD (CANFD0, CANFD1)
MCU Interface	MCUIF
CRC arithmetic unit	CRC
Power Management Unit	PMU
Performance Monitor	PFMON
Parity	PARITY
Software Triggered BIST	STBIST

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1.5. Block Diagram

1.5.1. TMPV7608XBG

"Figure 1.1 TMPV7608XBG Block Diagram" shows the block diagram of TMPV7608XBG.

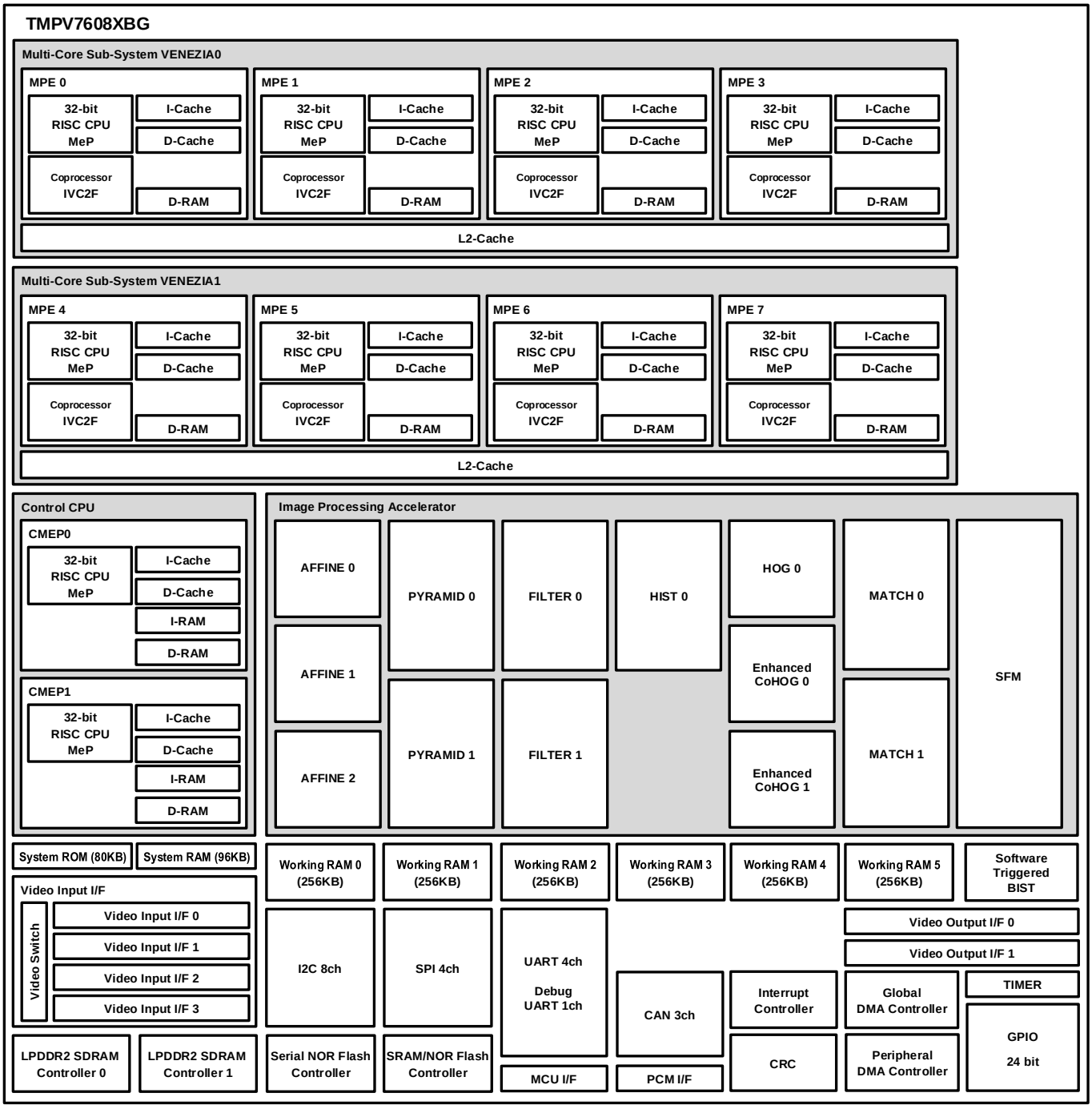

Figure 1.1 TMPV7608XBG Block Diagram

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1.5.2. TMPV7602XBG

"Figure 1.2 TMPV7602XBG Block Diagram" shows the block diagram of TMPV7602XBG.

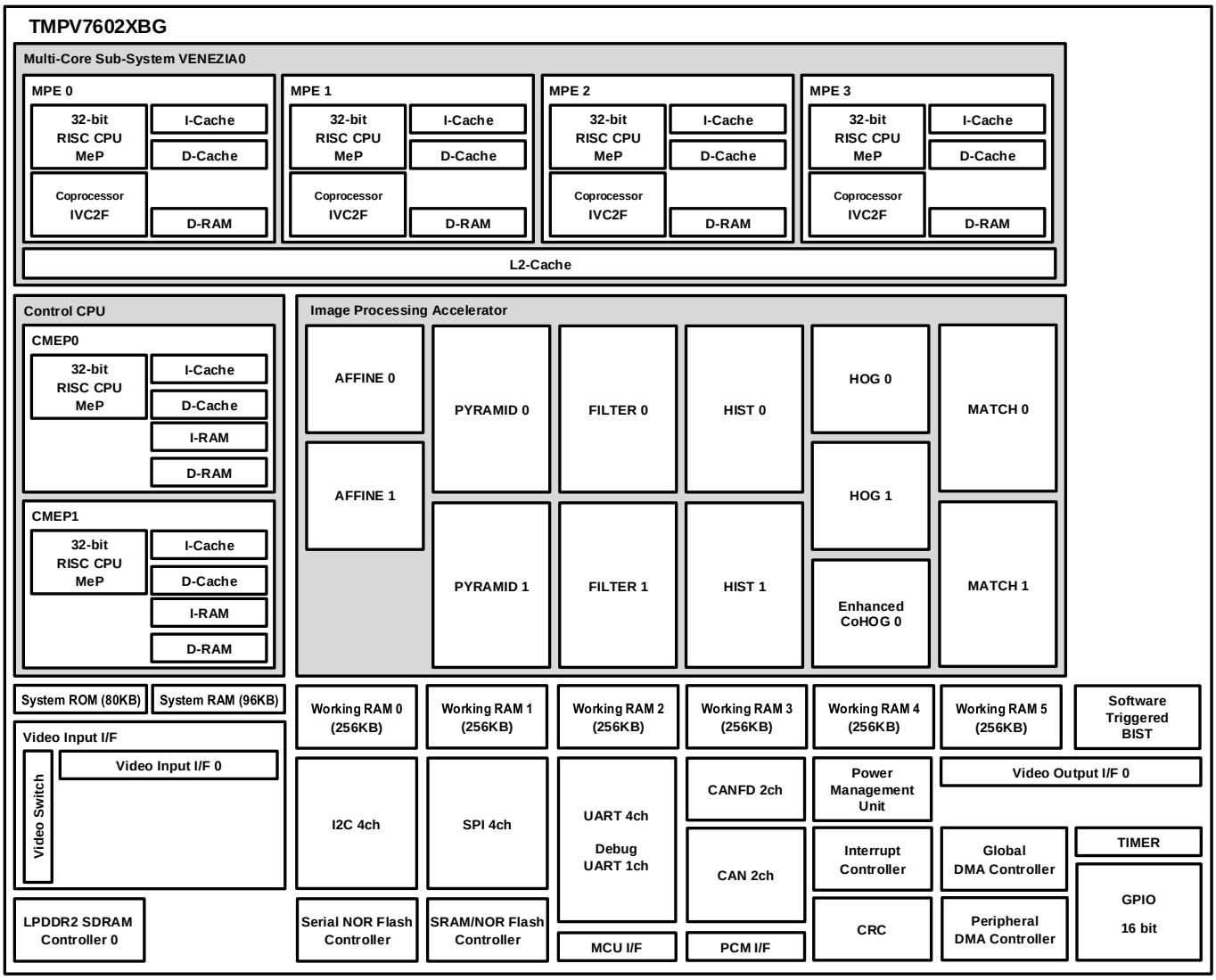

Figure 1.2 TMPV7602XBG Block Diagram

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1.6. Applications

The following are the major target applications for the TMPV760 Series.

- Automotive
  - Advanced Driver Assistance System (ADAS)
    - Lane Departure Warning (LDW) System
    - Forward Collision Warning (FCW) System
    - Backward Collision Warning (BCW) System
    - Traffic Sign Recognition (TSR) System
    - Forward Pedestrian Collision Warning System
      (The system for nighttime is referred to as Night Vision)
    - Backward Pedestrian Collision Warning or Back Over Prevention System
    - Lane Change Assistance (LCA) System
    - Driver Authentication System
    - Driver Monitoring System
    - Parking Assistance (Top View) System
    - Electric Side Mirror System
    - Electric Rearview Mirror System
    - Sway Warning System
    - Lead Car Departure Notification System
    - Red Light Detection Alarm System
    - Road Marking Recognition System
- Industrial
  - Intelligent Transport Systems (ITS)
  - Parking management system
  - Entrance management system
  - Surveillance camera
  - Machine vision
  - Air conditioning/lighting control system
  - Digital signage
- Consumer
  - Motion sensor
  - System used camera-based user interface (Games, Toys etc.)
  - Video contents management system
  - Home Security System

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1.6.1. Advanced Driver Assistance Systems Example 1: Forward- / Rear Blind Spot- /Backward-View Monitoring

Users can use the Advanced Driver Assistance Systems which assist drivers by providing information on the front, rear and rear blind spots of a vehicle with a single or a stereo camera system.

The following applications are available as “Forward-View Monitoring” by using a front-view camera facing forward.

- Lane Departure Warning (LDW) system
  The detection of traffic lane, and warns a driver if a vehicle is departing from a traffic lane without having made any indication of lane changing.
- Forward Collision Warning (FCW) system
  The detection of preceding vehicles, and warns of a hazard if there is a possibility of a collision.
- Forward Pedestrian Collision Warning (FPCW) system
  The detection of pedestrians in front of a vehicle, and warns a driver if there is a possibility of a collision.
- Traffic Sign Recognition (TSR) system
  This warns of a hazard for a driver when the traffic signs are detected and recognized.

The following applications are available as “Rear-View Monitoring” by using a rear-view camera facing toward the back.

- Lane Departure Warning (LDW) system
- Backward Collision Warning (BCW) system
  This detects overtaking vehicles and warns a driver if there is a possibility of a collision.
- Back Over prevention system
  This detects pedestrians behind a car.
- Lane Change Assistance (LCA) system
  This detects approaching vehicles from behind, and assists to change lane.

The following applications are available as “Rear Blind Spot Monitoring” using two single cameras attached to the side mirrors.

- Lane Departure Warning (LDW) system
- Lane Change Assistance (LCA) system
- Roll Warning system
  When vehicles turn to the right or left, this system warns a driver to prevent hitting a pedestrian or a bicycle.

The TMPV760 Series is capable of working some application at the same time.

In addition, when identify a person at night, use low light intensity and high sensitivity visible light cameras, near infrared cameras or far infrared cameras.

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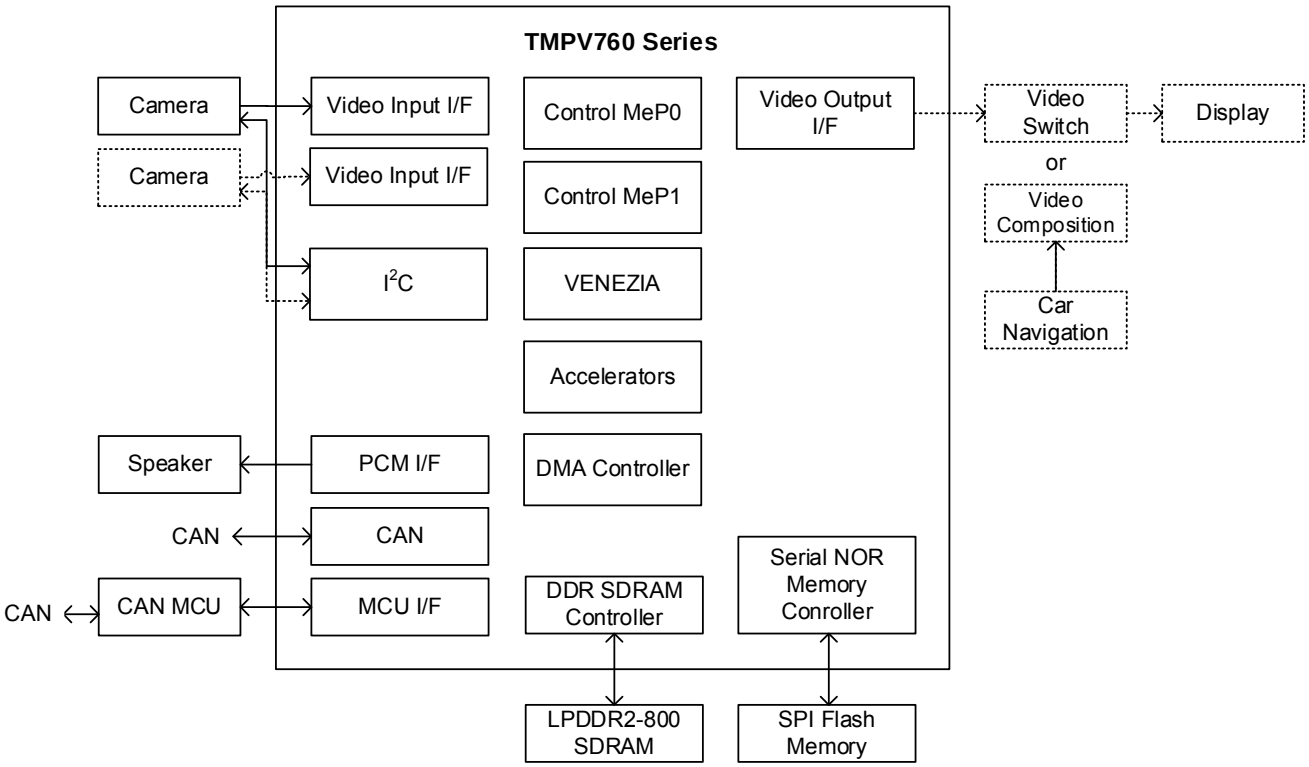

Figure 1.3 Example of Forward/Rear-View Monitoring System

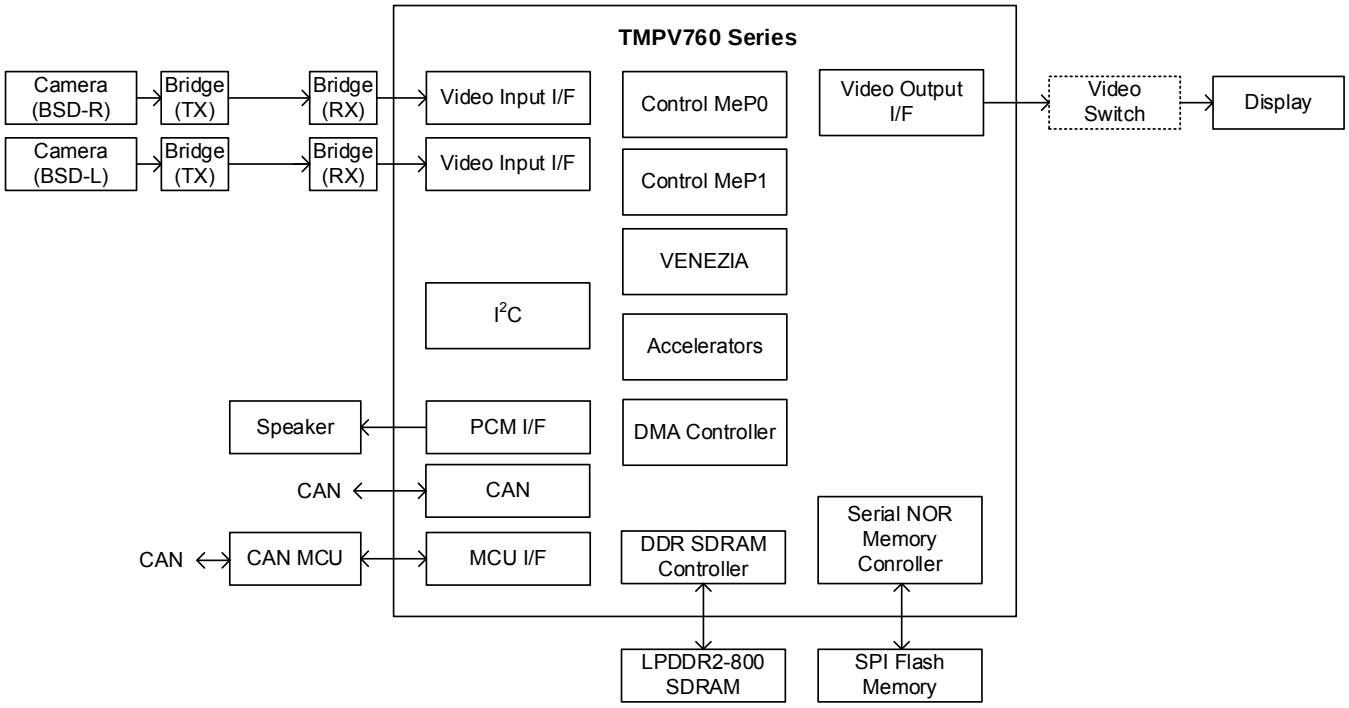

Figure 1.4 Example of Rear Blind Spot Monitoring System

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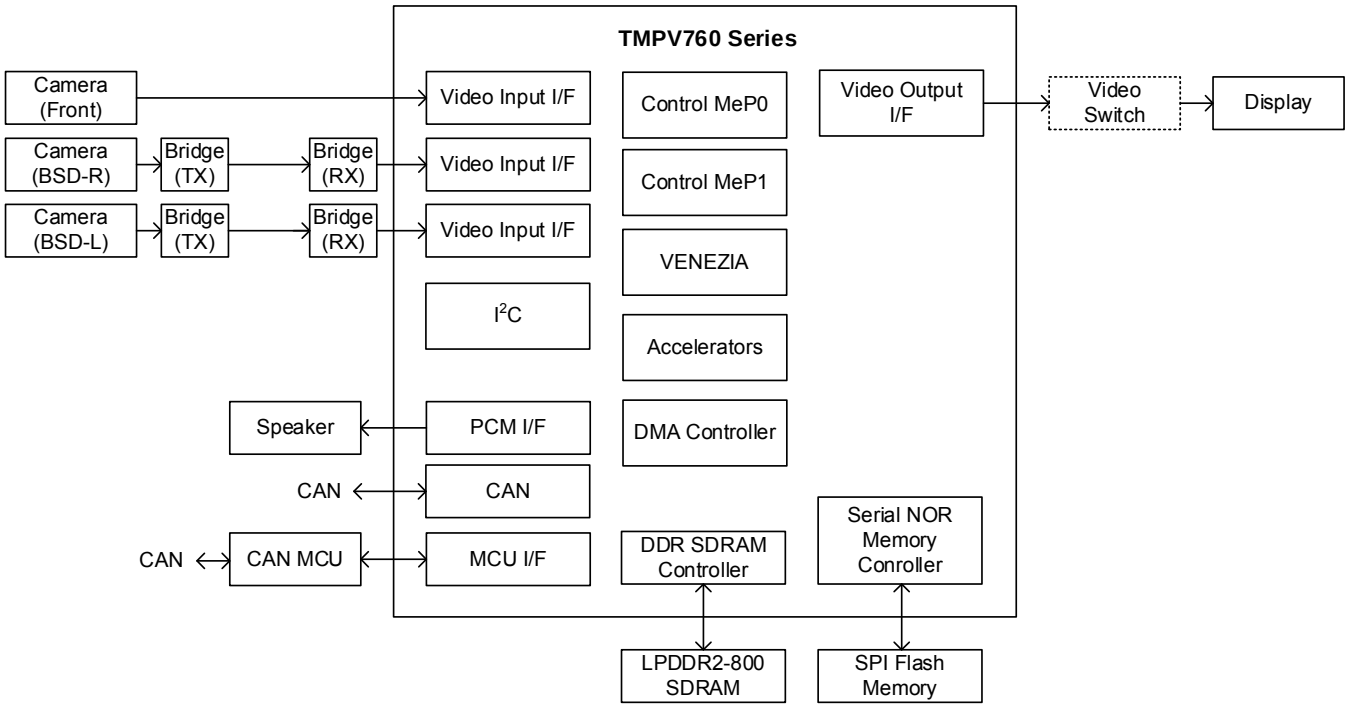

Figure 1.5 Example of Forward/Rear Blind Spot Monitoring System

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1.6.2. Advanced Driver Assistance Systems Example 2: Surround Monitoring

Forward, backward, left, and right pictures of vehicles are taken by using four fisheye cameras. These correct the distortion of lenses and change the viewing point. Corrected pictures and the top view of vehicles are composed. Monitored pictures from the top view point for the vehicle and its surroundings are synthesize and displayed on an LCD panel.

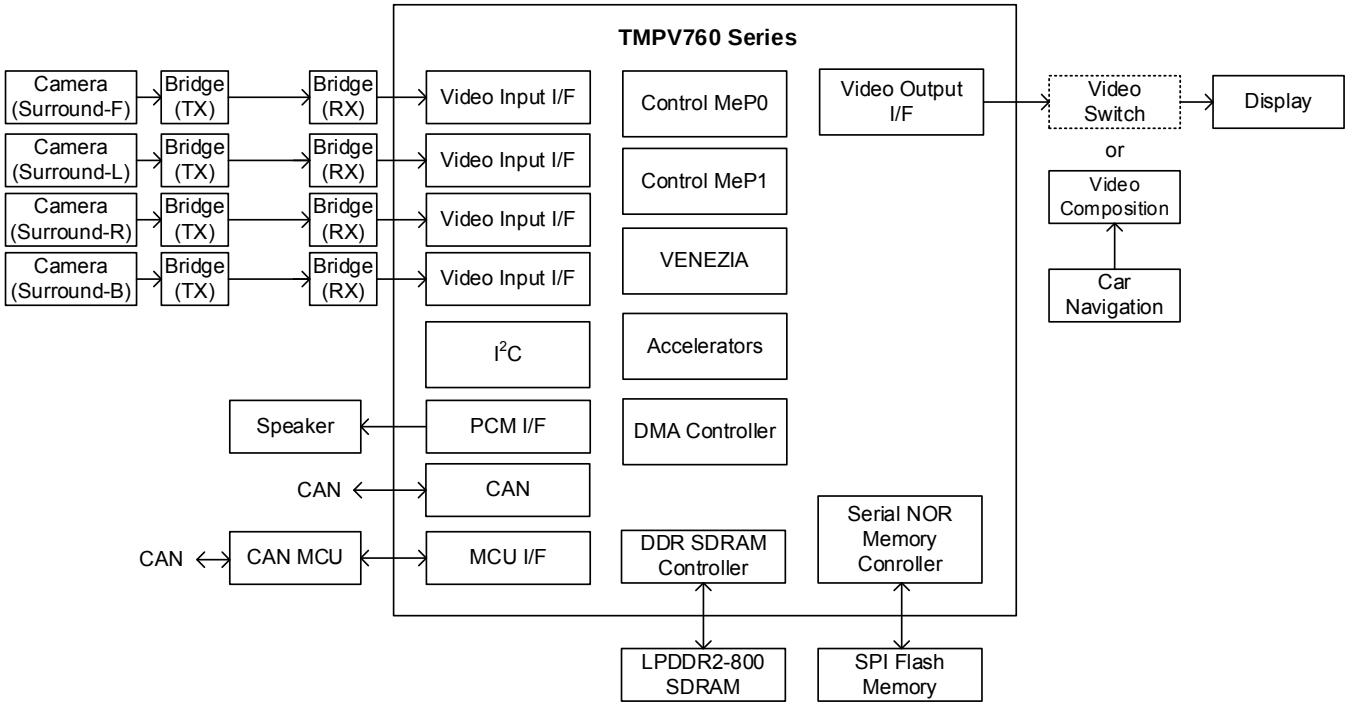

Figure 1.6 Example of Surrounding Monitoring System

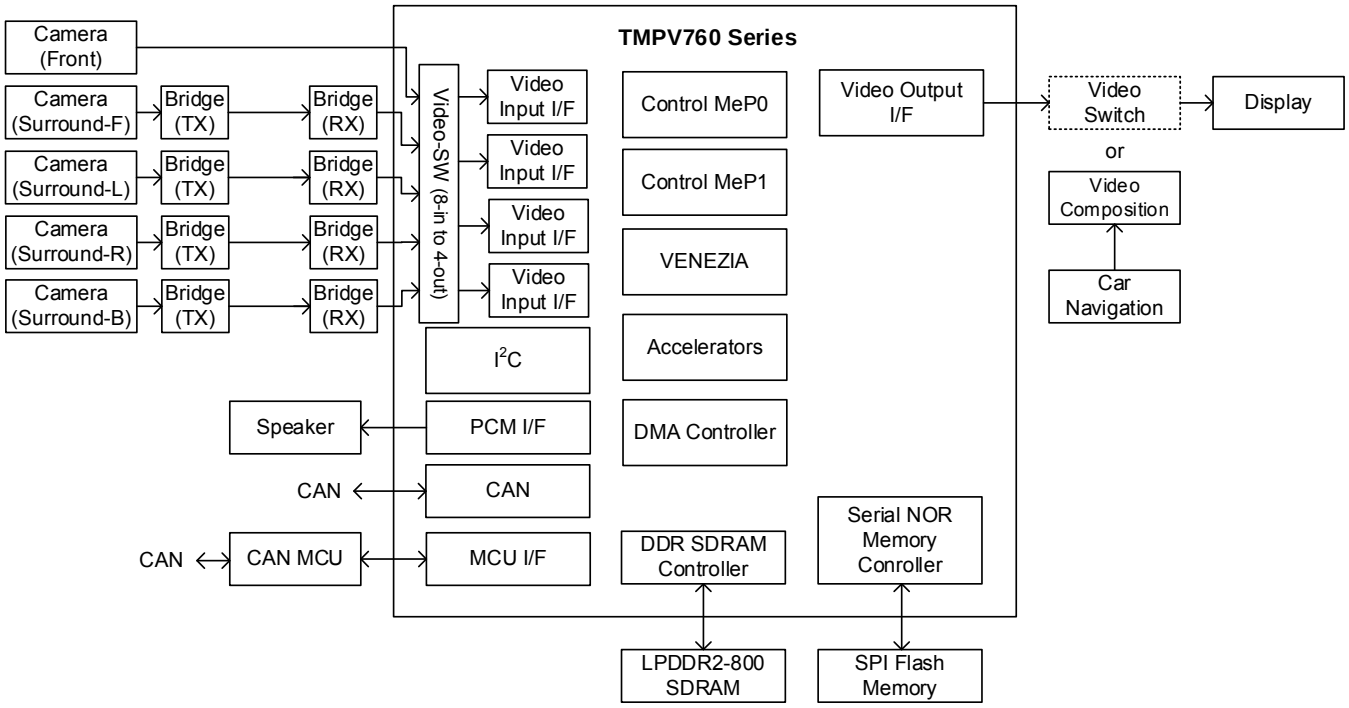

Figure 1.7 Example of Front-/Surrounding View Monitoring System of TMPV7608XBG

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1.6.3. Advanced Driver Assistance Systems Example 3: Vehicle Inside Monitoring

For the Driver Authentication system and Driver Monitoring system and Crew Monitoring system in which drivers or the crews of vehicles are subjected to near infrared rays. These pictures are taken by a single near infrared camera and are analyzed using a monitoring system.

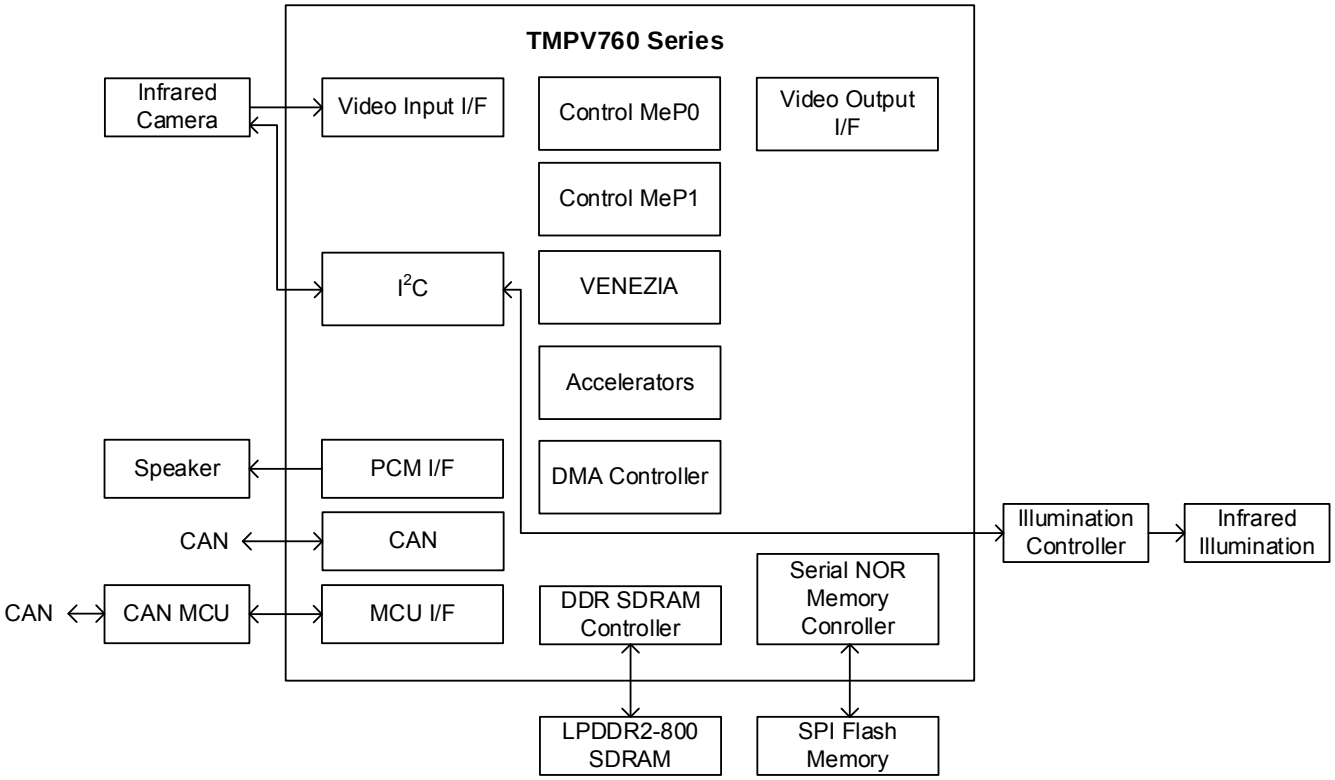

Figure 1.8 Example of Vehicle Inside Monitoring System

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1.7. Features

1.7.1. Control MeP

- Toshiba original 32-bit RISC core MeP-c5
- 16 KB (2-way set-associative) instruction cache and 8 KB (2-way set-associative) data cache
- 16 KB (8 KB × 2 banks) instruction RAM and 32 KB (8 KB × 4 banks) data RAM
- DMA controller used for reading/writing the instruction RAM and data RAM
- Operating frequency: 266.7 MHz maximum
- 2 channels of timer
- JTAG debug port
  It is also connected to VENEZIA, so a single ICE supports the control MeP and VENEZIA debugging.
- The number of modules: 2

1.7.2. Multi-Core Sub-System VENEZIA

- Toshiba original 32-bit RISC multi-core sub-system
- A multi-core with four media processing engine MPE
- Features of each MPE
  - 32-bit RISC core MeP-c5
  - 16 KB (2-way set-associative) instruction cache and 16 KB (2-way set-associative) data cache
  - 64 KB (16 KB × 4 banks) data RAM
  - Image recognition VLIW coprocessor IVC2F
  - VLIW (Very Long Instruction Word) technology that issues up to three instructions simultaneously (one MeP instruction and up to two IVC2 instructions can be encoded in a 64-bit VLIW code).
  - SIMD (Single Instruction stream, Multiple Data stream) that perform simultaneous operations on eight sets of 8-bit data, four sets of 16-bit data, and two sets of 32-bit data.
    Each IVC2F can execute simultaneously up to two SIMD instructions or double-precision floating point number data.
    Some SIMD instructions can store 256 bits of operation results in accumulators. When the calculation result does not exceed 32 bits, it can be speeded by omitting the carry processing.
  - DMA controller used for transferring the data of data RAM
  - Two channels of timer
- Shared use among the four MPE
  - 256 KB (4-way set-associative) L2 cache
  - 8 KB local SRAM
  - MPE-to-MPE interrupt controllers for controlling the interruption between each MPE
  - Local timer controller for 64-bit free-run counter and timer modules for each MPE core
- JTAG debug port
  It is also connected to VENEZIA, so a single ICE supports the control MeP and VENEZIA debugging.
- Operating frequency: 266.7 MHz maximum
- Number of modules:
  - TMPV7608XBG: 2 modules
  - TMPV7602XBG: 1 module

1.7.3. Image Processing Accelerators

1.7.3.1. Affine Transformation Accelerator

- Five operation modes
  - Geometric transformation such as rotation, expansion/dilation, translation, shear and so on of image data
  - Homography transformation
  - Image transformation using a distortion correction formula (e.g. lens distortion correction)

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  - Image transformation by using a lookup table (e.g. fisheye distortion correction, windshield distortion correction, viewpoint transformation)
  - Consecutive operation modes of Affine transformation/homography transformation and Distortion Correction Formula Conversion
- Number of channels:
  - TMPV7608XBG: 3 channels
  - TMPV7602XBG: 2 channels
- Operating frequency: 266.7 MHz maximum

1.7.3.2. Pyramid Accelerator

- Six types of horizontal and vertical scaling filter modes
  - 8-TAP 8 over sampling
  - 4-TAP 16 over sampling
  - 2-TAP 128 over sampling
  - 2-TAP 256 over sampling
  - 2-TAP 512 over sampling
  - Nearest neighbor interpolation
- Horizontal and vertical reduction rate
  - ×1 to ×1/2
    - Four reduction images are generated in one operation. (Each output image can be independently configured horizontal and vertical for each route).
    - Execute for multiple times to reduce an image to ×1/2 or lower.
- Number of channels: 2 channels
- Operating frequency: 266.7 MHz maximum

1.7.3.3. Histogram Accelerator

- Two operating modes
  - Histogram (Unweighted/weighted can be selected)
  - Image transformation (e.g. luminance transformation) by using a lookup table.
- Plural image areas can be specified between 1 and 255.
- Number of bins and counter sizes selectable from among eight types.
  - 256 bins 32-bit count
  - 512 bins 16-bit count
  - 1024 bins 8-bit count
  - 4096 bins 32-bit count
  - 8192 bins 32-bit count
  - 16384 bins 32-bit count
  - 32768 bins 16-bit count
  - 65536 bins 8-bit count
- Number of channels:
  - TMPV7608XBG: 1 channel
  - TMPV7602XBG: 2channels
- Operating frequency: 266.7 MHz maximum

1.7.3.4. HOG Accelerator

- Three operation modes
  - Dictionary transfer mode
  - Likelihood output mode
  - Feature descriptor output mode
- Feature descriptor can be selected from two types.
  - HOG of histogram of luminance gradient intensity
  - Toshiba's original technology, Co-occurrence Histograms of Oriented Gradients (CoHOG)
- Number of channels:
  - TMPV7608XBG: 1 channel

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  - TMPV7602XBG: 2 channels
- Operating frequency: 266.7 MHz maximum

1.7.3.5. Enhanced CoHOG Accelerator

- Two operation modes
  - Feature vector calculation (feature amount output) mode
  - Linear classification calculation (likelihood output) mode
- Feature descriptor of luminance and gradient in color space is used.
  - HOG of Histograms of Oriented Gradients (which can be set to weighted)
  - Toshiba's original Co-occurrence Histograms of Oriented Gradients (CoHOG)
  - Toshiba's original Co-occurrence Histogram of oriented gradients in color space (Color-CoHOG)
  - Toshiba's original CoHED, co-occurrence histogram of color difference in edge orthogonal direction.
  - Toshiba's original CoHD, co-occurrence histogram of color difference in linear direction.
  - Toshiba's original Color Histogram, secondary color histogram.
- The number of channels:
  - TMPV7608XBG: 2 channels
  - TMPV7602XBG: 1 channel
- Operating frequency: 266.7 MHz maximum

1.7.3.6. Filter Accelerator

- Parallel processing of 64-pixel
- Selection of the following processes by parameters
  - Operation between two image data
  - Operation between an image data item and a scalar
  - Smoothing
  - Canny edge detection
  - Harris corner detection
  - Gradient matrix calculation
  - Pyramid up/down
  - Color space conversion
  - Morphology operation
  - Template matching
  - Demosaicing
  - Other
- Number of channels: 2 channels
- Operating frequency: 180 MHz maximum

1.7.3.7. Matching Accelerator

- Two operating modes
  - Stereo disparity calculation mode
    Parallax calculation of left/right image data from a stereo camera. Polyline fitting or parabola fitting selectable.
  - Search mode
    A reference image for an input image is searched (free search, rectangle search, or slant search mode) for tracking and optical flow.
- Calculation mode
  - Sum of absolute difference (SAD)
  - Sum of orientation code difference
  - Normal cross correlation (NCC)
- Number of channels: 2 channels
- Operating frequency: 266.7 MHz maximum

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1.7.3.8. SfM Accelerator

- Two operation modes
  - Self-motion estimation mode
    Position and attitude for camera are estimated.
  - Three dimensional coordinate estimation mode
    The three dimensional coordinates of measurement points in an image is calculated based on the principle of triangulation using an estimated position and attitude for the camera.
- Number of channels: 1 channel (TMPV7608XBG)
- Operating frequency: 266.7 MHz maximum

1.7.4. Video Input Interface

- Connect up to eight cameras and up to four camera images can be captured (depending on a product and signal format).
- Parallel interface and serial interface (MIPI CSI-2) are supported.
  - TMPV7608XBG: Up to 8 (Parallel × 4, Serial × 4) connect → 4 input
  - TMPV7602XBG: Up to 2 (Parallel × 1, Serial × 1) connect → 1 input
- Color space conversion
  - YCbCr422 8/16 bits → RGB888 and RGB888+Y8
  - YCbCr422 20 bits → RGB888, RGB888+Y8, RGB888+Y16, and RGB16-16-16
  - RGB888 → YCbCr422 and RGB888+Y8
- Demosaicing
  - RAW 8bit → YCbCr422, RGB888, and RGB888+Y8
  - RAW 10/12/14/16 bits → YCbCr422, RGB888, RGB888+Y8, RGB888+Y16, and RGB16-16-16
- Cutting out and capturing specific regions
- Independent horizontal/vertical reduction (1/2, 1/4, 1/8) of capture image
- Odd, Even, and both fields can be selected for interlace.
- Gamma correction using a look up table method in which R, G, B, and Y are independent.

1.7.4.1. Parallel Interface

- Up to four camera images can be captured (depending on a signal format).
- Image size and frame rate
  - 1080p (1920 × 1080 pixels): 30 fps maximum
  - SXGA (1280 × 1024 pixels): 60 fps maximum
  - 720p (1280 × 720 pixels): 60 fps maximum
  - WVGA (800 × 480 pixels) or lower: 60 fps maximum
  - QVGA (320 × 240 pixels) or lower: 100 fps maximum
- Support for various input video signal formats
  - Grayscale Y8/10/12 bits: 4 channels maximum
  - Color ITU-R BT.656: 4 channels maximum
  - ColorYCbCr422 8/16 bits: 4 channels maximum
  - Color 16-bit separate YCbCr422: 2 channels maximum (Note 1)
  - Color 20-bit separate YCbCr422: 2 channels maximum (Note 1)
  - Color RGB888 24 bits: 2 channels maximum (Note 1)
  - Color RAW8/10/12/14/16 bits: 4 channels maximum
  - For CVBS input of NTSC/PAL, it needs to be connected via a video decoder such as Toshiba TC90105FG.

(Note 1) Formats (including 16-bit separate) exceeding 16 bits for the external video input has a limitation in the number of usable channels.

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1.7.4.2. Serial Interface (MIPI CSI-2)

- Four independent reception circuit (MIPI CSI2_0-3)

TMPV760 Series	MIPI_CSI2_0	MIPI_CSI2_1	MIPI_CSI2_2	MIPI_CSI2_3
TMPV7608XBG	1 or 2 or 4 data lanes	1 or 2 data lanes	1 or 2 or 4 data lanes	1 or 2 data lanes
TMPV7602XBG	1 or 2 or 4 data lanes	-	-	-

- Maximum lane speed
  - 800 Mbps@DDR - 400 MHz
- Maximum pixel rate
  - 200 Mpixel/s (When 1920 × 1080@60 fps, pixel rates are approximately 150 Mpixel/s)
- Various input video signal formats are supported.
  - Color RGB 888/565
  - Color YUV 422 8/10 bits
  - Color RAW 8/10/12/14 bits

  Interlace form (e.g. 1080i) is not supported.
- Other support for CSI-2 standard
  - Supported function
    - Embedded Data8 reception
    - Clock stop mode (Non-continuous clock mode)
  - Functions not supported
    - Virtual Channel
    - Data Interleaving
    - Power Down (1.2V power supply cut-off)

1.7.5. Video Output Interface

- Video output: 2 channels (Note 1) (TMPV7602XBG has 1 channel).
  - 24-bit RGB888
  - 16-bit RGB565
- Maximum size and frame rate
  - 720p (1280 × 720 pixels): 60 fps maximum
  - SXGA (1280 × 1024 pixels): 30 fps maximum
- Support for various video layer format (each layer can be selected).
  - 8-bit grayscale Y8
  - 24-bit color RGB888 (planar or packed)
  - 24-bit color ARGB8888 with 8-bit α value for blending
  - 16-bit color RGB565
  - Color YCbCr422 (planar or packed)
  - 8-bit index color (each color is specified by 24-bit color ARGB8888 look up table with 8-bit α value)
- Video Layer
  - Support for synthesis of background color and up to five layers
  - Layer synthesis can be made transparent using a color key, an 8-bit alpha value (selectable in pixel units or layer units) or the non-transparency processing by an escape key.
  - Specification of any one color from RGB888 for the background color
  - Each layer display position and display size can be specified in 1-pixel unit
  - ×1, ×2, and ×4 scaling can be independently configured every layer, horizontal, and vertical.

(Note 1) VOIF1 of TMPV7608XBG is not supported.

1.7.6. SRAM/NOR Memory Controller

- Memory type: 16-bit data bus width of parallel interface, such as NOR Flash memory (Note 1),

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SRAM, ROM.

- TMPV7608XBG: 24-bit address
- TMPV7602XBG: 8-bit address

- Access time: This value can be set as a multiple of 30.0 ns (when the system clock frequency is 266.7 MHz).
- Memory capacity: 32 Mbytes × 1 to 2 chip select (TMPV7602XBG is 1 chip select).

(Note 1) TMPV7602XBG is 8-bit address. Therefore, it does not support NOR Flash memory.

1.7.7. Serial NOR Memory Controller

- Memory type: NOR flash memory of the SPI interface.
- Transfer mode: SPI Mode0 and Quad I/O Read are supported.
- Memory capacity: 64 Kbytes to 64 Mbytes × 1 to 2 chip select (TMPV7602XBG is 1 chip select).
- Transfer clock: Up to 66.7 MHz

1.7.8. DDR SDRAM Controller

- Number of channels:
  - TMPV7608XBG: 2 channels
  - TMPV7602XBG: 1 channel
- Memory type: LPDDR2-800/667 is supported.
- Data bus width: 32 bits
- Connection number of SDRAM: 2 (per 1 channel)
- Address mapping area: Up to 16 Gbits (2 Gbytes)

1.7.9. On-Chip Memory

1.7.9.1. Working RAM

- 1.5-Mbytes working RAM for image data (scratchpad memory)
- Consists of 256 Kbytes × 6 (mapped as 1.5 Mbytes of continuous address area).
- Supports for parallel access of image data (128-bit width, 133.3 MHz maximum) from up to six masters (Control MeP, MPE in VENEZIA, image processing accelerators, DMA controllers, video input interfaces and video output interface)

Note: When use the SfM accelerator, user can only be used WRAM0-3.

1.7.9.2. System RAM

- 96-Kbytes scratchpad memory
  - It is used as a working memory for the control MeP.

1.7.9.3. System ROM

- 80-Kbytes mask ROM
  - Boot codes for the control MeP and font data of the ASCII codes are stored.

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1.7.10. Software Development Support

1.7.10.1. Performance Monitor

- DRAM access count function
  - Measures the data amount (in the unit of 256 bits) of the DRAM accessed by a master module.
- DRAM access checker function
  - Monitors a request to a specified address region in the DRAM. It issues an interrupt notification to the CPU when an access is done by an unauthorized master module.
  - 8 address regions can be checked at maximum.
- DRAM read latency measurement (counter) function
  - Measures the read latency when a master module reads DRAM data.
  - The data amount of 8 group master modules at maximum can be measured at the same time.

1.7.10.2. Bus Error

- Detection of the internal bus errors for support the debugging at the system development.

1.7.11. Hardware Diagnostic

1.7.11.1. Parity

- Incorporated the error detection circuit (1 bit parity) to detect a software error which may occur during system procedure execution, for each cache and internal RAM of Control MeP and VENEZIA, System RAM, and Working RAM.

1.7.11.2. Software Triggered BIST

- Self-diagnosis circuit which has a self-diagnosis mode and an initialization mode at the system startup for all of the internal RAMs.
  - Self-diagnosis mode: Start up the self-diagnosis for the internal RAMs and monitor the result.
  - Initialization mode: Internal RAMs are initialized to 0.

1.7.12. Interrupt Controller

- This function controls interrupts in the TMPV760 Series, notifying interrupts to the CPU (control MeP and VENEZIA).
- External Non-Maskable Interrupt (NMI) input: 1 channel
- External interrupt input
  - Pins are shared with the General-purpose I/O (up to 16 channels).
  - Edge/ level and polarity are selectable.

1.7.13. Global DMA Controller

- Built-in two DMA controllers.
- Two transfer modes: Channel transfer mode and thread transfer mode
  - Channel transfer mode: Specification of the transfer command by register, 1 channel
  - Thread transfer mode: Consecutive execution of the transfer commands stored in memory. This instruction can be executed repeatedly. 1 thread
- Source address/ destination address streaming also supported.
- Transfer up to 65,535 bytes with a single command.

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1.7.14. Peripheral DMA Controller

- Three DMA controllers
- Number of channels: 8 channels (per PDMAC)
- Bus master: 2 (per PDMAC)
- Number of DMA requests: Up to 16 (per PDMAC)
- Transfer type: Transfer between UART/SPI/I2C/PCMIF and a memory
- A single transfer command can transfer up to 16,380 bytes.
- Scatter/gather is supported.

1.7.15. General-purpose I/O

- 24 bits maximum (TMPV7602XBG is 16 bits maximum).
  (Pins are shared among UART interface, SPI interface, I2C interface, Timer, and PCM interface).
- Setting and clearing output in the unit of bit.

1.7.16. Timer

- Five modes
  - Timer modes
    - 32-bit free-run counter
    - Interval interrupt
  - Output compare mode
    - Minimum output unit: 1 µs. maximum output: 4294.9 s
  - Input capture mode
    - Minimum pulse measurement period: 1 µs. Measurement is supported up to 4294.9 s.
  - PWM (Pulse Width Modulation) output mode
  - Pulse generation mode
    - Pulse can be generated in synchronization with an external trigger.
- Up to four channels
  (Output compare mode, input capture mode, PWM output mode and pulse generation mode share pins with UART interface, SPI interface, I2C interface, PCM interface, and general purpose I/O).

1.7.17. UART Interface

- UART for users
  - Up to four channels
    (SPI interface, I2C interface, timer, PCM interface, and general purpose I/O share pins)
  - With flow control.
- UART for debugging
  - 1 channel (the pin is exclusive pin which is not shared with other functions)
- Full-duplex communication protocol (half-duplex communication protocol not supported)
  - Word length: Selectable from 5, 6, 7, and 8 bits (LSB first)
  - Stop bit: Selectable from 1 or 2 bits.
  - Parity bit: Selectable from odd parity, even parity and no parity.
- Programmable baud rate generator is incorporated.
  - UART 0-3 for users (up to 3,030,000 bps)
  - UART 4 for debugging (up to 921,600 bps)
- 32-stage FIFO for transmission and 32-stage FIFO for reception are incorporated respectively.

1.7.18. I2C Interface

- UP to 8 channels (TMPV7602XBG is up to 8 channels).
  (Of which 4 channels are UART interface, SPI interface, timer, PCM interface, and general purpose I/O share pins)

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- Slave and master functions are supported (multi-master function is not supported).
- Transmission and reception can be performed in standard mode (up to 100 kHz) and fast mode (up to 400 kHz).
- 8-stage FIFO for transmission and 8-stage FIFO for reception are incorporated.

1.7.19. SPI Interface

- Up to 4 channels
  (UART interface, I2C interface, timer, PCM interface, and general-purpose I/O share pins)
- Full-duplex, 4-line (data input, data output, serial clock, and chip select) can be simultaneously transferred.
  - Data frame size: 4 to 16 bits can be selected.
  - Master and slave function are supported (multi-master function is not supported).
- Clock prescale programming is supported.
- Cock polarity and phase can be selected.
- 8-stage FIFO for transmission and 8-stage FIFO for reception are incorporated.

1.7.20. PCM Interface

- Serial audio interface compliant to I2S standard
  - Data length: 16, 18, 20, and 24 bits
  - Number of slots: 32, 48, and 64 (slave mode), 64 (master modes)
- 2 channels (L/R) of input and 2 channels (L/R) output
  (UART interface, SPI interface, I2C interface, timer and general purpose I/O share pins).
- Sub oscillator for an audio clock is incorporated (master mode)
- 8-stage FIFO for transmission and 8-stage FIFO for reception are incorporated.

1.7.21. CAN Interface

- Conforming to the CAN protocol specification V2.0 Part B (active)
- Number of channels:
  - TMPV7608XBG: 3 channels
  - TMPV7602XBG: 2 channels
- Mailbox for each channel: 32 boxes (31 boxes for transmission/reception and one box for reception only)

1.7.22. MCU Interface

- For parallel communication interfacing with an external host MCU.
  - 8-bit bidirectional parallel bus
  - Controlled by four signals: read ready, read enable, write ready, and write enable.
- 32-bytes input FIFO and 32-bytes output FIFO.
- DMA controller for data transfer between a FIFO and a memory.

1.7.23. CRC Arithmetic Unit

- ITU-T CRC-16 calculation is supported.
  - Input data length: 8, 16, 32-bit data are supported.
- GDMAC transfer is supported.

1.7.24. CAN FD Interface

- Conforming to the CAN FD specification V1.0
- Number of channels: 2 channels (TMPV7602XBG)

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1.7.25. Power Management Unit

- Make the control of power-off and power restoration to the following module.
  - Affine transformation accelerator
  - Filter accelerator
  - Enhanced CoHOG accelerator
  - Matching accelerator
  - Pyramid accelerator
  - Working RAM
- TMPV7602XBG is incorporated.

1.7.26. Clock

- Oscillator
  - Main oscillator: For system PLL and video output interface PLL (Connected with a 12 MHz crystal oscillator)
  - Sub oscillator: For PCM interface
- PLL
  - TMPV7608XBG
    - System PLL: Generates a system clock. 266.7 MHz maximum.
    - Filter accelerator PLL: Generates a clock for a filter accelerator, 180 MHz maximum.
    - Video output interface PLL: Generates a clock for video output interface, 325 MHz maximum.
  - TMPV7602XBG
    - System PLL: Generates a system clock. 266.7 MHz maximum.
    - Filter accelerator PLL: Generates a clock for a filter accelerator, 180 MHz maximum.
    - Video output interface PLL: Generates a clock for video output interface, 325 MHz maximum.
    - CANFD PLL: Generates a clock for a CAN FD interface, 80 MHz maximum.

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2. Signal Description

2.1. Signal List

The following paragraphs explain each signal pin. The meaning of each item of each signal pin table is shown below.

- "Pin name": It shows the name of a pin.
- "Function": It shows the function of a pin.
- "Structure": It shows the structure of a pin. The meaning of each value is shown in "Table 2.1 Pin Structure."
- "I/O enabling control": It shows the state control at the time of initialization. The meaning of each value is shown below.
  - IE: IOSET_EN signal. It is in a Hi-Z state until I/O pin validation is performed.
  - —: I/O enabling control is not performed.
- "The input-and-output direction (DIR) ": (After I/O enabling control) The direction of the input and output is shown. The meaning of each value is shown below.
  - I: Input signal
  - O: Output signal
  - B: Bidirectional signal
  - —: Power supplies etc. are other signals.
- "Pull-Up/Pull-Down": It shows Pull Up and Pull Down control. The meaning of each value is shown below.
  - PU: Pull Up
  - PD: Pull Down
  - —: Neither -Pull Up nor Pull Down is carried out.
- "Handling of unused pin": It shows the processing when a pin is not used. The meaning of each value is shown below.
  - OPEN: OPEN (un-connecting) Please carry out.
  - VDD11: Connect to 1.1-V power supply.
  - VDD33: Connect to 3.3-V power supply.
  - GND: Connect to VSS ground.
  - PU: Pull up.
  - PD: Pull down.
  - RL: It is used as a Reset Latch setting.
- "TMPV760 Series": It shows the presence or absence of a pin for each product.
  - ✓: Pin exists.
  - —: Pin does not exist.

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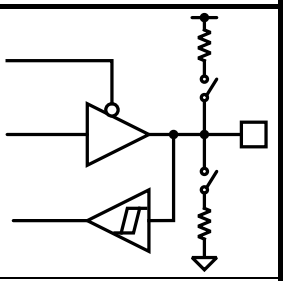
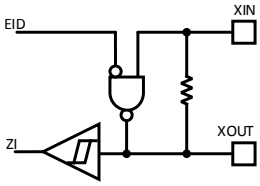
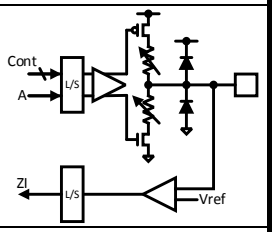
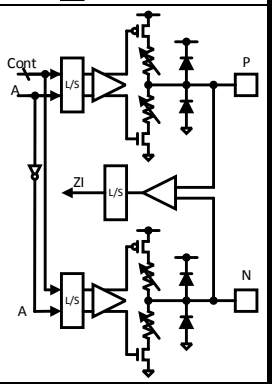
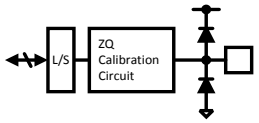
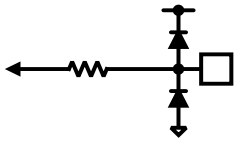
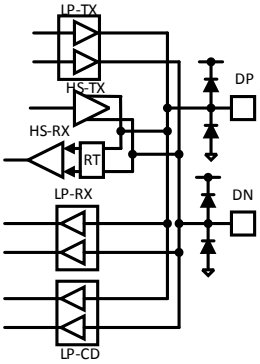
Table 2.1 Pin Structure

Symbol	Explanation	Structure
BD42(Note1)	3.3-V I/F bidirectional multi-drive buffer Schmidt Trigger input with pull-up / down (ON/OFF programmable)	
BD84(Note1)	3.3-V I/F bidirectional multi-drive buffer Schmidt Trigger input with pull-up / down (ON/OFF programmable)	
OSC	The buffer for crystal oscillators with feedback resistance	
DDR-IO	1.2-V LPDDR2 SDRAM input / output buffer (except DQS, CK)	
DDR-DQS	1.2-V LPDDR2 SDRAM input / output buffer	
DDR-CK	1.2-V LPDDR2 SDRAM input / output buffer	
DDR-ZQ	LPDDR2 SDRAM external resistance connection pin	
DDR-VREF	0.6-V LPDDR2 SDRAM reference voltage pin	
MIPI-IO	1.2-V MIPI-DPHY input buffer (Clock Lane, Data Lane)	
POWER	Digital power supply pin	—

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Symbol	Explanation	Structure
A-POWER	Analog power supply pin	—
GND	Ground pin	—

Note 1: It is basic structure. Please refer to the "Pull-Up/Pull-Down" item of each signal pin table for the existence of a pull-up/down.

2.1.1. Video Input Interface

Table 2.2 List of Parallel Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
VIIF_VSYNC0	VIIF0 Vertical-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	✓
VIIF_HSYNC0	VIIF0 Horizontal-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	✓
VIIF_FIELD0	VIIF0 Field signal input	BD42	IE	I	PD	OPEN	✓	✓
VIIF_CK0	VIIF0 Clock Input	BD42	IE	I	PD	OPEN	✓	✓
VIIF_VSYNC1	VIIF1 Vertical-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_HSYNC1	VIIF1 Horizontal-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_FIELD1	VIIF1 Field signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_CK1	VIIF1 Clock Input	BD42	IE	I	PD	OPEN	✓	—
VIIF_VSYNC2	VIIF2 Vertical-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_HSYNC2	VIIF2 Horizontal-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_FIELD2	VIIF2 Field signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_CK2	VIIF2 Clock Input	BD42	IE	I	PD	OPEN	✓	—
VIIF_VSYNC3	VIIF3 Vertical-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_HSYNC3	VIIF3 Horizontal-Synchronizing signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_FIELD3	VIIF3 Field signal input	BD42	IE	I	PD	OPEN	✓	—
VIIF_CK3	VIIF3 Clock Input	BD42	IE	I	PD	OPEN	✓	—
VIIF_D0	VIIF Data Input 0	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D1	VIIF Data Input 1	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D2	VIIF Data Input 2	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D3	VIIF Data Input 3	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D4	VIIF Data Input 4	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D5	VIIF Data Input 5	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D6	VIIF Data Input 6	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D7	VIIF Data Input 7	BD42	IE	I	PD	OPEN	✓	✓

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
VIIF_D8	VIIF Data Input 8	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D9	VIIF Data Input 9	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D10	VIIF Data Input 10	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D11	VIIF Data Input 11	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D12	VIIF Data Input 12	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D13	VIIF Data Input 13	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D14	VIIF Data Input 14	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D15	VIIF Data Input 15	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D16	VIIF Data Input 16	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D17	VIIF Data Input 17	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D18	VIIF Data Input 18	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D19	VIIF Data Input 19	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D20	VIIF Data Input 20	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D21	VIIF Data Input 21	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D22	VIIF Data Input 22	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D23	VIIF Data Input 23	BD42	IE	I	PD	OPEN	✓	✓
VIIF_D24	VIIF Data Input 24	BD42	IE	I	PD	OPEN	✓	—
VIIF_D25	VIIF Data Input 25	BD42	IE	I	PD	OPEN	✓	—
VIIF_D26	VIIF Data Input 26	BD42	IE	I	PD	OPEN	✓	—
VIIF_D27	VIIF Data Input 27	BD42	IE	I	PD	OPEN	✓	—
VIIF_D28	VIIF Data Input 28	BD42	IE	I	PD	OPEN	✓	—
VIIF_D29	VIIF Data Input 29	BD42	IE	I	PD	OPEN	✓	—
VIIF_D30	VIIF Data Input 30	BD42	IE	I	PD	OPEN	✓	—
VIIF_D31	VIIF Data Input 31	BD42	IE	I	PD	OPEN	✓	—
VIIF_D32	VIIF Data Input 32	BD42	IE	I	PD	OPEN	✓	—
VIIF_D33	VIIF Data Input 33	BD42	IE	I	PD	OPEN	✓	—
VIIF_D34	VIIF Data Input 34	BD42	IE	I	PD	OPEN	✓	—
VIIF_D35	VIIF Data Input 35	BD42	IE	I	PD	OPEN	✓	—
VIIF_D36	VIIF Data Input 36	BD42	IE	I	PD	OPEN	✓	—
VIIF_D37	VIIF Data Input 37	BD42	IE	I	PD	OPEN	✓	—
VIIF_D38	VIIF Data Input 38	BD42	IE	I	PD	OPEN	✓	—
VIIF_D39	VIIF Data Input 39	BD42	IE	I	PD	OPEN	✓	—
VIIF_D40	VIIF Data Input 40	BD42	IE	I	PD	OPEN	✓	—
VIIF_D41	VIIF Data Input 41	BD42	IE	I	PD	OPEN	✓	—
VIIF_D42	VIIF Data Input 42	BD42	IE	I	PD	OPEN	✓	—
VIIF_D43	VIIF Data Input 43	BD42	IE	I	PD	OPEN	✓	—
VIIF_D44	VIIF Data Input 44	BD42	IE	I	PD	OPEN	✓	—
VIIF_D45	VIIF Data Input 45	BD42	IE	I	PD	OPEN	✓	—
VIIF_D46	VIIF Data Input 46	BD42	IE	I	PD	OPEN	✓	—
VIIF_D47	VIIF Data Input 47	BD42	IE	I	PD	OPEN	✓	—
VIIF_D48	VIIF Data Input 48	BD42	IE	I	PD	OPEN	✓	—
VIIF_D49	VIIF Data Input 49	BD42	IE	I	PD	OPEN	✓	—
VIIF_D50	VIIF Data Input 50	BD42	IE	I	PD	OPEN	✓	—
VIIF_D51	VIIF Data Input 51	BD42	IE	I	PD	OPEN	✓	—
VIIF_D52	VIIF Data Input 52	BD42	IE	I	PD	OPEN	✓	—
VIIF_D53	VIIF Data Input 53	BD42	IE	I	PD	OPEN	✓	—
VIIF_D54	VIIF Data Input 54	BD42	IE	I	PD	OPEN	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
VIIF_D55	VIIF Data Input 55	BD42	IE	I	PD	OPEN	✓	—
VIIF_D56	VIIF Data Input 56	BD42	IE	I	PD	OPEN	✓	—
VIIF_D57	VIIF Data Input 57	BD42	IE	I	PD	OPEN	✓	—
VIIF_D58	VIIF Data Input 58	BD42	IE	I	PD	OPEN	✓	—
VIIF_D59	VIIF Data Input 59	BD42	IE	I	PD	OPEN	✓	—
VIIF_D60	VIIF Data Input 60	BD42	IE	I	PD	OPEN	✓	—
VIIF_D61	VIIF Data Input 61	BD42	IE	I	PD	OPEN	✓	—
VIIF_D62	VIIF Data Input 62	BD42	IE	I	PD	OPEN	✓	—
VIIF_D63	VIIF Data Input 63	BD42	IE	I	PD	OPEN	✓	—

For the correspondence between each channel of video input interface and each pin of parallel interface is as shown in "Table 2.3 Connection between Parallel Interface Pins and ."

Table 2.3 Connection between Parallel Interface Pins and Video Input Interface

Symbol	Connection Destination			
	VIIF0	VIIF1	VIIF2	VIIF3
VIIF_D[15:0]	DATA[15:0]	—	—	—
VIIF_D[23:16]	DATA[23:16]	DATA[7:0]	—	—
VIIF_D[31:24]	—	DATA[15:8]	—	—
VIIF_D[47:32]	—	—	DATA[15:0]	—
VIIF_D[55:48]	—	—	DATA[23:16]	DATA[7:0]
VIIF_D[63:56]	—	—	—	DATA[15:8]
VIIF_HSYNC0	HSYNC	—	—	—
VIIF_HSYNC1	—	HSYNC	—	—
VIIF_HSYNC2	—	—	HSYNC	—
VIIF_HSYNC3	—	—	—	HSYNC
VIIF_VSYNC0	VSYNC	—	—	—
VIIF_VSYNC1	—	VSYNC	—	—
VIIF_VSYNC2	—	—	VSYNC	—
VIIF_VSYNC3	—	—	—	VSYNC
VIIF_FIELD0	FIELD	—	—	—
VIIF_FIELD1	—	FIELD	—	—
VIIF_FIELD2	—	—	FIELD	—
VIIF_FIELD3	—	—	—	FIELD
VIIF_CK0	VCLK	—	—	—
VIIF_CK1	—	VCLK	—	—
VIIF_CK2	—	—	VCLK	—
VIIF_CK3	—	—	—	VCLK

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The video signal input to the VIIF_D[63:0] pin uses the DATA[23:0] as video input interface data signal. The position of the data bit of the input video signal is as shown in "Table 2.4 Corresponds between Video Input Format and Video Input Interface Data Signal."

Table 2.4 Corresponds between Video Input Format and Video Input Interface Data Signal

VIIF Data Signal	Video Input Format													
	RGB 888	YCbCr				BT.656	RAW					Y		
		20bit separate	16bit separate	16bit	8bit		16bit	14bit	12bit	10bit	8bit	12bit	10bit	8bit
DATA0	R0	Y0	Y0	Y0	bit 0	bit 0	bit 0	bit 0	bit 0	bit 0	bit 0	Y0	Y0	Y0
DATA1	R1	Y1	Y1	Y1	bit 1	bit 1	bit 1	bit 1	bit 1	bit 1	bit 1	Y1	Y1	Y1
DATA2	R2	Y2	Y2	Y2	bit 2	bit 2	bit 2	bit 2	bit 2	bit 2	bit 2	Y2	Y2	Y2
DATA3	R3	Y3	Y3	Y3	bit 3	bit 3	bit 3	bit 3	bit 3	bit 3	bit 3	Y3	Y3	Y3
DATA4	R4	Y4	Y4	Y4	bit 4	bit 4	bit 4	bit 4	bit 4	bit 4	bit 4	Y4	Y4	Y4
DATA5	R5	Y5	Y5	Y5	bit 5	bit 5	bit 5	bit 5	bit 5	bit 5	bit 5	Y5	Y5	Y5
DATA6	R6	Y6	Y6	Y6	bit 6	bit 6	bit 6	bit 6	bit 6	bit 6	bit 6	Y6	Y6	Y6
DATA7	R7	Y7	Y7	Y7	bit 7	bit 7	bit 7	bit 7	bit 7	bit 7	bit 7	Y7	Y7	Y7
DATA8	G0	Y8	—	CbCr0	—	—	bit 8	bit 8	bit 8	bit 8	—	Y8	Y8	—
DATA9	G1	Y9	—	CbCr1	—	—	bit 9	bit 9	bit 9	bit 9	—	Y9	Y9	—
DATA10	G2	—	—	CbCr2	—	—	bit 10	bit 10	bit 10	—	—	Y10	—	—
DATA11	G3	—	—	CbCr3	—	—	bit 11	bit 11	bit 11	—	—	Y11	—	—
DATA12	G4	CbCr0	CbCr0	CbCr4	—	—	bit 12	bit 12	—	—	—	—	—	—
DATA13	G5	CbCr1	CbCr1	CbCr5	—	—	bit 13	bit 13	—	—	—	—	—	—
DATA14	G6	CbCr2	CbCr2	CbCr6	—	—	bit 14	—	—	—	—	—	—	—
DATA15	G7	CbCr3	CbCr3	CbCr7	—	—	bit 15	—	—	—	—	—	—	—
DATA16	B0	CbCr4	CbCr4	—	—	—	—	—	—	—	—	—	—	—
DATA17	B1	CbCr5	CbCr5	—	—	—	—	—	—	—	—	—	—	—
DATA18	B2	CbCr6	CbCr6	—	—	—	—	—	—	—	—	—	—	—
DATA19	B3	CbCr7	CbCr7	—	—	—	—	—	—	—	—	—	—	—
DATA20	B4	CbCr8	—	—	—	—	—	—	—	—	—	—	—	—
DATA21	B5	CbCr9	—	—	—	—	—	—	—	—	—	—	—	—
DATA22	B6	—	—	—	—	—	—	—	—	—	—	—	—	—
DATA23	B7	—	—	—	—	—	—	—	—	—	—	—	—	—

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Table 2.5 List of Serial Interface (MIPI CSI-2) Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
MIPI0_CMCP	MIPI_CSI2_0 Clock	MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMCN		MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD0P	MIPI_CSI2_0 Data 0	MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD0N		MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD1P	MIPI_CSI2_0 Data 1	MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD1N		MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD2P	MIPI_CSI2_0 Data 2	MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD2N		MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD3P	MIPI_CSI2_0 Data 3	MIPI-IO	—	I	—	GND	✓	✓
MIPI0_CMD3N		MIPI-IO	—	I	—	GND	✓	✓
MIPI1_CMCP	MIPI_CSI2_1 Clock	MIPI-IO	—	I	—	GND	✓	—
MIPI1_CMCN		MIPI-IO	—	I	—	GND	✓	—
MIPI1_CMD0P	MIPI_CSI2_1 Data 0	MIPI-IO	—	I	—	GND	✓	—
MIPI1_CMD0N		MIPI-IO	—	I	—	GND	✓	—
MIPI1_CMD1P	MIPI_CSI2_1 Data 1	MIPI-IO	—	I	—	GND	✓	—
MIPI1_CMD1N		MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMCP	MIPI_CSI2_2 Clock	MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMCN		MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD0P	MIPI_CSI2_2 Data 0	MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD0N		MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD1P	MIPI_CSI2_2 Data 1	MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD1N		MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD2P	MIPI_CSI2_2 Data 2	MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD2N		MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD3P	MIPI_CSI2_2 Data 3	MIPI-IO	—	I	—	GND	✓	—
MIPI2_CMD3N		MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMCP	MIPI_CSI2_3 Clock	MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMCN		MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMD0P	MIPI_CSI2_3 Data 0	MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMD0N		MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMD1P	MIPI_CSI2_3 Data 1	MIPI-IO	—	I	—	GND	✓	—
MIPI3_CMD1N		MIPI-IO	—	I	—	GND	✓	—

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2.1.2. Video Output Interface

Table 2.6 List of Video Output Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
VOIF0_VSYNC_N	VOIF0 Vertical-synchronizing Output	BD84	IE	O	PU	OPEN	✓	✓
VOIF0_HSYNC_N	VOIF0 Horizontal-Synchronizing Output	BD84	IE	O	PU	OPEN	✓	✓
VOIF0_DE	VOIF0 Data Enable	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_CK	VOIF0 Clock	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D0	VOIF0 Data 0	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D1	VOIF0 Data 1	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D2	VOIF0 Data 2	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D3	VOIF0 Data 3	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D4	VOIF0 Data 4	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D5	VOIF0 Data 5	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D6	VOIF0 Data 6	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D7	VOIF0 Data 7	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D8	VOIF0 Data 8	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D9	VOIF0 Data 9	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D10	VOIF0 Data 10	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D11	VOIF0 Data 11	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D12	VOIF0 Data 12	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D13	VOIF0 Data 13	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D14	VOIF0 Data 14	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D15	VOIF0 Data 15	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D16	VOIF0 Data 16	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D17	VOIF0 Data 17	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D18	VOIF0 Data 18	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D19	VOIF0 Data 19	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D20	VOIF0 Data 20	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D21	VOIF0 Data 21	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D22	VOIF0 Data 22	BD84	IE	O	PD	OPEN	✓	✓
VOIF0_D23	VOIF0 Data 23	BD84	IE	O	PD	OPEN	✓	✓
VOIF1_VSYNC_N	VOIF1 Vertical-synchronizing Output	BD84	IE	O	PU	OPEN	✓	—
VOIF1_HSYNC_N	VOIF1 Horizontal-synchronizing Output	BD84	IE	O	PU	OPEN	✓	—
VOIF1_DE	VOIF1 Data Enable	BD84	IE	O	PD	OPEN	✓	—
VOIF1_CK	VOIF1 Clock	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D0	VOIF1 Data 0	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D1	VOIF1 Data 1	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D2	VOIF1 Data 2	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D3	VOIF1 Data 3	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D4	VOIF1 Data 4	BD84	IE	O	PD	OPEN	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
VOIF1_D5	VOIF1 Data 5	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D6	VOIF1 Data 6	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D7	VOIF1 Data 7	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D8	VOIF1 Data 8	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D9	VOIF1 Data 9	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D10	VOIF1 Data 10	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D11	VOIF1 Data 11	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D12	VOIF1 Data 12	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D13	VOIF1 Data 13	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D14	VOIF1 Data 14	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D15	VOIF1 Data 15	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D16	VOIF1 Data 16	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D17	VOIF1 Data 17	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D18	VOIF1 Data 18	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D19	VOIF1 Data 19	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D20	VOIF1 Data 20	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D21	VOIF1 Data 21	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D22	VOIF1 Data 22	BD84	IE	O	PD	OPEN	✓	—
VOIF1_D23	VOIF1 Data 23	BD84	IE	O	PD	OPEN	✓	—

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The correspondence of the VOIFn_D[23:0] pins (n = 0 or 1) and the RGB signal is as shown in "Table 2.7 Corresponds between Video Output Format and Each Pins."

Table 2.7 Corresponds between Video Output Format and Each Pins

Symbol	Video Output Format	
	RGB888	RGB565
VOIFn_D23	R7	R4
VOIFn_D22	R6	R3
VOIFn_D21	R5	R2
VOIFn_D20	R4	R1
VOIFn_D19	R3	R0
VOIFn_D18	R2	0
VOIFn_D17	R1	0
VOIFn_D16	R0	0
VOIFn_D15	G7	G5
VOIFn_D14	G6	G4
VOIFn_D13	G5	G3
VOIFn_D12	G4	G2
VOIFn_D11	G3	G1
VOIFn_D10	G2	G0
VOIFn_D9	G1	0
VOIFn_D8	G0	0
VOIFn_D7	B7	B4
VOIFn_D6	B6	B3
VOIFn_D5	B5	B2
VOIFn_D4	B4	B1
VOIFn_D3	B3	B0
VOIFn_D2	B2	0
VOIFn_D1	B1	0
VOIFn_D0	B0	0

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2.1.3. Serial NOR Memory Controller

Table 2.8 List of Serial NOR Memory Controller Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
SNORC_CS0_N	SPI Flash Memory Chip Select 0	BD84	—	O	—	OPEN	✓	✓
SNORC_CS1_N	SPI Flash Memory Chip Select 1	BD84	—	O	—	OPEN	✓	—
SNORC_CLK	SPI Flash Memory Clock	BD84	—	O	—	OPEN	✓	✓
SNORC_MOSI	SPI Flash Memory MOSI (Quad-compliant data 0)	BD84	—	B	—	OPEN	✓	—
					PU		—	✓
SNORC_MISO	SPI Flash Memory MISO (Quad-compliant data 1)	BD84	—	B	—	OPEN	✓	—
					PU		—	✓
SNORC_IO2	SPI Flash Memory Data 2 (Connect to a Quad-compliant SPI Flash Memory. Do not connect to a Single/Dual SPI Flash Memory).	BD84	—	B	—	OPEN	✓	—
					PU		—	✓
SNORC_IO3	SPI Flash Memory Data 3 (Connect to a Quad-compliant SPI Flash Memory. Do not connect to a Single/Dual SPI Flash Memory).	BD84	—	B	—	OPEN	✓	—
					PU		—	✓

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2.1.4. SRAM/NOR Memory Controller and MCU Interface

- The SRAM/NOR memory controller pin is shared with the MCU interface pin. Functions can be selected by the register setting.
- Specified as "RL" for the "Handling of unused pin" is used for Reset Latch setting. Pins set as "H" need to be pulled up by a 10kΩ resistor. Pins set as "L" need to be pulled down by a 10kΩ resistor.

Table 2.9 List of SRAM/NOR Memory Controller and MCU Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
MEMC_CS0_N	MEMC Chip Select 0	BD42	IE	O	PU	OPEN	✓	✓
MEMC_CS1_N	MEMC Chip Select 1	BD42	IE	O	PU	OPEN	✓	—
MEMC_WE_N	MEMC Write Enable	BD42	IE	O	PU	OPEN	✓	✓
MEMC_OE_N	MEMC Output Enable	BD42	IE	O	PU	OPEN	✓	✓
MEMC_A0	MEMC Address 0 (TMPV7602XBG is pin sharing with the MCUIF read-enable input)	BD42	IE	B	PD	PD	✓	✓
MEMC_A1	MEMC Address 1 (TMPV7602XBG is pin sharing with the MCUIF read ready output)	BD42	IE	B	PD	RL	✓	✓
MEMC_A2	MEMC Address 2 (TMPV7602XBG is pin sharing with the MCUIF write-enable input)	BD42	IE	B	PD	RL	✓	✓
MEMC_A3	MEMC Address 3 (TMPV7602XBG is pin sharing with the MCUIF write ready output)	BD42	IE	B	PD	RL	✓	✓
MEMC_A4	MEMC Address 4	BD42	IE	B	PD	PD	✓	✓
MEMC_A5	MEMC Address 5	BD42	IE	B	PD	PD	✓	✓
MEMC_A6	MEMC Address 6	BD42	IE	B	PD	PD	✓	✓
MEMC_A7	MEMC Address 7	BD42	IE	B	PD	PD	✓	✓
MEMC_A8	MEMC Address 8	BD42	IE	B	PD	RL	✓	—
MEMC_A9	MEMC Address 9	BD42	IE	B	PD	RL	✓	—
MEMC_A10	MEMC Address 10	BD42	IE	B	PD	RL	✓	—
MEMC_A11	MEMC Address 11	BD42	IE	B	PD	RL	✓	—
MEMC_A12	MEMC Address 12 (TMPV7608XBG is pin sharing with the MCUIF read-enable input)	BD42	IE	B	PD	RL	✓	—
MEMC_A13	MEMC Address 13 (TMPV7608XBG is pin sharing with the MCUIF read ready output)	BD42	IE	B	PD	RL	✓	—
MEMC_A14	MEMC Address 14 (TMPV7608XBG is pin sharing with the MCUIF write-enable input)	BD42	IE	B	PD	RL	✓	—
MEMC_A15	MEMC Address 15 (TMPV7608XBG is pin sharing with the MCUIF write ready output)	BD42	IE	B	PD	RL	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
MEMC_A16	MEMC Address 16 (TMPV7608XBG is pin sharing with the MCUIF Data 0)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A17	MEMC Address 17 (TMPV7608XBG is pin sharing with the MCUIF Data 1)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A18	MEMC Address 18 (TMPV7608XBG is pin sharing with the MCUIF Data 2)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A19	MEMC Address 19 (TMPV7608XBG is pin sharing with the MCUIF Data 3)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A20	MEMC Address 20 (TMPV7608XBG is pin sharing with the MCUIF Data 4)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A21	MEMC Address 21 (TMPV7608XBG is pin sharing with the MCUIF Data 5)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A22	MEMC Address 22 (TMPV7608XBG is pin sharing with the MCUIF Data 6)	BD42	IE	B	PD	OPEN	✓	—
MEMC_A23	MEMC Address 23 (TMPV7608XBG is pin sharing with the MCUIF Data 7)	BD42	IE	B	PD	OPEN	✓	—
MEMC_D0	MEMC Data 0 (TMPV7602XBG is pin sharing with the MCUIF Data 0)	BD42	IE	B	PD	PD	✓	✓
MEMC_D1	MEMC Data 1 (TMPV7602XBG is pin sharing with the MCUIF Data 1)	BD42	IE	B	PD	PD	✓	—
						RL	—	✓
MEMC_D2	MEMC Data 2 (TMPV7602XBG is pin sharing with the MCUIF Data 2)	BD42	IE	B	PD	PD	✓	—
						RL	—	✓
MEMC_D3	MEMC Data 3 (TMPV7602XBG is pin sharing with the MCUIF Data 3)	BD42	IE	B	PD	PD	✓	✓
MEMC_D4	MEMC Data 4 (TMPV7602XBG is pin sharing with the MCUIF Data 4)	BD42	IE	B	PD	PD	✓	✓

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
MEMC_D5	MEMC Data 5 (TMPV7602XBG is pin sharing with the MCUIF Data 5)	BD42	IE	B	PD	PD	✓	✓
MEMC_D6	MEMC Data 6 (TMPV7602XBG is pin sharing with the MCUIF Data 6)	BD42	IE	B	PD	PD	✓	✓
MEMC_D7	MEMC Data 7 (TMPV7602XBG is pin sharing with the MCUIF Data 7)	BD42	IE	B	PD	PD	✓	✓
MEMC_D8	MEMC Data 8	BD42	IE	B	PD	RL	✓	✓
MEMC_D9	MEMC Data 9	BD42	IE	B	PD	RL	✓	✓
MEMC_D10	MEMC Data 10	BD42	IE	B	PD	RL	✓	✓
MEMC_D11	MEMC Data 11	BD42	IE	B	PD	RL	✓	✓
MEMC_D12	MEMC Data 12	BD42	IE	B	PD	RL	✓	✓
MEMC_D13	MEMC Data 13	BD42	IE	B	PD	RL	✓	✓
MEMC_D14	MEMC Data 14	BD42	IE	B	PD	RL	✓	✓
MEMC_D15	MEMC Data 15	BD42	IE	B	PD	RL	✓	✓

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2.1.5. DDR SDRAM Controller

Table 2.10 DDR SDRAM Controller Pin List

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC0_CKE0	DDRC0 Clock Enable 0	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CKE1	DDRC0 Clock Enable 1	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CKN	DDRC0 Clock	DDR-CK	—	O	—	OPEN	✓	✓
DDRC0_CKP			—	O	—	OPEN	✓	✓
DDRC0_CS_N0	DDRC0 Chip Select 0	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CS_N1	DDRC0 Chip Select 1	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA0	DDRC0 Address 0	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA1	DDRC0 Address 1	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA2	DDRC0 Address 2	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA3	DDRC0 Address 3	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA4	DDRC0 Address 4	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA5	DDRC0 Address 5	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA6	DDRC0 Address 6	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA7	DDRC0 Address 7	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA8	DDRC0 Address 8	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_CA9	DDRC0 Address 9	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM0	DDRC0 Data Mask 0	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM1	DDRC0 Data Mask 1	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM2	DDRC0 Data Mask 2	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM3	DDRC0 Data Mask 3	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM4	DDRC0 Data Mask 4	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM5	DDRC0 Data Mask 5	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM6	DDRC0 Data Mask 6	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DM7	DDRC0 Data Mask 7	DDR-IO	—	O	—	OPEN	✓	✓
DDRC0_DQ0	DDRC0 Data 0	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ1	DDRC0 Data 1	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ2	DDRC0 Data 2	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ3	DDRC0 Data 3	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ4	DDRC0 Data 4	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ5	DDRC0 Data 5	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ6	DDRC0 Data 6	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ7	DDRC0 Data 7	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ8	DDRC0 Data 8	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ9	DDRC0 Data 9	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ10	DDRC0 Data 10	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ11	DDRC0 Data 11	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ12	DDRC0 Data 12	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ13	DDRC0 Data 13	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ14	DDRC0 Data 14	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ15	DDRC0 Data 15	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ16	DDRC0 Data 16	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ17	DDRC0 Data 17	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ18	DDRC0 Data 18	DDR-IO	—	B	—	OPEN	✓	✓

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC0_DQ19	DDRC0 Data 19	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ20	DDRC0 Data 20	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ21	DDRC0 Data 21	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ22	DDRC0 Data 22	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ23	DDRC0 Data 23	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ24	DDRC0 Data 24	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ25	DDRC0 Data 25	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ26	DDRC0 Data 26	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ27	DDRC0 Data 27	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ28	DDRC0 Data 28	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ29	DDRC0 Data 29	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ30	DDRC0 Data 30	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ31	DDRC0 Data 31	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ32	DDRC0 Data 32	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ33	DDRC0 Data 33	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ34	DDRC0 Data 34	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ35	DDRC0 Data 35	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ36	DDRC0 Data 36	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ37	DDRC0 Data 37	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ38	DDRC0 Data 38	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ39	DDRC0 Data 39	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ40	DDRC0 Data 40	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ41	DDRC0 Data 41	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ42	DDRC0 Data 42	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ43	DDRC0 Data 43	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ44	DDRC0 Data 44	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ45	DDRC0 Data 45	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ46	DDRC0 Data 46	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ47	DDRC0 Data 47	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ48	DDRC0 Data 48	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ49	DDRC0 Data 49	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ50	DDRC0 Data 50	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ51	DDRC0 Data 51	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ52	DDRC0 Data 52	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ53	DDRC0 Data 53	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ54	DDRC0 Data 54	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ55	DDRC0 Data 55	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ56	DDRC0 Data 56	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ57	DDRC0 Data 57	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ58	DDRC0 Data 58	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ59	DDRC0 Data 59	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ60	DDRC0 Data 60	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ61	DDRC0 Data 61	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ62	DDRC0 Data 62	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQ63	DDRC0 Data 63	DDR-IO	—	B	—	OPEN	✓	✓
DDRC0_DQSN0	DDRC0 Data Strobe 0	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP0			—	B	—	OPEN	✓	✓

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC0_DQSN1	DDRC0 Data Strobe 1	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP1	DDRC0 Data Strobe 1	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSN2	DDRC0 Data Strobe 2	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP2			—	B	—	OPEN	✓	✓
DDRC0_DQSN3	DDRC0 Data Strobe 3	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP3			—	B	—	OPEN	✓	✓
DDRC0_DQSN4	DDRC0 Data Strobe 4	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP4		DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSN5	DDRC0 Data Strobe 5	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP5		DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSN6	DDRC0 Data Strobe 6	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP6		DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSN7	DDRC0 Data Strobe 7	DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_DQSP7		DDR-DQS	—	B	—	OPEN	✓	✓
DDRC0_ZQ	Reference Input for DDRC0 Calibration	DDR-ZQ	—	I	—	OPEN	✓	✓
DDRC0_VREF0	DDRC0 Reference Voltage Input 0 (DDRC0_VDDO × 0.5V)	DDR-VREF	—	I	—	GND	✓	✓
DDRC0_VREF1	DDRC0 Reference Voltage Input 1 (DDRC0_VDDO × 0.5V)	DDR-VREF	—	I	—	GND	✓	✓
DDRC0_VREF2	DDRC0 Reference Voltage Input 2 (DDRC0_VDDO × 0.5V)	DDR-VREF	—	I	—	GND	✓	✓
DDRC0_VREF3	DDRC0 Reference Voltage Input 3 (DDRC0_VDDO × 0.5V)	DDR-VREF	—	I	—	GND	✓	✓
DDRC0_TEST0	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST1	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST2	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST3	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST4	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST5	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST6	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST7	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC0_TEST8	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST9	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST10	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST11	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST12	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST13	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC0_TEST14	DDRC0 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	✓
DDRC1_CKE0	DDRC1 Clock Enable 0	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CKE1	DDRC1 Clock Enable 1	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CKN	DDRC1 Clock	DDR-CK	—	O	—	OPEN	✓	—
DDRC1_CKP			—	O	—	OPEN	✓	—
DDRC1_CS_N0	DDRC1 Chip Select 0	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CS_N1	DDRC1 Chip Select 1	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA0	DDRC1 Address 0	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA1	DDRC1 Address 1	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA2	DDRC1 Address 2	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA3	DDRC1 Address 3	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA4	DDRC1 Address 4	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA5	DDRC1 Address 5	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA6	DDRC1 Address 6	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA7	DDRC1 Address 7	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA8	DDRC1 Address 8	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_CA9	DDRC1 Address 9	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM0	DDRC1 Data Mask 0	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM1	DDRC1 Data Mask 1	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM2	DDRC1 Data Mask 2	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM3	DDRC1 Data Mask 3	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM4	DDRC1 Data Mask 4	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM5	DDRC1 Data Mask 5	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM6	DDRC1 Data Mask 6	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DM7	DDRC1 Data Mask 7	DDR-IO	—	O	—	OPEN	✓	—
DDRC1_DQ0	DDRC1 Data 0	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ1	DDRC1 Data 1	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ2	DDRC1 Data 2	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ3	DDRC1 Data 3	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ4	DDRC1 Data 4	DDR-IO	—	B	—	OPEN	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC1_DQ5	DDRC1 Data 5	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ6	DDRC1 Data 6	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ7	DDRC1 Data 7	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ8	DDRC1 Data 8	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ9	DDRC1 Data 9	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ10	DDRC1 Data 10	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ11	DDRC1 Data 11	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ12	DDRC1 Data 12	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ13	DDRC1 Data 13	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ14	DDRC1 Data 14	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ15	DDRC1 Data 15	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ16	DDRC1 Data 16	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ17	DDRC1 Data 17	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ18	DDRC1 Data 18	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ19	DDRC1 Data 19	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ20	DDRC1 Data 20	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ21	DDRC1 Data 21	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ22	DDRC1 Data 22	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ23	DDRC1 Data 23	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ24	DDRC1 Data 24	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ25	DDRC1 Data 25	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ26	DDRC1 Data 26	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ27	DDRC1 Data 27	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ28	DDRC1 Data 28	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ29	DDRC1 Data 29	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ30	DDRC1 Data 30	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ31	DDRC1 Data 31	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ32	DDRC1 Data 32	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ33	DDRC1 Data 33	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ34	DDRC1 Data 34	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ35	DDRC1 Data 35	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ36	DDRC1 Data 36	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ37	DDRC1 Data 37	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ38	DDRC1 Data 38	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ39	DDRC1 Data 39	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ40	DDRC1 Data 40	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ41	DDRC1 Data 41	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ42	DDRC1 Data 42	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ43	DDRC1 Data 43	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ44	DDRC1 Data 44	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ45	DDRC1 Data 45	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ46	DDRC1 Data 46	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ47	DDRC1 Data 47	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ48	DDRC1 Data 48	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ49	DDRC1 Data 49	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ50	DDRC1 Data 50	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ51	DDRC1 Data 51	DDR-IO	—	B	—	OPEN	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC1_DQ52	DDRC1 Data 52	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ53	DDRC1 Data 53	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ54	DDRC1 Data 54	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ55	DDRC1 Data 55	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ56	DDRC1 Data 56	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ57	DDRC1 Data 57	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ58	DDRC1 Data 58	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ59	DDRC1 Data 59	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ60	DDRC1 Data 60	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ61	DDRC1 Data 61	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ62	DDRC1 Data 62	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQ63	DDRC1 Data 63	DDR-IO	—	B	—	OPEN	✓	—
DDRC1_DQSN0	DDRC1 Data Strobe 0	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP0			—	B	—	OPEN	✓	—
DDRC1_DQSN1	DDRC1 Data Strobe 1	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP1			—	B	—	OPEN	✓	—
DDRC1_DQSN2	DDRC1 Data Strobe 2	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP2			—	B	—	OPEN	✓	—
DDRC1_DQSN3	DDRC1 Data Strobe 3	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP3			—	B	—	OPEN	✓	—
DDRC1_DQSN4	DDRC1 Data Strobe 4	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP4			—	B	—	OPEN	✓	—
DDRC1_DQSN5	DDRC1 Data Strobe 5	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP5			—	B	—	OPEN	✓	—
DDRC1_DQSN6	DDRC1 Data Strobe 6	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP6			—	B	—	OPEN	✓	—
DDRC1_DQSN7	DDRC1 Data Strobe 7	DDR-DQS	—	B	—	OPEN	✓	—
DDRC1_DQSP7			—	B	—	OPEN	✓	—
DDRC1_ZQ	Reference Input for DDRC1 Calibration	DDR-ZQ	—	I	—	OPEN	✓	—
DDRC1_VREF0	DDRC1 Reference Voltage Input 0 (DDRC1_VDDO × 0.5 V)	DDR-VREF	—	I	—	GND	✓	—
DDRC1_VREF1	DDRC1 Reference Voltage Input 1 (DDRC1_VDDO × 0.5 V)	DDR-VREF	—	I	—	GND	✓	—
DDRC1_VREF2	DDRC1 Reference Voltage Input 2 (DDRC1_VDDO × 0.5 V)	DDR-VREF	—	I	—	GND	✓	—
DDRC1_VREF3	DDRC1 Reference Voltage Input 3 (DDRC1_VDDO × 0.5 V)	DDR-VREF	—	I	—	GND	✓	—
DDRC1_TEST0	DDRC1 Test Signal (This pin should be OPEN.)	—	—	—	—	OPEN	✓	—
DDRC1_TEST1	DDRC1 Test Signal (This pin should be OPEN.)	—	—	—	—	OPEN	✓	—

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Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
DDRC1_TEST2	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST3	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST4	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST5	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST6	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST7	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST8	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST9	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST10	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST11	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST12	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST13	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—
DDRC1_TEST14	DDRC1 Test Signal (This pin should be OPEN).	—	—	—	—	OPEN	✓	—

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2.1.6. General Purpose I/O

Table 2.11 List of General Purpose I/O Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
GPIO0	GPIO Data 0 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO1	GPIO Data 1 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO2	GPIO Data 2 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO3	GPIO Data 3 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO4	GPIO Data 4 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO5	GPIO Data 5 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO6	GPIO Data 6 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO7	GPIO Data 7 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO8	GPIO Data 8 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO9	GPIO Data 9 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO10	GPIO Data 10 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO11	GPIO Data 11 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO12	GPIO Data 12 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO13	GPIO Data 13 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO14	GPIO Data 14 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO15	GPIO Data 15 (with pin share)	BD84	IE	B	PD	OPEN	✓	✓
GPIO16	GPIO Data 16 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO17	GPIO Data 17 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO18	GPIO Data 18 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO19	GPIO Data 19 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO20	GPIO Data 20 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO21	GPIO Data 21 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO22	GPIO Data 22 (with pin share)	BD84	IE	B	PD	OPEN	✓	—
GPIO23	GPIO Data 23 (with pin share)	BD84	IE	B	PD	OPEN	✓	—

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General purpose I/O pins share pins with the following functions. As shown in "Table 2.12 List of Share Pins of General Purpose I/O Pins." Functions can be selected by the register settings.

Table 2.12 List of Share Pins of General Purpose I/O Pins

Symbol	Functions								
	Timer Module (TIMER)			UART Interface (UART0-3)		I2C Interface (I2C0-3)	SPI Interface (SPI0-3)		PCM Interface (PCMIF)
	TIMER GTI / GTO	TIMER PWM	TIMER DPG	UART w/o AFC (Note 1)	UART w/ AFC (Note 2)	I2C	SPI MASTER	SPI SLAVE	PCMIF
GPIO0	TIMER_GTI0	TIMER_PWM0_N	DPG	UART0_RXD	UART1_CTS1_N	I2C0_SDA	SPI0_SDO	SPI0_SDO	PCMIF_LRCKI
GPIO1	TIMER_GTI1	TIMER_PWM1_N	(GPIO1)	UART0_TXD	UART1_RTS1_N	I2C0_SCL	SPI0_SDI	SPI0_SDI	PCMIF_BCKI
GPIO2	TIMER_GTO0	TIMER_PWM2_N	(GPIO2)	UART1_RXD	UART1_RXD	I2C1_SDA	SPI0_SCK	SPI0_SCK	PCMIF_DI
GPIO3	TIMER_GTO1	TIMER_PWM3_N	(GPIO3)	UART1_TXD	UART1_TXD	I2C1_SCL	SPI0_SCS_N	SPI0_SCS_N	(GPIO3)
GPIO4	TIMER_GTI2	TIMER_PWM0_N	(GPIO4)	UART2_RXD	UART3_CTS3_N	I2C2_SDA	SPI1_SDO	SPI1_SDO	(GPIO4)
GPIO5	TIMER_GTI3	TIMER_PWM1_N	(GPIO5)	UART2_TXD	UART3_RTS3_N	I2C2_SCL	SPI1_SDI	SPI1_SDI	(GPIO5)
GPIO6	TIMER_GTO2	TIMER_PWM2_N	(GPIO6)	UART3_RXD	UART3_RXD	I2C3_SDA	SPI1_SCK	SPI1_SCK	(GPIO6)
GPIO7	TIMER_GTO3	TIMER_PWM3_N	(GPIO7)	UART3_TXD	UART3_TXD	I2C3_SCL	SPI1_SCS_N	SPI1_SCS_N	(GPIO7)
GPIO8	TIMER_GTI0	TIMER_PWM0_N	DPG	UART1_RXD	UART0_CTS0_N	I2C0_SDA	SPI2_SDO	SPI2_SDO	PCMIF_LRCKI
GPIO9	TIMER_GTI1	TIMER_PWM1_N	(GPIO9)	UART1_TXD	UART0_RTS0_N	I2C0_SCL	SPI2_SDI	SPI2_SDI	PCMIF_BCKI
GPIO10	TIMER_GTO0	TIMER_PWM2_N	(GPIO10)	UART0_RXD	UART0_RXD	I2C1_SDA	SPI2_SCK	SPI2_SCK	PCMIF_DI
GPIO11	TIMER_GTO1	TIMER_PWM3_N	(GPIO11)	UART0_TXD	UART0_TXD	I2C1_SCL	SPI2_SCS_N	SPI2_SCS_N	(GPIO11)
GPIO12	TIMER_GTI2	TIMER_PWM0_N	(GPIO12)	UART3_RXD	UART2_CTS2_N	I2C2_SDA	SPI3_SDO	SPI3_SDO	(GPIO12)
GPIO13	TIMER_GTI3	TIMER_PWM1_N	(GPIO13)	UART3_TXD	UART2_RTS2_N	I2C2_SCL	SPI3_SDI	SPI3_SDI	(GPIO13)
GPIO14	TIMER_GTO2	TIMER_PWM2_N	(GPIO14)	UART2_RXD	UART2_RXD	I2C3_SDA	SPI3_SCK	SPI3_SCK	(GPIO14)
GPIO15	TIMER_GTO3	TIMER_PWM3_N	(GPIO15)	UART2_TXD	UART2_TXD	I2C3_SCL	SPI3_SCS_N	SPI3_SCS_N	(GPIO15)
GPIO16	TIMER_GTI0	TIMER_PWM0_N	DPG	UART0_RXD	UART1_CTS1_N	I2C0_SDA	—	—	PCMIF_LRCKI
GPIO17	TIMER_GTI1	TIMER_PWM1_N	(GPIO17)	UART0_TXD	UART1_RTS1_N	I2C0_SCL	—	—	PCMIF_BCKI
GPIO18	TIMER_GTO0	TIMER_PWM2_N	(GPIO18)	UART1_RXD	UART1_RXD	I2C1_SDA	—	—	PCMIF_DI
GPIO19	TIMER_GTO1	TIMER_PWM3_N	(GPIO19)	UART1_TXD	UART1_TXD	I2C1_SCL	—	—	(GPIO19)
GPIO20	TIMER_GTI2	TIMER_PWM0_N	(GPIO20)	UART2_RXD	UART3_CTS3_N	I2C2_SDA	—	—	(GPIO20)
GPIO21	TIMER_GTI3	TIMER_PWM1_N	(GPIO21)	UART2_TXD	UART3_RTS3_N	I2C2_SCL	—	—	(GPIO21)
GPIO22	TIMER_GTO2	TIMER_PWM2_N	(GPIO22)	UART3_RXD	UART3_RXD	I2C3_SDA	—	—	(GPIO22)
GPIO23	TIMER_GTO3	TIMER_PWM3_N	(GPIO23)	UART3_TXD	UART3_TXD	I2C3_SCL	—	—	(GPIO23)

Note 1: UART w/o AFC: UART function without Flow control.
Note 2: UART w/ AFC: UART function with Flow control.

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2.1.7. I2C Interface

Table 2.13 List of I2C Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
I2C4_SCL	I2C Bus 4 SCL	BD42	IE	B	PU	OPEN	✓	—
I2C4_SDA	I2C Bus 4 SDA	BD42	IE	B	PU	OPEN	✓	—
I2C5_SCL	I2C Bus 5 SCL	BD42	IE	B	PU	OPEN	✓	—
I2C5_SDA	I2C Bus 5 SDA	BD42	IE	B	PU	OPEN	✓	—
I2C6_SCL	I2C Bus 6 SCL	BD42	IE	B	PU	OPEN	✓	—
I2C6_SDA	I2C Bus 6 SDA	BD42	IE	B	PU	OPEN	✓	—
I2C7_SCL	I2C Bus 7 SCL	BD42	IE	B	PU	OPEN	✓	—
I2C7_SDA	I2C Bus 7 SDA	BD42	IE	B	PU	OPEN	✓	—

Note: All signals are shared with the general purpose I/O pin with the exception of the signals other than the above: I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, I2C2_SCL, I2C2_SDA, I2C3_SCL and I2C3_SDA. For details about sharing pins, refer to "Table 2.12 List of Share Pins of General Purpose I/O Pins."

2.1.8. PCM Interface

Table 2.14 List of PCM Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
PCMIF_CKO	PCMIF Reference Clock	BD42	IE	O	PD	OPEN	✓	✓
PCMIF_BCKO	PCMIF Bit Clock (for output systems)	BD42	IE	B	PD	OPEN	✓	✓
PCMIF_LRCKO	PCMIF Channel Clock (for output systems)	BD42	IE	B	PD	OPEN	✓	✓
PCMIF_DO	PCMIF Data (for output systems)	BD42	IE	O	PD	OPEN	✓	✓

Note: All signals are shared with the general purpose I/O pin with the exception of those other than the above: PCMIF_BCKI, PCMIF_LRCKI and PCMIF_DI. For details about sharing pins, refer to "Table 2.12 List of Share Pins of General Purpose I/O Pins."

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2.1.9. CAN Interface and CAN FD Interface

- The each pin of CAN0_RX, CAN0_TX, CAN1_RX and CAN1_TX of TMPV7602XBG is shared with the CAN FD interface. Functions can be selected by the register setting.

Table 2.15 List of CAN Interface Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
CAN0_RX	CAN0 Receive Data (pin sharing with CANFD0_RX)	BD42	IE	I	PU	OPEN	✓	✓
CAN0_TX	CAN0 Transmit Data (pin sharing with CANFD0_TX)	BD42	IE	O	PU	OPEN	✓	✓
CAN1_RX	CAN1 Receive Data (pin sharing with CANFD1_RX)	BD42	IE	I	PU	OPEN	✓	✓
CAN1_TX	CAN1 Transmit Data (pin sharing with CANFD1_TX)	BD42	IE	O	PU	OPEN	✓	✓
CAN2_RX	CAN2 Receive Data	BD42	IE	I	PU	OPEN	✓	—
CAN2_TX	CAN2 Transmit Data	BD42	IE	O	PU	OPEN	✓	—

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2.1.10. Debugging Support

Contact us if you develop debugging support tools, such as ICE, using a debug support signal.

Table 2.16 List of Debugging Support Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
MEP_TDI	JTAG data input for CMEP / VENEZIA (When connected to ICE, pull up by a resistor of 1 kΩ).	BD42	—	I	—	VDD33	✓	✓
MEP_TDO	JTAG data output for CMEP / VENEZIA (When connected to ICE, pull down by a resistor of 470 kΩ).	BD84	—	B	PD	OPEN or PD (Note 1)	✓	✓
MEP_TCK	JTAG clock input for CMEP / VENEZIA (When connected to ICE, pull down by a resistor of 1 kΩ).	BD42	—	I	—	VDD33	✓	✓
MEP_TMS	JTAG mode select for CMEP / VENEZIA (When connected to ICE, pull up by a resistor of 1 kΩ).	BD42	—	I	—	VDD33	✓	✓
MEP_TRST_N	JTAG reset input for CMEP / VENEZIA (When connected to ICE, pull up by a resistor of 1 kΩ).	BD42	—	I	—	VDD33	✓	✓
DBGUART_RXD	UART receive data for debugging	BD42	IE	I	PU	OPEN	✓	✓
DBGUART_TXD	UART transmit data for debugging	BD42	IE	O	PU	OPEN	✓	✓

Note 1: In the case of PD, pull down with a resistance value of approximately 1kΩ.

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2.1.11. Others

Table 2.17 List of Other Pins

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	TMPV760 Series	
							7608	7602
RESET_N	Reset Input	BD42	—	I	—	—	✓	✓
NMI_N	NMI Request Input	BD42	—	I	—	VDD33	✓	✓
ALARM_0	ALARM Output 0	BD42	—	O	PU	OPEN	✓	✓
ALARM_1	ALARM Output 1	BD42	—	O	PD	OPEN	✓	✓
XIN1	OSC1 (main oscillator) Crystal oscillator connect pins (Usually 12 MHz oscillator should be connected).	OSC	—	I	—	—	✓	✓
XOUT1			—	O	—	—	✓	✓
XIN2	OSC2 (sub oscillator) Crystal oscillator connect pins	OSC	—	I	—	PD	✓	✓
XOUT2			—	O	—	OPEN	✓	✓
TEST0	Test Control Signal (This pin should be connected to GND).	BD42	—	I	—	GND	✓	✓
TEST1	Test Control Signal (This pin should be connected to GND).	BD42	—	I	—	GND	✓	✓
TEST2	Test Control Signal (This pin should be connected to GND).	BD42	—	I	—	GND	✓	✓
TESTV	Test Power Supply (This pin should be connected to GND).	—	—	—	—	GND	✓	✓

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2.1.12. Power Supply and Ground

Table 2.18 List of Power Supply and Ground Pins

Symbol	Function	Structure	TMPV760 Series	
			7608	7602
DDRC0_AVD	DDRC0 PHY Power Supply (1.1 V)	A-POWER	✓	✓
DDRC0_VDDO	DDRC0 Power Supply (1.2 V)	A-POWER	✓	✓
DDRC1_AVD	DDRC1 PHY Power Supply (1.1 V)	A-POWER	✓	—
DDRC1_VDDO	DDRC1 Power Supply (1.2 V)	A-POWER	✓	—
MIPI01_AVDD12	MIPI0, MIPI1 DPHY Power Supply (1.2 V)	A-POWER	✓	✓
MIPI23_AVDD12	MIPI2, MIPI3 DPHY Power Supply (1.2 V)	A-POWER	✓	—
PLL1_AVDD11	PLL1 Power Supply (1.1 V)	A-POWER	✓	✓
PLL2_AVDD11	PLL2 Power Supply (1.1 V)	A-POWER	✓	✓
PLL3_AVDD11	PLL3 Power Supply (1.1 V)	A-POWER	✓	✓
PLL4_AVDD11	PLL4 Power Supply (1.1 V)	A-POWER	✓	✓
VDD11	System Power Supply (1.1 V)	POWER	✓	✓
VDD33	System Power Supply (3.3 V)	POWER	✓	✓
VSS	System Ground	GND	✓	✓

Note : When DDRC1 is not used, it is also possible to connect the DDRC1_VDDO to GND. The other power supply pins including MIPI should supply each power supply also at the time of un-using it.

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3. Package Information

3.1. TMPV7608XBG Outline Drawing

- Package name: P-FBGA796-2727-0.80-001

Unit: mm

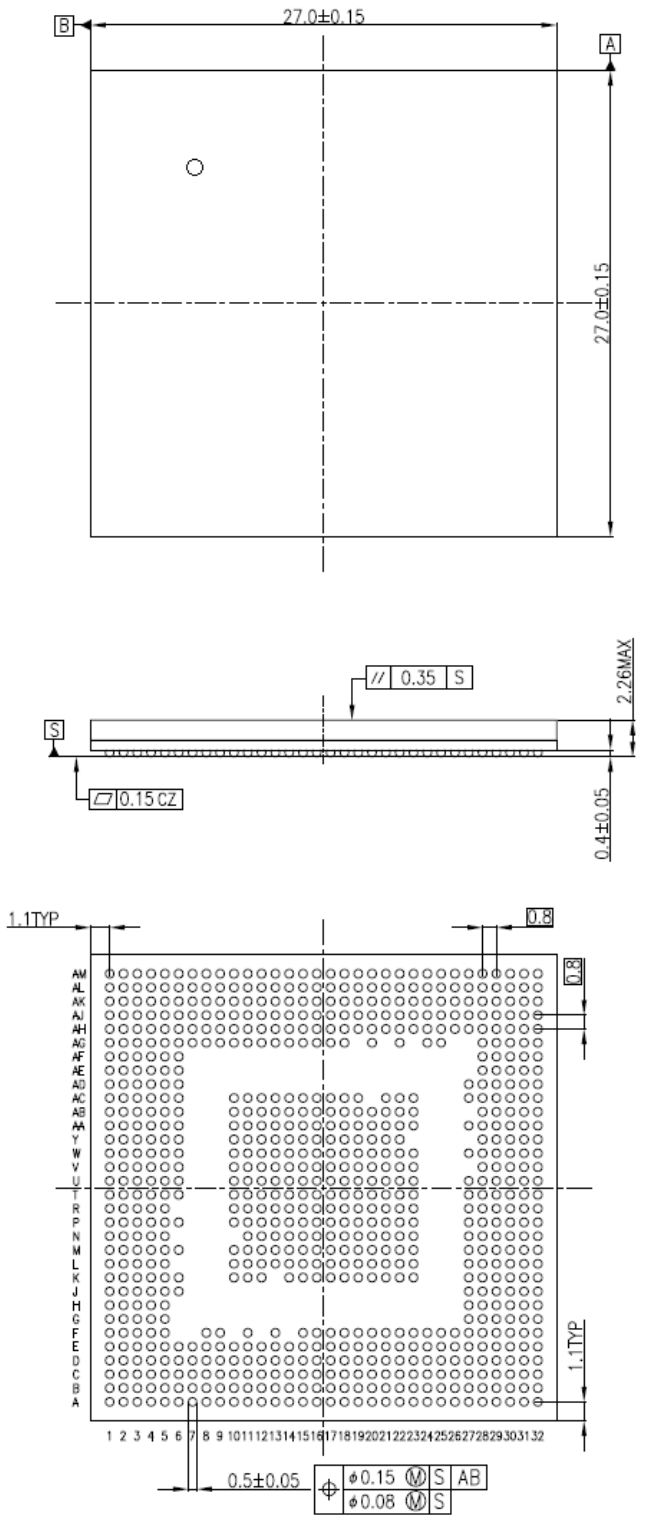

Figure 3.1 TMPV7608XBG Package Outline

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3.2. TMPV7602XBG Outline Drawing (PRELIMINARY)

- Package name: P-LFBGA521-1717-0.65-001

PRELIMINARY

This drawing is subject to change without notice. If you use the information on this drawing, TOSHIBA assumes no liability for your products.

Unit: mm

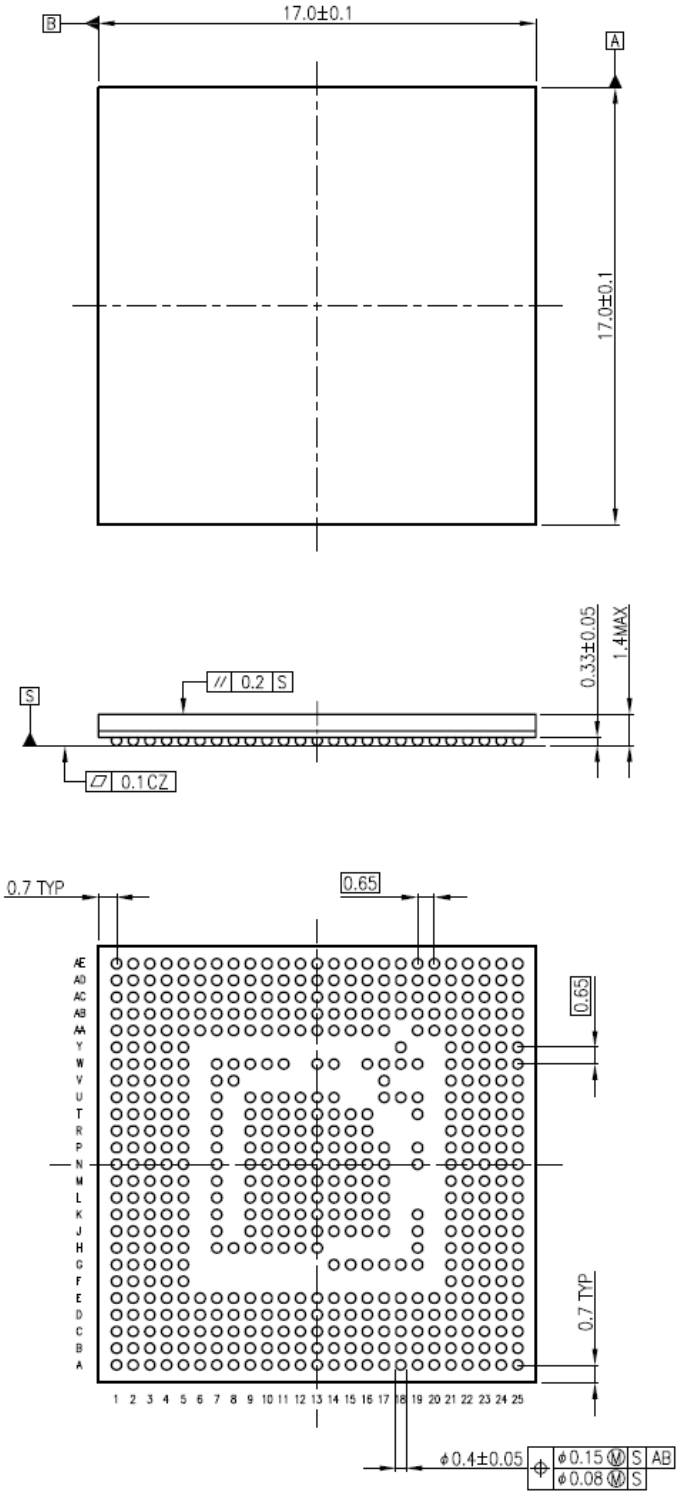

Figure 3.2 TMPV7602XBG Package Outline (PRELIMINARY)

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Revision History

Revision	Date	Description
1.0.0	2016-03-31	Newly Released
1.1.0	2017-03-31	Contents Revised

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