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As part of the acquisition of the non-optical analog/mixed-signal sensor portfolio from ams-OSRAM by Infineon, Infineon is in the process of rebranding all relevant documents.
Due to the large volume of documents, this process will be completed in phases. In the interim, we are providing access to legacy ams-OSRAM documents under the terms of a trademark license agreement.

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Contact:

Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg
Germany

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Product Document

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AS5030

8-Bit Programmable High Speed Magnetic Rotary Encoder

General Description

The AS5030 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°.
It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8 bit = 256 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

In addition to the angle information, the strength of the magnetic field is also available as a 6-bit code.

Data transmission can be configured for 1-wire (PWM), 2-wires (CLK, DIO) or 3-wires (CLK, DIO, CS).

A software programmable (OTP) zero position simplifies assembly as the zero position of the magnet does not need to be mechanically aligned.

A Power Down Mode together with fast startup- and measurement cycles allows for very low average power consumption and makes the AS5030 also suitable for battery operated equipment.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5030, 8-Bit Programmable High Speed Magnetic Rotary Encoder are listed below:

Figure 1:
Added Value of Using AS5030

Benefits	Features
• Complete system-on-chip, no calibration required	• 360° contactless angular position encoding

• Multiple data output formats	• Two digital 8-bit absolute outputs:
	  • Serial interface
	  • Pulse width modulated (PWM) output

• Flexible setup for fitting in almost any application	• User programmable zero position
	• Serial read-out of multiple interconnected AS5030 devices using daisy chain mode

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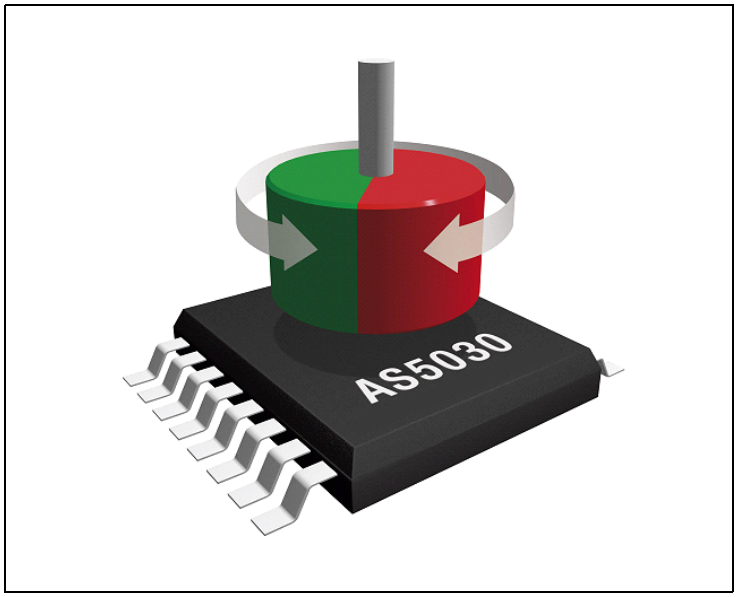
Benefits	Features
• Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic stray fields	• Wide magnetic field input range: 20mT ~ 80mT
	• Wide temperature range: -40°C to 125°C
	• Small Pb-free package: TSSOP 16

Applications

The AS5030 is suitable for Contactless rotary position sensing, Rotary switches (human machine interface), AC/DC motor position control, Robotics and Encoder for battery operated equipment.

Figure 2:
Typical Arrangement of AS5030 and Magnet



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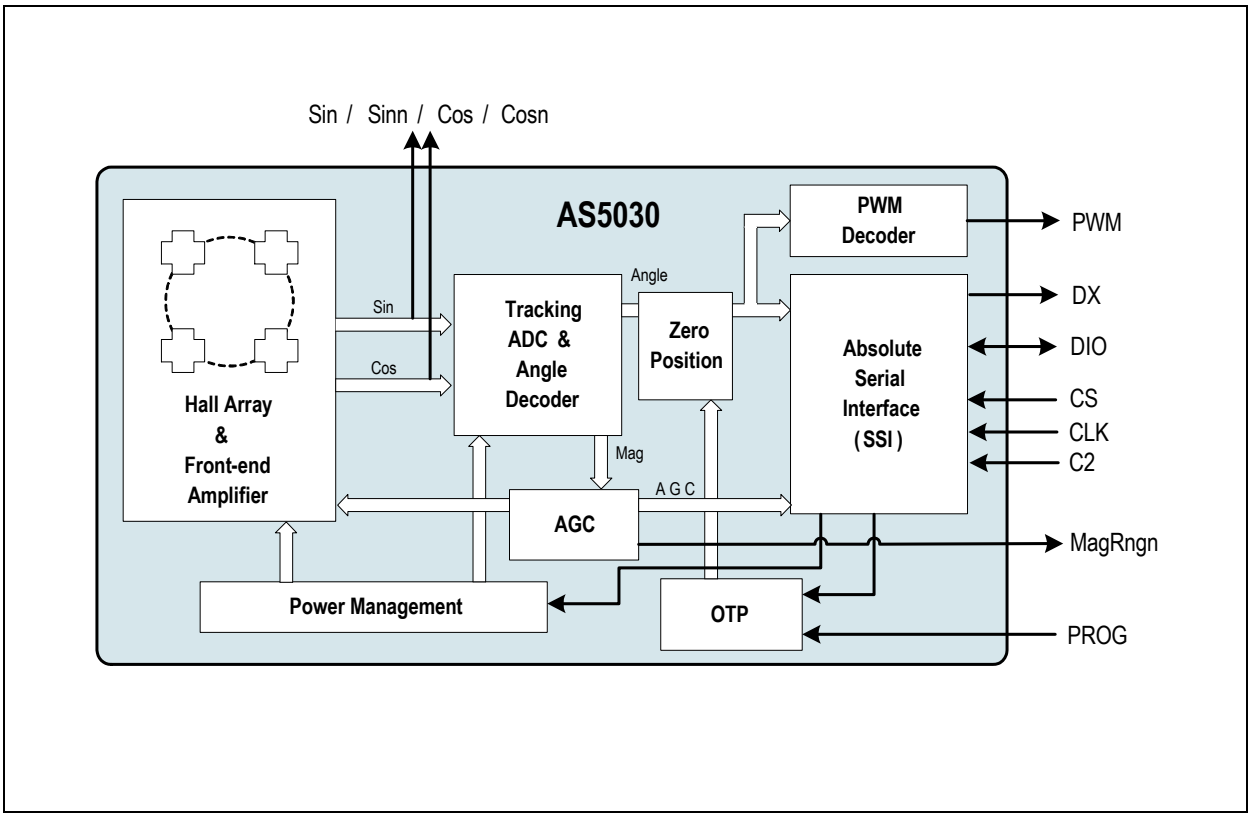
Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS5030 Block Diagram



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Pin Assignments

Figure 4:
Pin Diagram (Top View)

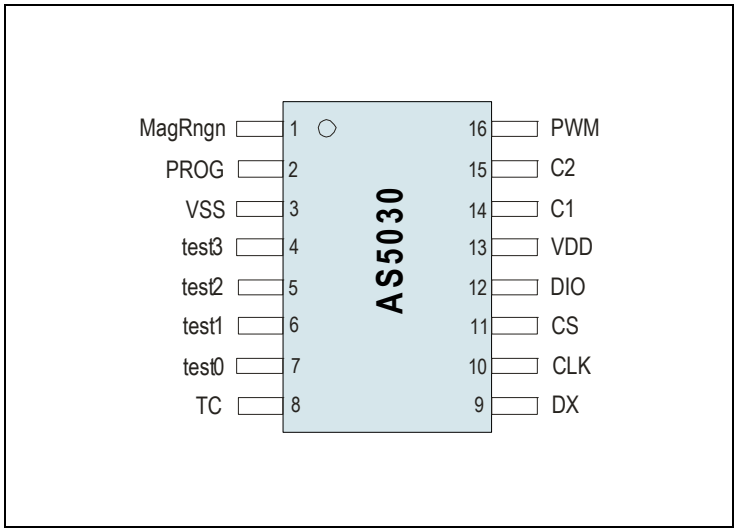

Figure 5:
Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	MagRngn	Digital output / tri-state	Push-Pull output. Is 'HIGH' when the magnetic field strength is too weak, e.g. due to missing magnet
2	PROG	Supply pin	Programming voltage input. Must be left open in normal operation. Maximum load = 20pF (except during programming)
3	VSS		Supply ground
4	T3_SINn	-	This pin is used for factory testing. For normal operation it must be left unconnected. Inverse SIN (Sinn) output in SIN/COS output mode
5	T2_SIN	-	This pin is used for factory testing. For normal operation it must be left unconnected. SIN output in SIN/COS mode
6	T1_COSn	-	This pin is used for factory testing. For normal operation it must be left unconnected. Inverse COS (Cosn) output in SIN/COS mode
7	T0_COS	-	This pin is used for factory testing. For normal operation it must be left unconnected. COS output in SIN/COS mode
8	TC	-	Test pin. Connect to VSS or leave unconnected

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Pin Number	Pin Name	Pin Type	Description
9	DX	Digital output	Digital output for 2-wire operation and Daisy Chain mode
10	CLK	Digital input / Schmitt-Trigger	Clock input of synchronous serial interface; Schmitt-Trigger input
11	CS		Chip Select for serial data transmission, active high; Schmitt-Trigger input, external pull-down resistor (~50kΩ) required in read-only mode
12	DIO	Bi-directional digital pin	Data output / command input for digital serial interface
13	VDD	Supply pin	Positive supply voltage, 4.5V to 5.5V
14	C1	Digital input (standard CMOS; no pull-up or pull-down)	Configuration input: Connect to VSS for normal operation, connect to VDD to enable SIN-COS outputs. This pin is scanned at power-on-reset and at wake-up from one of the Ultra-Low Power Modes
15	C2		Configuration input: Connect to VSS for 3-wire operation, connect to VDD for 2-wire operation. This pin is scanned at power-on-reset and at wake-up from one of the Ultra-Low Power Modes
16	PWM	Digital output	Pulse Width Modulation output, 2µs pulse width per step (2µs ~ 512µs)

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Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply voltage	-0.3	7	V	Except during OTP programming
V_{IN}	Input pin voltage	VSS - 0.5	VDD+ 0.5	V	
I_{scr}	Input current (latch-up immunity)	-100	100	mA	JEDEC 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	MIL 883 E method 3015
Θ_{JA}	Package thermal resistance		137	°C/W	Still Air / Single Layer PCB
			89	°C/W	Still Air / Multilayer PCB
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	150	°C	Min: -67°F; Max: 302°F
T_{BODY}	Body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor time of 168h

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Electrical Characteristics

T_{AMB} = -40°C to 125°C, VDD5V = 4.5V ~ 5.5V, all voltages referenced to VSS, unless otherwise noted.

Figure 7:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Positive supply voltage		4.5		5.5	V
IDD	Operating current	No load on outputs. Minimum AGC (strong magnetic field)		14	18	mA
		No load on outputs. Maximum AGC (weak or no magnetic field)		18	22	
I_{off}	Power-down current	Low Power Mode		1400	2000	µA
		Ultra-Low Power Mode		30	120	
T_{AMB}	Ambient temperature	-40°F ~ 257°F	-40		125	°C

Figure 8:
System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N	Resolution			8		bit
				1.406		°
T_{PwrUp}	Power up time	Startup from zero; AGC not regulated			1000	µs
		Startup from zero until regulated AGC			3300	
		Startup from Power Down Mode			500	
		Startup from Low Power Mode Setting 1: No hysteresis, no reset			46	
		Setting 2: Hysteresis and reset			1500	
t_{da}	Propagation delay	Analog signal path; over full temperature range		15	17	µs
t_{dd}	Tracking rate	Step rate of tracking ADC; 1 step = 1.406°	0.85	1.15	1.45	µs
t_{delay}	Signal processing delay	Total signal processing delay, analog + digital (t_{da} + t_{dd})		16.15	18.45	µs

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
T	Analog filter time constant	Internal low-pass filter	4.1	6.6	12.5	µs
INL_{cm}	Accuracy	Centered magnet	-2		2	°
		Within horizontal displacement radius. See Magnet Specifications	-3		3	
TN	Transition noise	rms (1 sigma)			0.235	°
POR_r	Power-on-reset levels	VDD rising	3.5		4.5	V
POR_f		VDD falling	3.0		4.5	V
Hyst		Hysteresis $\lvert POR_r - POR_f \rvert$		500		mV

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Figure 9:
Magnet Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MD	Magnet diameter	Diametrically magnetized		6		mm
MT	Magnet thickness			2.5		mm
B_i	Magnetic input range	At chip surface, on a radius of 1mm	20		80	mT
v_i	Magnet rotation speed	To maintain locked state			30000	rpm
B_{max}	Magnetic field high detection	T_{AMB}=25°C, AGC @ lower limit, 1 sigma = 2.5mT		52		mT
B_{min}	Magnetic field low detection	T_{AMB}=25°C, AGC @ upper limit, 1 sigma = 1.5mT		23		
	Hall array radius	Over x/y chip center		1		mm
	Vertical distance of magnet	Recommended distance; operation outside this range is possible, accuracy may be reduced	0.5	1	1.8	mm
	Horizontal magnet displacement radius	From diagonal package center			0.25	mm
		From diagonal IC center			0.5	
tk_M	Recommended magnet material and temperature drift	NdFeB Material		-0.12		%/K
		SmCo Material		-0.035		

Note(s):

1. Recommended magnet: NdFeB 35H BR = 12000 Gauss, Ø6mm x 2.5mm.

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Figure 10:
Magnetic Field Alarm Limits

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AGC_{FF}	Magnetic field too low alarm limit	AGC = FF_H untrimmed, 25°C, 1sigma	20.3		23.6	mT
AGC_0	Magnetic field too high alarm limit	AGC = 0_H untrimmed, 25°C, 1sigma	44.5		52.2	mT
	Magnetic field alarm limit trim range	See Hall Element Sensitivity Options	100		121	%
	Temperature coefficient of alarm ranges	Sensitivity increases with temperature which partly compensates the temperature coefficient of the magnet		0.052		%/K

Figure 11:
Hall Element Sensitivity Options

Symbol	Parameter	Conditions	Min	Typ	Max	Units
sens	Hall element sensitivity setting	sens = 00 (default); low sensitivity. See 18-Bit OTP Write Commands		100		%
		sens = 01		106		
		sens = 10		113		
		sens = 11 (high sensitivity)		121		

Figure 12:
Programming Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PROG}	Programming voltage	Static voltage at pin PROG	8.0		8.5	V
I_{PROG}	Programming current				100	mA
$Tamb_{PROG}$	Programming ambient temperature	During programming	0		85	°C
t_{PROG}	Programming time	Timing is internally generated	2		4	µs
$V_{R,prog}$	Analog readback voltage	During analog readback mode at pin PROG			0.5	V
$V_{R,unprog}$			2.2		3.5	

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DC Characteristics of Digital Inputs and Outputs

Figure 13:
CMOS Inputs: CLK, CS, DIO, C1, C2

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIH	High level input voltage		0.7*VDD			V
VIL	Low level input voltage				0.3*VDD	V
I_{LEAK}	Input leakage current				1	µA

Figure 14:
CMOS Outputs: DIO, MagRngn, PWM, DX

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOH	High level output voltage	Source current <4mA	VDD-0.5			V
VOH	Low level output voltage	Sink current <4mA			0.4	V
CL	Capacitive load				35	pF

Figure 15:
CMOS Tristate Output: DIO

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IO_Z	Tristate leakage current	CS = low			1	µA

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Figure 16:
8-Bit PWM Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N_{PWM}	PWM resolution			8		bit
				2		µs/step
PW_{MIN}	PWM pulse width	Angle = 0° (00_H)	1.66	2.26	2.85	µs
PW_{MAX}	PWM pulse width	Angle = 358.6° (FF_H)	427	578	731	µs
PW_P	PWM period	Over full temperature range(1)	428	581	734	µs
f_{PWM}	PWM frequency	1 / PWM period		1.72		kHz
Hyst	Digital hysteresis(2)	At change of rotation direction		1		bit

Note(s):

1. The tolerance of the absolute PWM pulse width and frequency can be eliminated by using the duty cycle $t_{ON}/(t_{ON}+t_{OFF})$ for angle measurement, see 1-Wire PWM Connection.
2. Hysteresis may be temporarily disabled by software, see 16-Bit Write Command.

Figure 17:
Serial 8-Bit Output 3-Wire Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CLK}	Clock frequency	Normal operation			6	MHz
t_{CLK}			166.6			ns
$f_{clk,P}$	Clock frequency	During OTP programming	250		500	kHz

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Figure 18:
Serial 8-Bit Output 2-Wire Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CLK}	Clock frequency	Normal operation	0.1		6	MHz
t_{CLK}			166.6		10000	ns
$f_{clk,P}$	Clock frequency	During OTP programming	250		500	kHz
t_{TO}	Synchronization timeout	Rising edge of CLK to internally generated chip select on pin DX	16.6	27	34.3	ms
Hyst	Digital hysteresis[(1)]	At change of rotation direction		1		bit

Note(s):

1. Hysteresis may be temporarily disabled by software.

Figure 19:
General Data Transmission Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t0	Rising CLK to CS		CLK/2 +0		CLK/2 +50	ns
t1	Chip select to positive edge of CLK		50			ns
t2	Chip select to drive bus externally		0			ns
t3	Setup time command bit data valid to positive edge of CLK		50			ns
t4	Hold time command bit data valid after positive edge of CLK		15			ns
t5	Float time positive edge of CLK for last command bit to bus float				CLK/2 +0	ns
t6	Bus driving time positive edge of CLK for last command bit to bus drive		CLK/2 +0			ns
t7	Setup time data bit data valid to positive edge of CLK		CLK/2 +0		CLK/2 +30	ns
t8	Hold time data bit data valid after positive edge of CLK		CLK/2 +0			ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
t9	Hold time chip select positive edge CLK to negative edge of chip select		CLK/2 +50			ns
t10	Bus floating time negative edge of chip select to float bus				50	ns
t11	Hold time data bit @ write access data valid to positive edge of CLK		50			ns
t12	Hold time data bit @ write access data valid after positive edge of CLK		15			ns
t13	Bus floating time negative edge of chip select to float bus				50	ns
t_{TO}	Timeout period in 2-wire mode (from rising edge of CLK)		20		24	µs

See Figure 21 for the corresponding timing diagram.

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Detailed Description

Connecting the AS5030

The following examples show various ways to connect the AS5030 to an external controller:

Serial 3-Wire R/W Connection

In this mode, the AS5030 is connected to the external controller via three signals:

Chip Select (CS), Clock (CLK) inputs and bi-directional DIO (Data In/Out) output.

The controller sends commands over the DIO pin at the beginning of each data transmission sequence, such as reading the angle or putting the AS5030 in and out of the reduced power modes.

A pull-down resistor is not required. C1 and C2 are hardware configuration inputs. C1 must always be connected to VSS, C2 selects 3-wire mode (C2 = low) or 2-wire mode (C2 = high).

Figure 20:
SSI Read/Write Serial Data Transmission

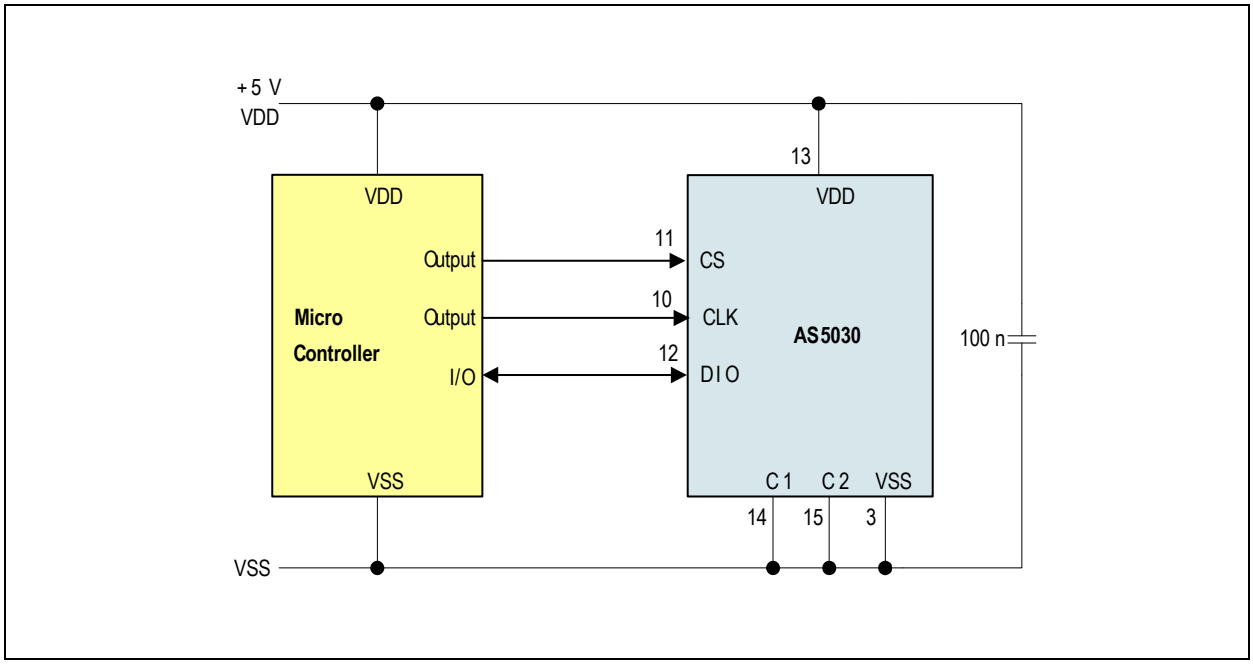

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Figure 21:
Timing Diagram in 3-Wire SSI R/W Mode

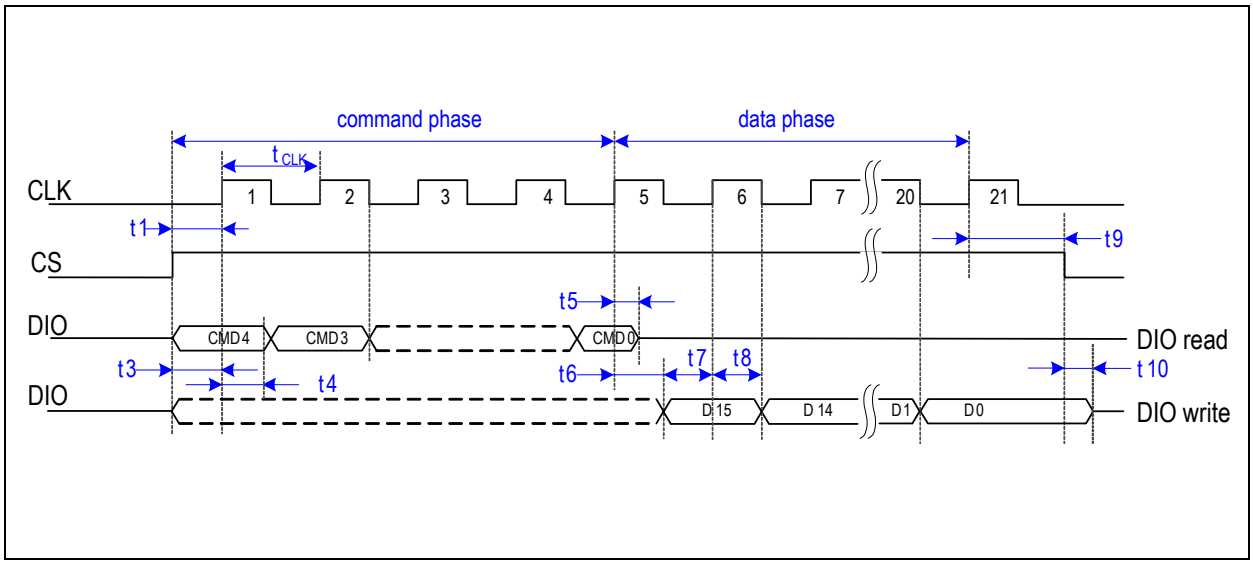

Figure 22:
Serial Bit Sequence (16-bit read/write)

Write Command					Read / Write Data															
C 4	C 3	C 2	C 1	C 0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

Serial 3-Wire Read-Only Connection

If the AS5030 is only used to provide the angular data (no power down or OTP access) this simplified connection is possible. The Chip Select (CS) and Clock (CLK) connection is the same as in the R/W mode, but only a digital input pin (not an I/O pin) is required for the DIO connection.
As the first 5 bits of the data transmission are command bits sent to the AS5030, both the microcontroller and the AS5030 are configured as digital inputs during this phase. Therefore, a pull-down resistor must be added to make sure that the AS5030 reads “00000” as the first 5 bits which sets the Read_Angle command.

All further application examples are shown in R/W mode, however read-only mode is also possible, unless otherwise noted.

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Figure 23:
SSI Read-Only Serial Data Transmission

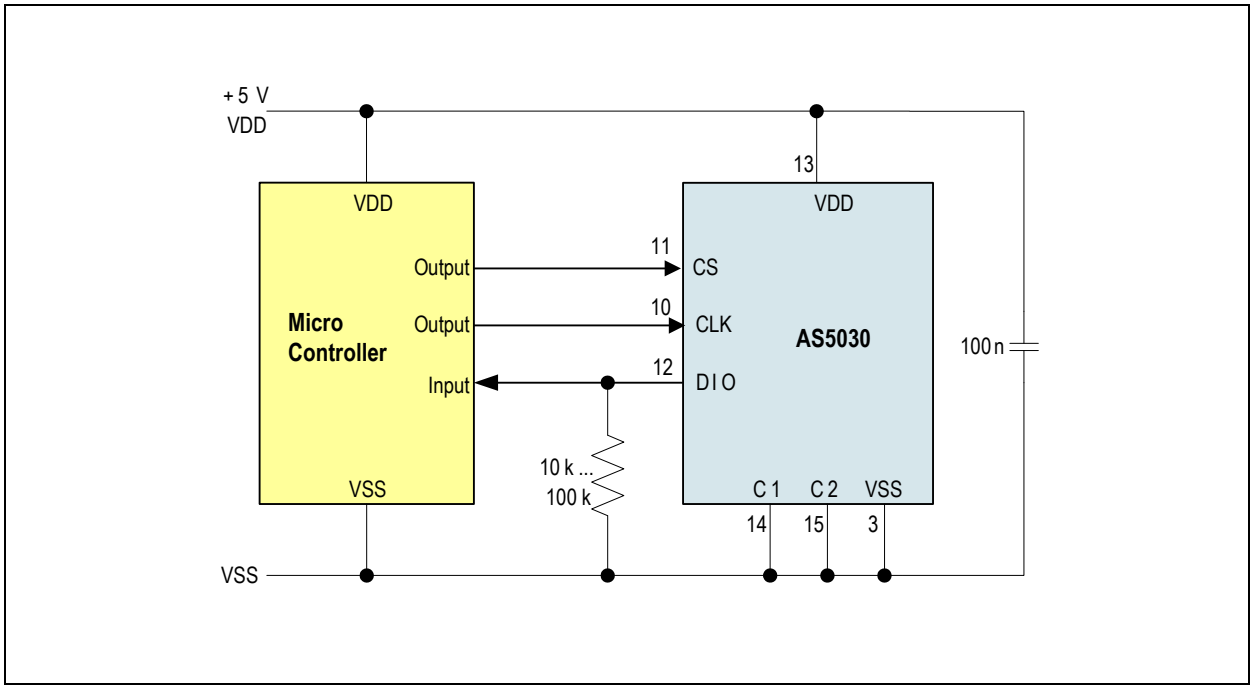

Figure 24:
Timing Diagram in 2-Wire and 3-Wire SSI Mode

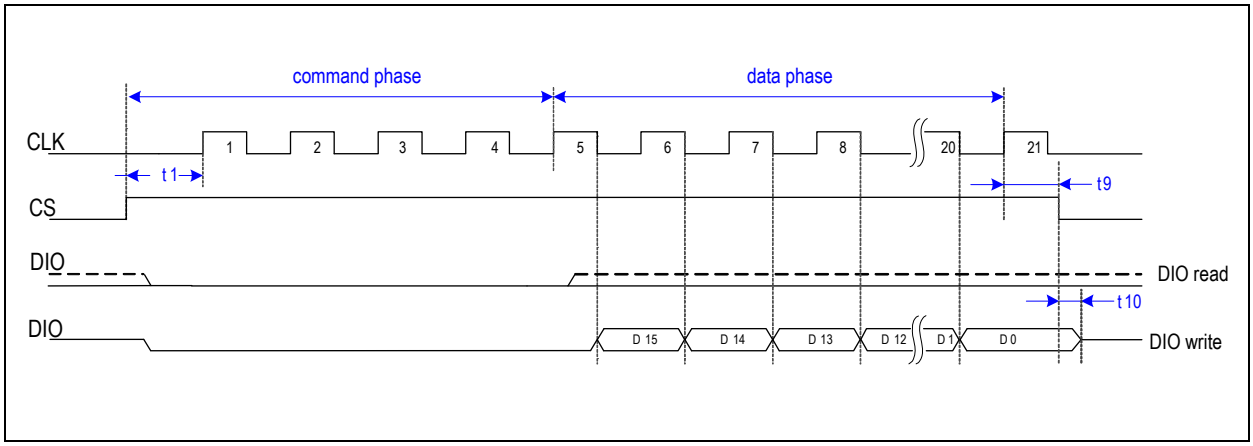

Figure 25:
Serial Bit Sequence (16-bit read/write)

Read																				
D 20	D 19	D 18	D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	C2	lock	AGC						Angle							
							D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

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Serial 2-Wire Connection (R/W Mode)

By connecting the configuration input C2 to VDD, the AS5030 is configured to 2-wire data transmission mode.

Only Clock (CLK) and Data (DIO) signals are required. A Chip Select (CS) signal is automatically generated by the DX output, when a time-out of CLK occurs (typ. 20µs).

Note(s): Read-only mode is also possible in this configuration.

Figure 26:
SSI R/W Mode 2-Wire Data Transmission

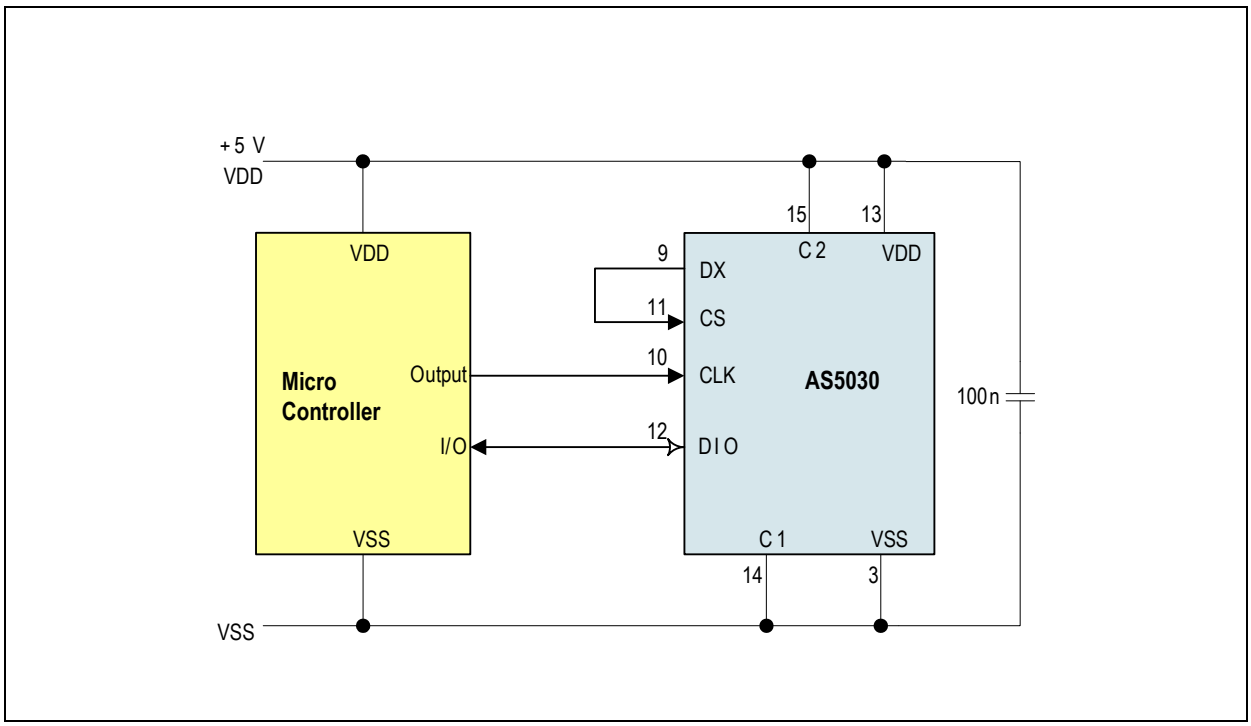
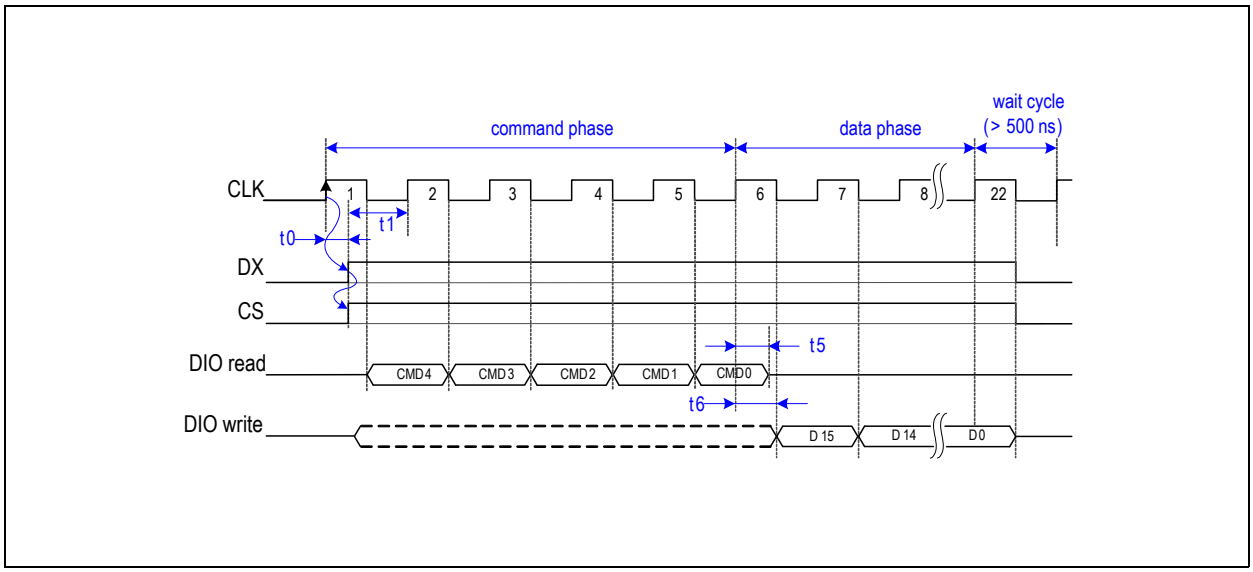


Figure 27:
Timing Diagram in 2-Wire SSI Mode



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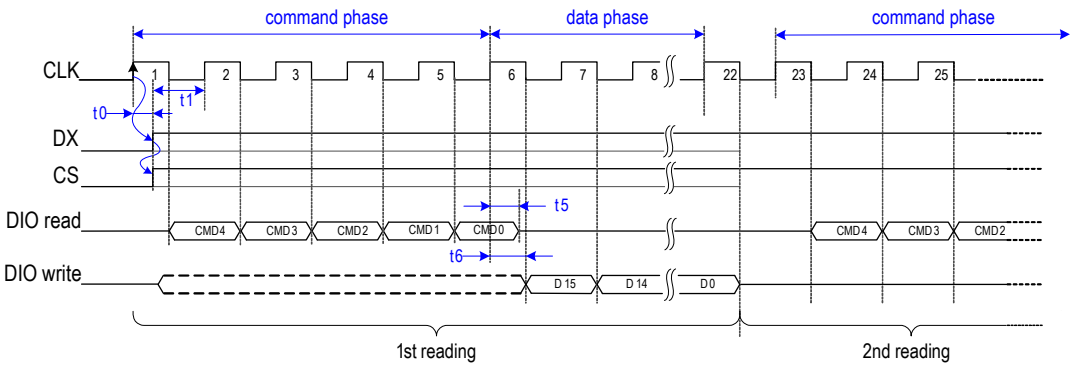
Serial 2-Wire Continuous Readout

The termination of each readout sequence by a timeout of CLK after the 22nd clock pulse as described in Serial 2-Wire Connection (R/W Mode) is the safest method to ensure synchronization, as each timeout of CLK resets the serial interface.

However, it is not mandatory to apply a timeout of CLK and consequently synchronization after each reading. It is also possible to read several consecutive angle values without synchronization by simply continuing the CLK pulses without timeout after the 22nd clock. The 23rd clock is equal to the 1st clock of the next measurement, etc.

This is the fastest way to read multiple angle values, as there is no timeout period between the readings. It is still possible to synchronize the serial data transmission by a timeout of CLK after a given number of readouts (e.g. synchronize after every 5th reading, etc.).

Figure 28:
Timing Diagram in 2-Wire SSI Continuous Readout



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Serial 2-Wire Differential SSI Connection

With the addition of a RS-422 / RS-485 transceiver, a fully differential data transmission, according to the 21-bit SSI interface standard is possible. To be compatible with this standard, the CLK signal must be inverted. This is done by reversing the Data+ and Data- lines of the transceivers.

Note(s): This type of transmission is read-only.

Figure 29:
2-Wire SSI Read-Only Mode

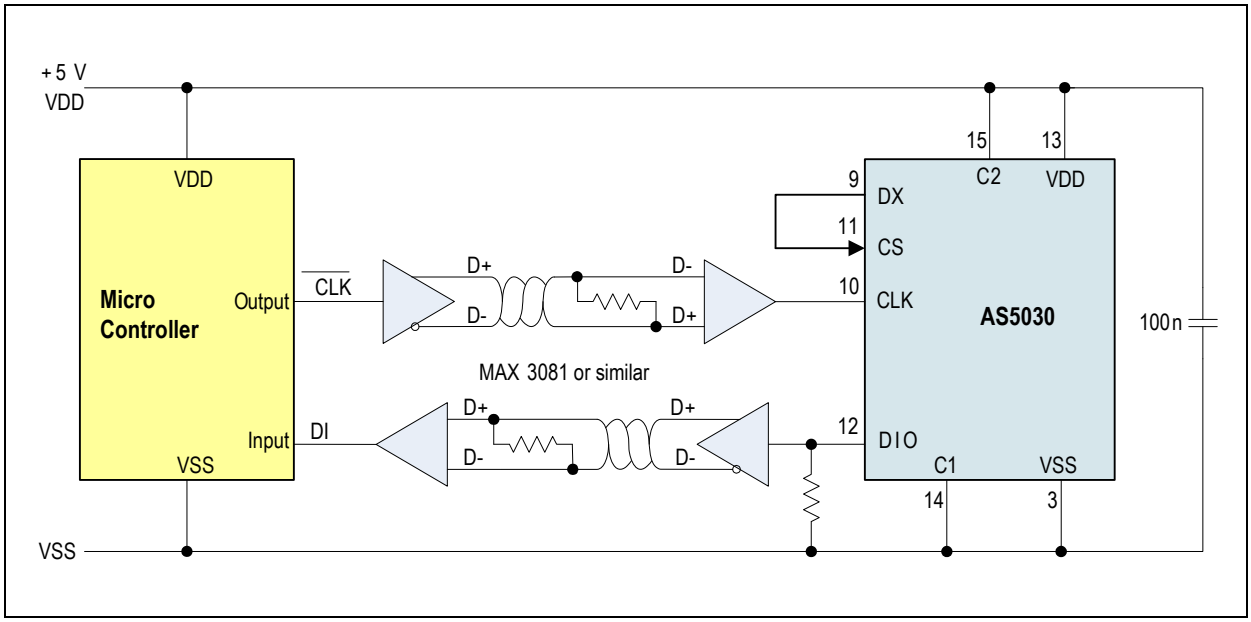

Figure 30:
Timing Diagram in 2-Wire Read-Only Mode (differential transmission)

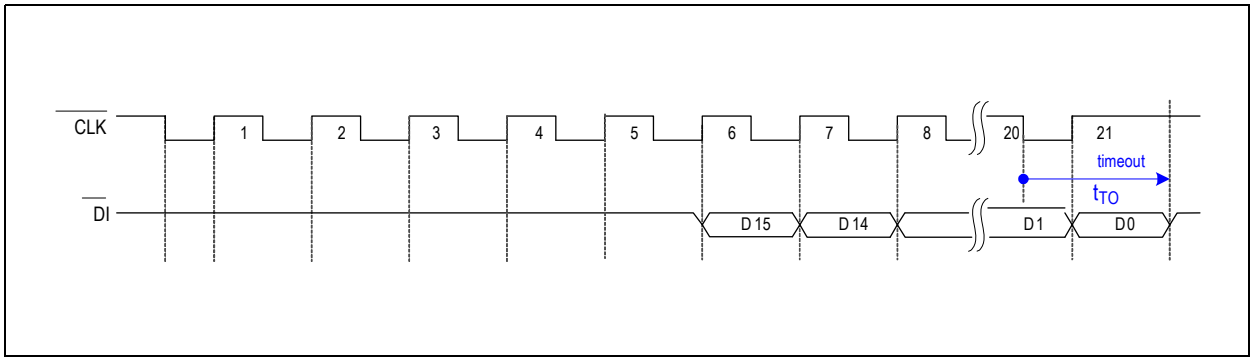

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Figure 31:
SSI Read-Only Serial Bit Sequence (21-bit read)

Read																				
D 20	D 19	D 18	D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	C2	lock	AGC						Angle							
							D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

1-Wire PWM Connection

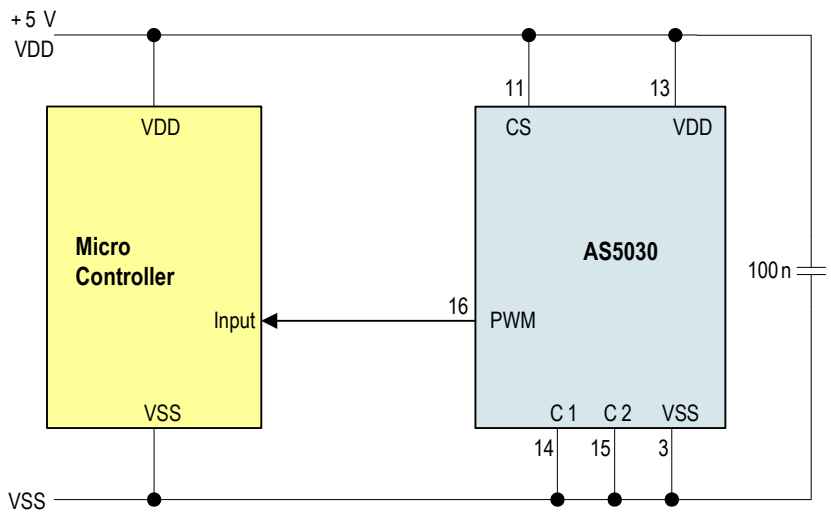
This configuration uses the least number of wires: only one line (PWM) is used for data, leaving the total number of connection to three, including the supply lines. This type of configuration is especially useful for remote sensors.

Ultra-Low Power Mode is not possible in this configuration, as there is no bi-directional data transmission.

If the AS5030 angular data is invalid, the PWM output will remain at low state. Pins that are not shown may be left open.

Note that the PWM output is invalid when the AGC is disabled.

Figure 32:
Data Transmission with Pulse Width Modulated (PWM) Output



The minimum PWM pulse width t_{ON} (PWM = high) is 1 LSB @ 0° (Angle reading = 00_H).

1LSB = nom. 2.26µs.

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The PWM pulse width increases with 1LSB per step. At the maximum angle 358.6° (Angle reading = FF_H), the pulse width t_{ON} (PWM = high) is 256 LSB and the pause width t_{OFF} (PWM = low) is 1 LSB.

This leads to a total period ($t_{ON} + t_{OFF}$) of 257LSB

Figure 33:
PWM Timing

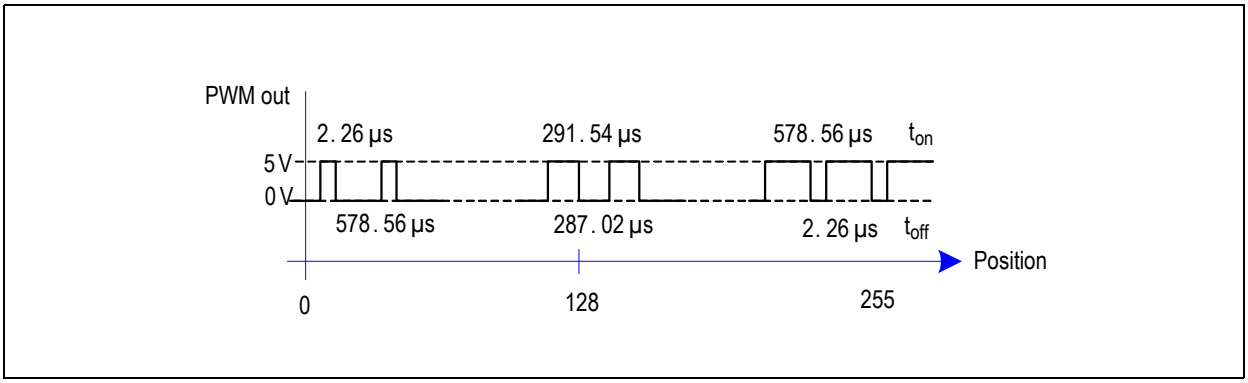

Figure 34:
SSI Read-Only Serial Bit Sequence (21-bit read)

Position	Angle	High	t_high	Low	t_low	Duty-Cycle
0	0°	1	2.26µs	256	578.56µs	0.39%
127	178.59	128	287.02µs	129	291.54µs	49.4%
128	180°	129	291.54µs	128	287.02µs	50.2%
255	358.59°	256	578.56µs	1	2.26µs	99.6%

This means that the PWM pulse width is (position + 1) LSB, where position is 0 …255.

The tolerance of the absolute pulse width and -frequency can be eliminated by calculating the angle with the duty cycle rather than with the absolute pulse width:

(EQ1) $$angle[8-bit] = \left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}}\right) - 1$$

results in an 8-bit value from 00_H to FF_H,

(EQ2) $$angle[°] = \frac{360}{256}\left[\left(257 \frac{t_{ON}}{t_{ON} + t_{OFF}}\right) - 1\right]$$

results in a degree value from 0° ~ 358.6°

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Note(s): The absolute frequency tolerance is eliminated by dividing t_{ON} by (t_{ON}+T_{OFF}), as the change of the absolute timing effects both T_{ON} and T_{OFF} in the same way.

Analog Output

This configuration is similar to the PWM connection (only three lines including supply are required). With the addition of a low-pass filter at the PWM output, this configuration produces an analog voltage that is proportional to the angle.

This filter can be either passive (as shown) or active. The lower the bandwidth of the filter, the less ripple of the analog output can be achieved.

If the AS5030 angular data is invalid, the PWM output will remain at low state and thus the analog output will be 0V. Pins that are not shown may be left open.

Note(s): The PWM output is invalid when the AGC is disabled.

Figure 35:
Data Transmission with Pulse Width Modulated (PWM) Output

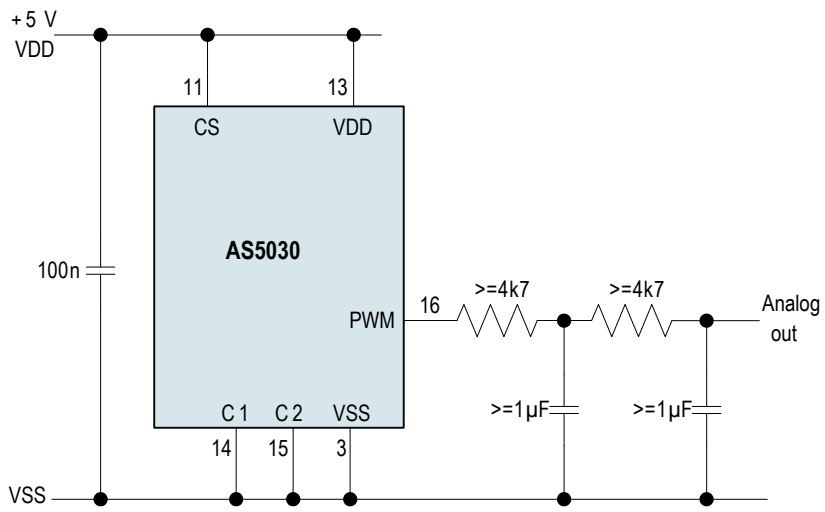

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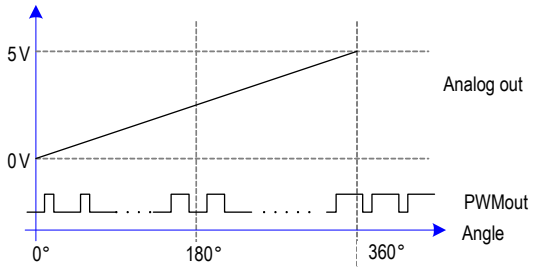
Figure 36:
Relation of PWM/Analog Output with Angle



Analog Sin/Cos Outputs with External Interpolator

By connecting C1 to VDD, the AS5030 provides analog Sine and Cosine outputs (Sin, Cos) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution.

In addition, the inverted Sine and Cosine signals (Sinn, Cosn; see dotted lines) are available for differential signal transmission.

The input resistance of the receiving amplifier or ADC should be greater than 100kΩ. The signal lines should be kept as short as possible, longer lines should be shielded in order to achieve best noise performance.

The SIN / COS / SINn / COSn signals are amplitude controlled to ~1.3Vp (differential) by the internal AGC controller. The DC bias voltage is 2.25V.

If the SIN(n)- and COS(n)- outputs cannot be sampled simultaneously, it is recommended to disable the automatic gain control as the signal amplitudes may be changing between two readings of the external ADC. This may lead to less accurate results.

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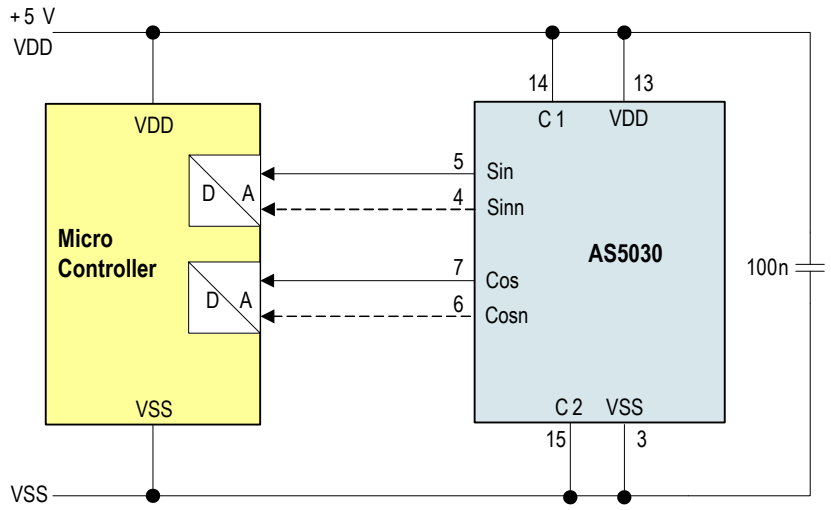
Figure 37:
Sine and Cosine Outputs for External Angle Calculation



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3-Wire Daisy Chain Mode

The Daisy Chain mode allows connection of more than one AS5030 to the same controller interface. Independent of the number of connected devices, the interface to the controller remains the same with only three signals: CSn, CLK and DO. In Daisy Chain mode, the data from the second and subsequent devices is appended to the data of the first device.

The 100nF buffer cap at the supply (shown only for the last device) is recommended for all devices.

The total number of serial bits is: n*21, where n is the number of connected devices: e.g. for 2 devices, the serial bit stream is 42-bits. For three devices it is 63 bits.

Figure 38:
Connection of Devices in 3-Wire Daisy Chain Mode

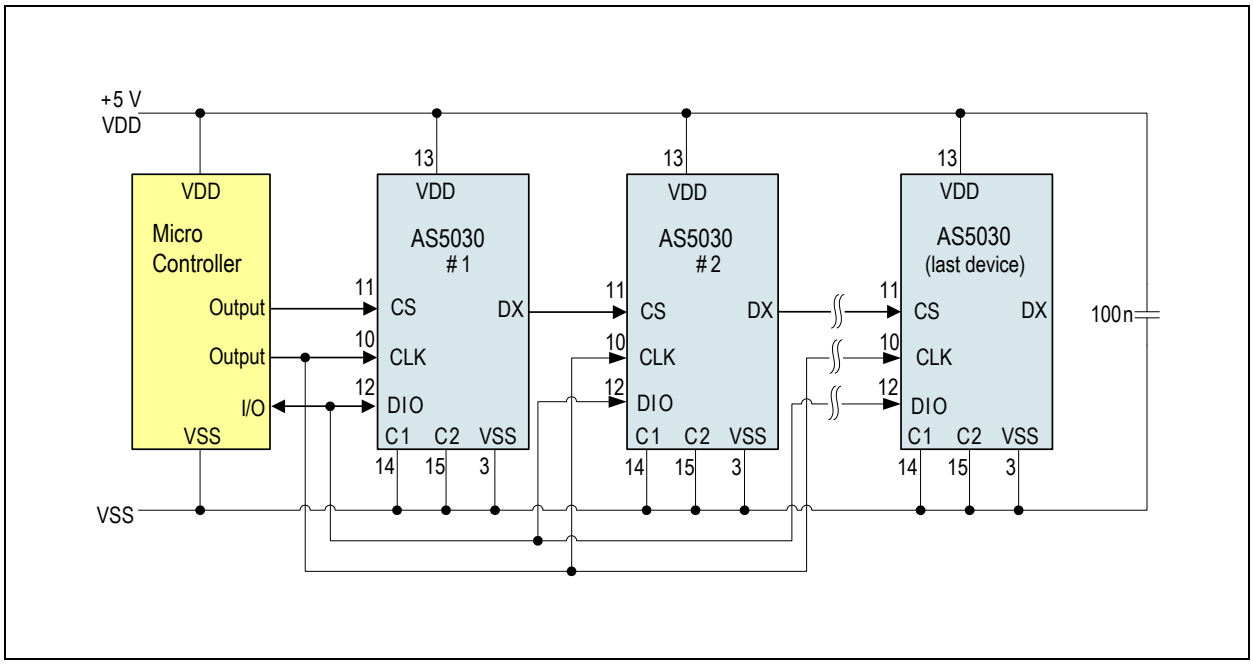
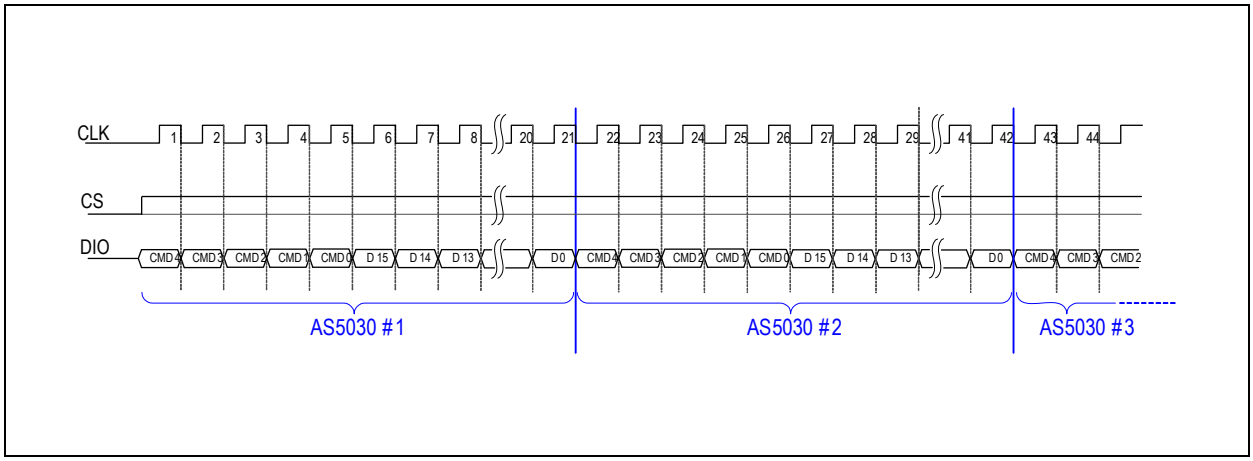


Figure 39:
Timing Diagram in 3-Wire Daisy Chain Mode



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2-Wire Daisy Chain Mode

The AS5030 can also be connected in 2-wire Daisy Chain mode, requiring only two signals (Clock and Data) for any given number of daisy-chained devices. Note that the connection of all devices except the last device is the same as for the 3-wire connection (see Figure 38). The last device must have pin C2 (#15) set to 'high' and feeds the DX signal to CS of the first device.

Again, each device should be buffered with a 100nF cap (shown only for the last device).

The total number of serial bits is: n*21, where n is the number of connected devices. Note that this configuration requires one extra clock (#1) to initiate the generation of the CS signal for the first device. After reading the last device, the communication must be reset back to the first device by introducing a timeout of CLK (no rising edge for >24µs).

Figure 40:
2-Wire Daisy Chain Mode

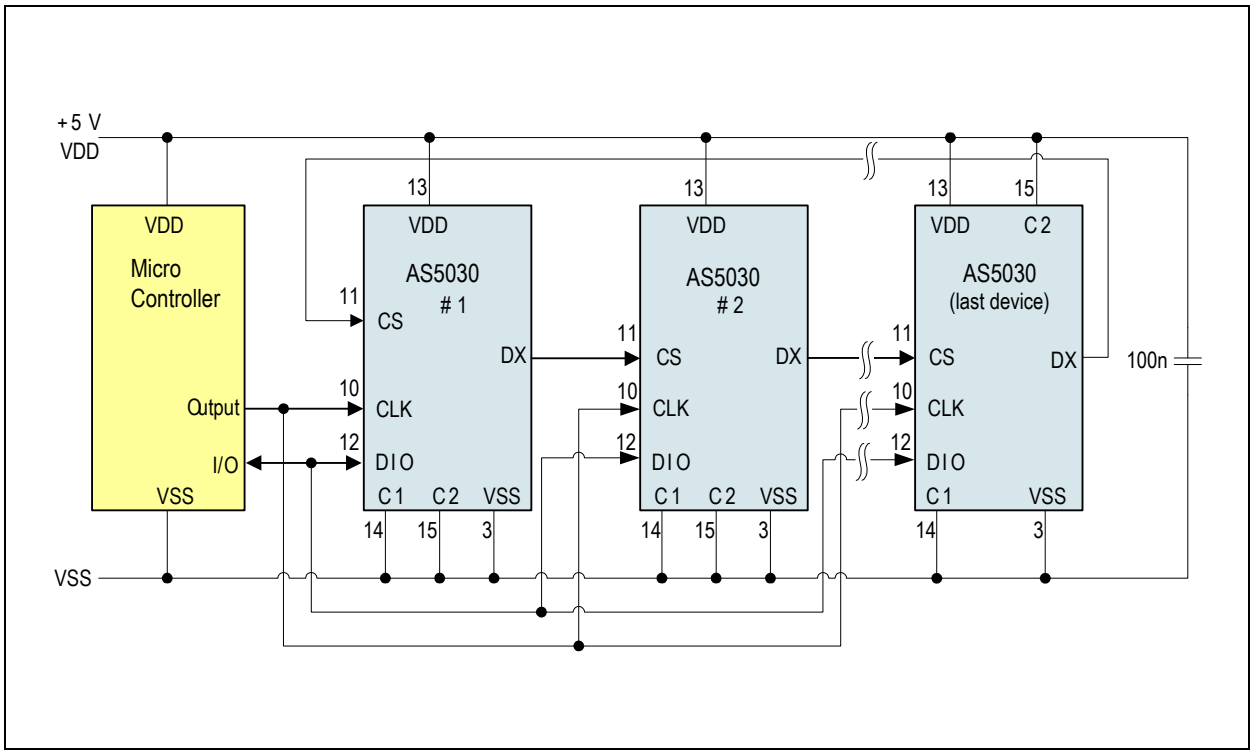

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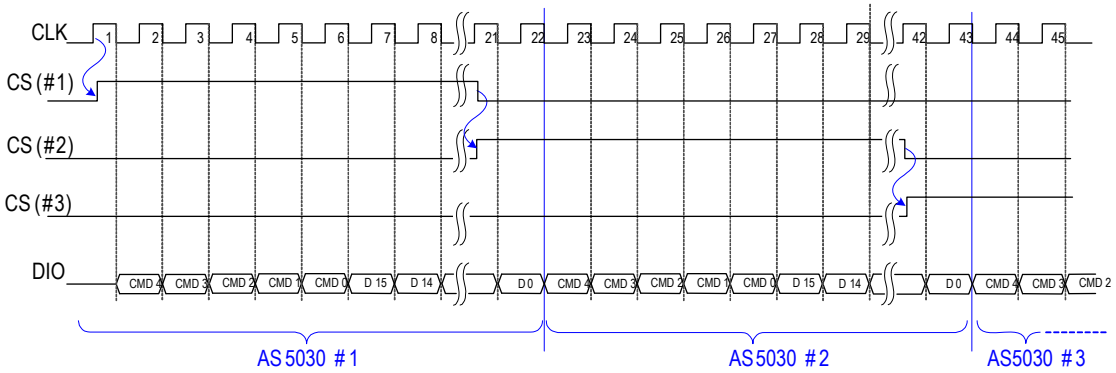
Figure 41:
Timing Diagram in 2-Wire Daisy Chain Mode



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Application Information

Figure 42:
AS5030 Parameter and Features List

Parameter	Description
Supply voltage	5V ± 10%
Supply current	Low Power Mode, non-operational: typ. 1.4mA Ultra-Low Power Mode, non-operational: typ. 30µA Normal operating mode: typ. 14mA.
Absolute output; Serial Interface	21-bit Synchronous Serial Interface (SSI): 5 command bits, 2 data valid bits, 6 data bits for magnetic field strength, 8 data bits for angle. Configurable for 2-wire (Clock, Data) or 3-wire (Chip Select, Clock, Data) operation Daisy Chain mode for reading multiple encoders through a 2- or 3-wire interface. Zero Position Programming (OTP)
SSI clock rate	≤ 6 MHz data clock rate, 250 ~ 500kHz during programming
2-wire readout mode	DIO and CLK signals. 0.1 ~ 6MHz clock rate. Synchronization through time-out of CLK signal.
Power down modes	Activated and deactivated by software commands. Low Power Mode: power down current = 1.4mA typ.; power up time <150µs Ultra-Low Power Mode: power down current = 30µA typ.; power up time <500µs
Digital input cells	CLK, CS = Schmitt trigger inputs
SIN-COS mode	Sine, inverse Sine, Cosine and inverse Cosine outputs. 360° per period.
Maximum speed	30000 rpm with locked ADC
Resolution and accuracy	Resolution = 8-bit (1.406°) Accuracy ≤ ± 2° with centered magnet
Transition noise	0.24°rms (1 sigma)
PWM output	2.26µs / Step, PWM will be permanently low when angular data is not valid (e.g. during startup).
Digital output current	4mA @ VDD = 5V (PWM, DIO, DX, MagRngn outputs)
OTP programming mode	Through serial interface with static programming voltage on pin #2 (PROG) 16-bit OTP programming register. OTP user programming options: Angular zero position: 8 bit Hall element sensitivity: 2 bit
Magnetic field range	Trimmable in four steps with OTP programming (sensitivity) maximum/minimum ratio ~ 2.5:1. Field range window = 20 ~ 80mT (e.g. maximum sensitivity range = 20 ~ 48mT, minimum sensitivity range = 32 ~ 80mT

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Parameter	Description
Non-valid-range indication	By hardware: MagRngn pin indicates locked condition of ADC By software: LOCK1&2 status bits indicate locked condition of ADC
Start-up timings	Start-up time after shutdown < 2ms Start-up time after power-down from Ultra-Low Power Mode: < 500µs Start-up time after power-down from Low Power Mode: < 150µs
ESD protection	± 2kV
Operating temperature	-40°C ~ 125°C

AS5030 Programming

The AS5030 has an integrated 18-bit OTP ROM for configuration purposes.

OTP Programming Options

The OTP programming options can be set permanently by programming or temporarily by overwriting. Both methods are carried out over the serial interface, but with different commands (WRITE OTP, PROG OTP).

Note(s): During the 18-bit OTP programming, each bit needs 4 clock pulses to be validated.

- **Zero Position Programming**
  This programming option allows the user to program any rotation angle of the magnet as the new zero position. This useful feature simplifies the assembly process as the magnet does not need to be mechanically adjusted to the electrical zero position. It can be assembled in any rotation angle and later matched to the mechanical zero position by zero position programming.
  The 8-bit user programmable zero position can be applied both temporarily (command WRITE OTP, #1F_H) or permanently (command PROG OTP, #19$_H$).

- **Magnetic Field Optimization**
  This programming option allows the user to match the vertical distance of the magnet with the optimum magnetic field range of the AS5030 by setting the sensitivity level.
  The 2-bit user programmable sensitivity setting can be applied both temporarily (command WRITE OTP, #1F_H) or permanently (command PROG OTP, #19$_H$).

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Reduced Power Mode Programming Options

These temporary programming options are also carried out over the serial interface.

- **Low Power Mode**
  Low Power Mode is a power saving mode with fast start-up. In Low Power Mode, all internal digital registers are frozen and the power consumption is reduced to max. 1.5mA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 150µs. This mode is recommended for applications, where low power, but fast start-up and short reading cycle intervals are required.
- **Ultra-Low Power Mode**
  Ultra-Low Power Mode is a power saving mode with even reduced power-down current consumption. In this mode, all chip functions are frozen and the power consumption is reduced to max. 50µA. The serial interface remains active. Start-up from this mode to normal operation can be accomplished within 500µs. This mode is recommended for applications, where very low average power consumption is required, e.g. for battery operated equipment. For example, in a cycled operation with 10 readings per second, the average power consumption of the AS5030 can be reduced to only 120µA.

AS5030 Read / Write Commands

Data transmission with the AS5030 is handled over the 2-wire or 3-wire interface. The transmission protocol begins with sending a 5-bit command to the AS5030, followed by reading or writing 16 or 18 bits of data:

16-Bit Read Command

Figure 43:
16-Bit Read Command

Command	Bin	Hex	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
RD ANGLE	00000	00	C2	lock	AGC 5:0						Angle 7:0							

C2 displays status of hardware pin C2 (pin #15)

Lock: Indicates that the AGC is locked. Data is invalid when this bit is 0

AGC: 6-bit AGC register. Indicates the strength of the magnet (e.g. for push-button applications)

000000_b indicates a strong magnetic field

111111_b indicates a weak magnetic field

Ideally, the vertical distance of the magnet should be chosen such that the AGC value is in the middle (around 100000b).

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Angle: 8-bit Angle value; represents the rotation angle of the magnet. One step = 360°/256 = 1.4°.

16-Bit Write Command

These settings are temporary; they cannot be programmed permanently. The settings will be lost when the power supply is removed

Figure 44:
16-Bit Write Command.

Command	Bin	Hex	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
EN PROG	10000	10	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0
SET PWR MODE	10001	11	ULP/ LPn	PSM	0													
DIS HYST	10011	13	HYS	0														
DIS AGC	10101	15	0	0	0	0	0	rst	0	0	0	AGC 5:0						FA

EN PROG: Command must be sent with a fixed 16-bit code ($8CAE_H$) to enable subsequent OTP access.

ULP/LPn: Selects the Ultra-Low Power Mode, when bit PSM is set: 0 = Low Power Mode, 1 = Ultra-Low Power Mode

PSM: Enables power saving modes: 0 = normal operation, 1 = reduced power mode selected by bit ULP/LPn

HYS: Disables the hysteresis of the digital serial and PWM outputs:

0 (default) = 1-bit hysteresis, 1 = no hysteresis

DIS AGC: Disables the automatic gain control. The AGC will be frozen to a gain setting written in bits AGC 5:0 (D6:D1), bit FA must be set.

rst: General Reset: 0 = normal operation, 1 = perform general reset (required after return from reduced power modes)

FA: Freeze AGC; 0 = normal operation, 1= freeze AGC with the values stored in bits AGC 5:0. The PWM output will be invalid when bit FA is set.

18-Bit OTP Read Commands

Note(s): To prohibit unintentional access to the OTP register, OTP PROG/write access is only enabled after the EN PROG command has been sent. OTP access is locked again by sending a RD ANGLE or SET PWR MODE command.

EN PROG need not to be sent before a READ OTP.

During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

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Figure 45:
18-Bit OTP Read Commands

Command	Bin	Hex	D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
READ OTP	011 11	0F	Reserved for factory settings								sens 1:0		Zero position 7:0							
ANALOG OTP RD	010 01	09	Reserved for factory settings								sens 1:0		Zero position 7:0							

READ OTP: Reads the contents of the OTP register in digital form. The reserved area may contain any value.

ANALOG OTP RD: Reads the contents of the OTP register as an analog voltage at pin PROG.

sens: Reads the sensitivity setting of the Hall elements: 00 = low sensitivity, 11 = high sensitivity.

zero position: Reads the programmed zero position; the actual angle of the magnet which is displayed as 000.

18-Bit OTP Write Commands

During the 18bit OTP read/write transfer, each bit needs 4 clock pulses to be validated.

Figure 46:
18-Bit OTP Write Commands

Command	Bin	Hex	D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
WRITE OTP	11111	1F	copy factory settings obtained from READ OTP command								sens 1:0		zero position 7:0							
PROG OTP	11001	19	00000000 reserved for factory settings,								sens 1:0		zero position 7:0							

WRITE OTP: Non-permanent ("soft write") modification of the OTP register. To set the reserved factory settings area properly, a preceding READ OTP command must be made to receive the correct setting for bits D17:D10. The WRITE OTP command must then set these bits in exactly the same way. Improper setting of the factory settings by a WRITE OTP command may cause malfunction of the chip. The OTP register, including the factory settings can be restored to default by a power-up cycle.
For non-permanent writing, a programming voltage at pin PROG (#2) is not required. EN_PROG must be sent before WRITE_OTP to enable OTP.

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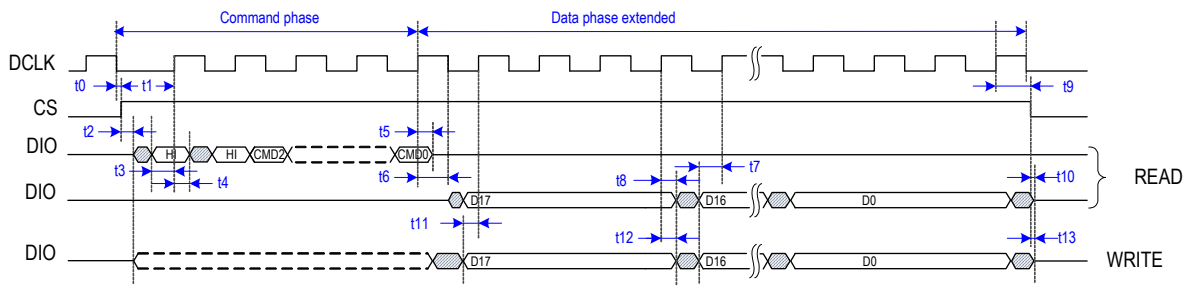
PROG OTP: Permanent modification of the OTP register. An unprogrammed OTP bit contains a '0, programmed bits are 1's. It is possible to program the OTP in several sequences. However, only a 0 can be programmed to 1. Once programmed, an OTP bit cannot be set back to 0. For subsequent programming, bits that are already programmed should be set to 0 to avoid double programming.
During permanent programming, the factory settings D17:D10 should always be set to zero to avoid modification of the factory settings.
Modifying the factory settings may cause irreversible malfunction of the chip.
For permanent programming, a static programming voltage of 8.0-8.5V must be applied at pin PROG (#2). EN_PROG must be sent before PROG_OTP to enable OTP.

sens: Sets the sensitivity setting of the Hall elements:
00: gain factor = 1.65 (low sensitivity)
01: gain factor = 1.75
10: gain factor = 1.86
11: gain factor = 2.00 (high sensitivity)
zero position: Sets the user programmable zero position; the actual angle of the magnet which is displayed as 000.

Figure 47:
Timing Diagram in OTP 18-Bit Read/Write Mode



OTP Programming Connection

Programming of the AS5030 OTP memory does not require a dedicated programming hardware. The programming can be simply accomplished over the serial 3-wire interface (see Figure 48) or the optional 2-wire interface (see Figure 26).

For permanent programming (command PROG OTP, #19_H), a constant DC voltage of 8.0V ~ 8.5V (≥100mA) must be connected to pin #2 (PROG).

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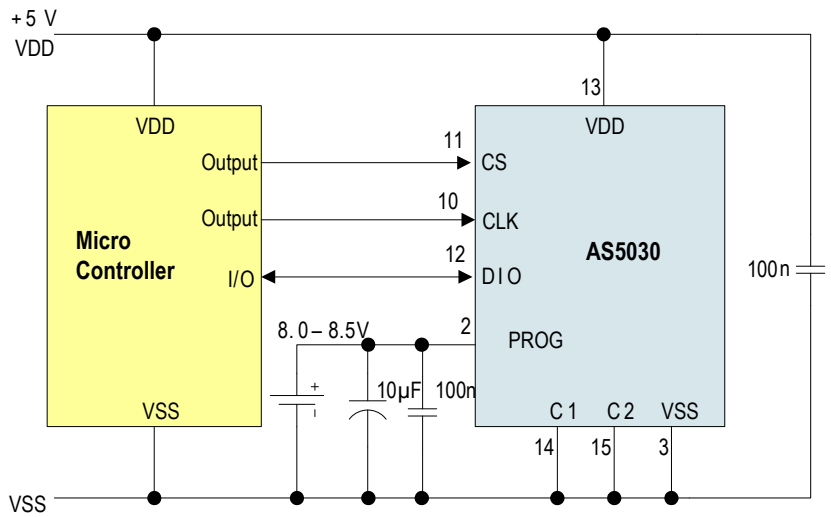
For temporary OTP write ("soft write"; command WRITE OTP, $\#1F_H$), the programming voltage is not required.

To secure unintentional programming, any modification of the OTP memory is only enabled after a special password (command $\#10_H$) has been sent to the AS5030.

Figure 48:
OTP Programming Connection



Programming in Daisy Chain Mode

Programming in Daisy chain mode is possible for both 3-wire and 2-wire mode (see Figure 38 and Figure 40). For temporary programming (soft write), no additional connections are required. Programming is executed with the respective programming commands. For permanent programming, the programming voltage must be applied on pin#2 (PROG) of the device to be programmed. It is also possible to apply the programming voltage simultaneously to all devices, as the actual programming is only executed by a software command.

A parallel connection of all PROG-pins allows digital programming verification but does not allow analog programming verification.

If analog programming verification is required, each PROG pin must be selected individually for verification.

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Programming Verification

After programming, the programmed OTP bits may be verified in two ways:

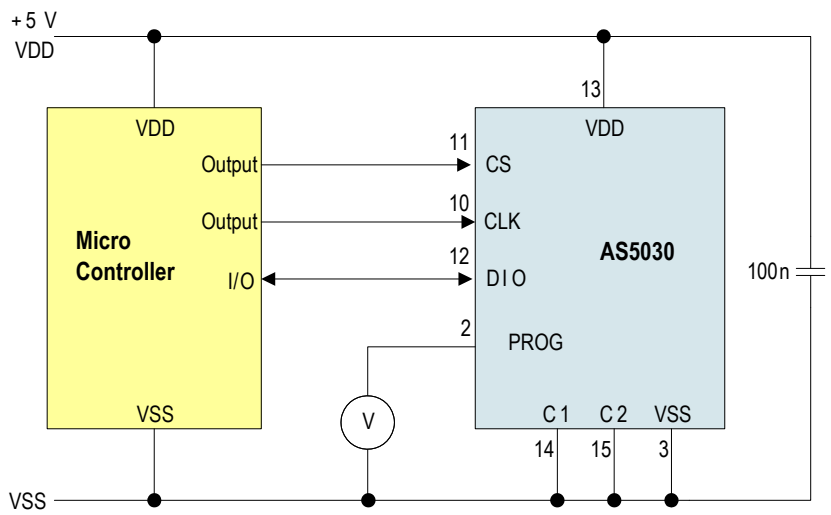
By digital verification:

This is simply done by sending a READ OTP command (#0F$_H$). The structure of this register is the same as for the OTP PROG or OTP WRITE commands.

By analog verification:

By sending an ANALOG OTP READ command (#09$_H$), pin PROG becomes an output, sending an analog voltage with each clock, representing a sequence of the bits in the OTP register. A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2.2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates improper programming.

Figure 49:
Analog OTP Verification



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AS5030 Status Indicators

Refer to Figure 43.

C2 Status Bit

This bit represents the hardware connection of the C2 configuration pin (#15) to determine, which hardware configuration is selected for the AS5030 in question.
C2 = low: pin C2 is 'low', indicating that the AS5030 is in 3-wire mode or a member of a 2-wire daisy chain connection (except the last).

C2 = high: pin C2 is 'high', indicating that the AS5030 is in 2-wire mode and/or the last member of a 2-wire daisy chain connection.

Lock Status Bit

The Lock signal indicates the ADC lock status. If Lock = low (ADC unlocked), the angle information is invalid. To determine a valid angular signal at best performance, the following indicators should be set:

Lock = 1

AGC > 00_H and < $2F_H$

Note(s): The angle signal may also be valid (Lock = 1), when the AGC is out of range (00_H or $2F_H$), but the accuracy of the AS5030 may be reduced due to the out of range condition of the magnetic field strength.

Magnetic Field Strength Indicators

The AS5030 is not only able to sense the angle of a rotating magnet, it can also measure the magnetic field strength (and hence the vertical distance) of the magnet.

This extra feature can be used for several purposes:

- As a safety feature by constantly monitoring the presence and proper vertical distance of the magnet
- As a state-of-health indicator, e.g. for a power-up self test
- As a push-button feature for rotate-and-push types of manual input devices
- The magnetic field strength information is available in two forms:

Magnetic Field Strength Hardware Indicator:

Pin MagRngn (#1) will be 'high', when the magnetic field is too weak. The switching limit is determined by the value of the AGC. If the AGC value is <$3F_H$, the MagRngn output will be 'low' (green range), If the AGC is at its upper limit ($3F_H$), the MagRngn output will be 'high' (red range).

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Magnetic Field Strength Software Indicator:

D13:D7 in the serial data that is obtained by command READ ANGLE contains the 6-bit AGC information. The AGC is an automatic gain control that adjusts the internal signal amplitude obtained from the Hall elements to a constant level. If the magnetic field is weak, e.g. with a large vertical gap between magnet and IC, with a weak magnet or at elevated temperatures of the magnet, the AGC value will be 'high'. Likewise, the AGC value will be lower when the magnet is closer to the IC, when strong magnets are used and at low temperatures.
The best performance of the AS5030 will be achieved when operating within the AGC range. It will still be operational outside the AGC range, but with reduced performance especially with a weak magnetic field due to increased noise.

Factors Influencing the AGC Value:

In practical use, the AGC value will depend on several factors:

- The initial strength of the magnet. Aging magnets may show a reducing magnetic field over time which results in an increase of the AGC value. The effect of this phenomenon is relatively small and can easily be compensated by the AGC.
- The vertical distance of the magnet. Depending on the mechanical setup and assembly tolerances, there will always be some variation of the vertical distance between magnet and IC over the lifetime of the application using the AS5030. Again, vertical distance variations can be compensated by the AGC.
- The temperature and material of the magnet. The recommended magnet for the AS5030 is a diametrically magnetized, 5-6mm diameter NdFeB (Neodymium-Iron-Boron) magnet. Other magnets may also be used as long as they can maintain to operate the AS5030 within the AGC range.
  Every magnet has a temperature dependence of the magnetic field strength. The temperature coefficient of a magnet depends on the used material. At elevated temperatures, the magnetic field strength of a magnet is reduced, resulting in an increase of the AGC value. At low temperatures, the magnetic field strength is increased, resulting in a decrease of the AGC value.
  The variation of magnetic field strength over temperature is automatically compensated by the AGC.

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OTP Sensitivity Adjustment

To obtain best performance and tolerance against temperature or vertical distance fluctuations, the AGC value at normal operating temperature should be in the middle between minimum and maximum, hence it should be around 100000 (20_H).

To facilitate the "vertical centering" of the magnet+IC assembly, the sensitivity of the AS5030 can be adjusted in the OTP register in 4 steps. A sensitivity adjustment is recommended, when the AGC value at normal operation is close to its lower limit (around 00_H). The default sensitivity setting is 00_H = low sensitivity.

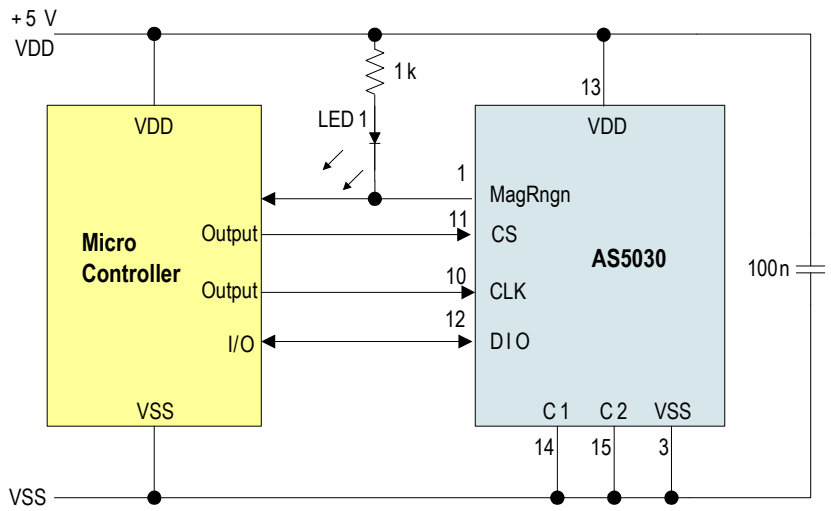
"Push-Button" Feature

Using the magnetic field strength software and hardware indicators described above, the AS5030 provides a useful method of detecting both rotation and vertical distance simultaneously. This is especially useful in applications implementing a rotate-and-push type of human interface (e.g. in panel knobs and switches).

The MagRngn output is 'high', when the magnetic field is below the low limit (weak or no magnet) and low when the magnetic field is above the low limit (in-range or strong magnet).

A finer detection of a vertical distance change, for example when only short vertical strokes are made by the push-button, is achieved by memorizing the AGC value in normal operation and triggering on a change from that nominal the AGC value to detect a vertical movement.

Figure 50:
Magnetic Field Strength Indicator



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High Speed Operation

The AS5030 is using a fast tracking ADC (TADC) to determine the angle of the magnet. The TADC has a tracking rate of 1.15µs (typ).

Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register. In worst case, usually at start-up, the TADC requires a maximum of 127 steps (127 * 1.15µs = 146.05µs) to lock. Once it is locked, it requires only one cycle (1.15µs) to track the moving magnet.
The AS5030 can operate in locked mode at rotational speeds up to 30000 rpm.

In Low Power Mode or Ultra-Low Power Mode, the position of the TADC is frozen. It will continue from the frozen position once it is powered up again. If the magnet has moved during the power down phase, several cycles will be required before the TADC is locked again. The tracking time to lock in with the new magnet angle can be roughly calculated as:

(EQ3) $$t_{LOCK} = 1.15\mu s * |NewPos - OldPos|$$

t_{LOCK} = time required to acquire the new angle after power up from one of the reduced power modes [µs]

OldPos = Angle position when one of the reduced power modes is activated [°]

NewPos = Angle position after resuming from reduced power mode [°]

Propagation Delay

The Propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds it is an important parameter at high speeds.

The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed.

The main factors contributing to the propagation delay are:

ADC Sampling Rate

For high speed applications, fast ADCs are essential. The ADC sampling rate directly influences the propagation delay. The fast tracking ADC used in the AS5030 with a tracking rate of only 1.15µs (typ.) is a perfect fit for both high speed and high performance.

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Chip Internal Low-Pass Filtering

A commonplace practice for systems using analog-to-digital converters is to filter the input signal by an anti-aliasing filter. The filter characteristic must be chosen carefully to balance propagation delay and noise.

The low-pass filter in the AS5030 has a cut-off frequency of typ. 23.8kHz and the overall propagation delay in the analog signal path is typ. 15.6µs.

Digital Readout Rate

Aside from the chip-internal propagation delay, the time required to read and process the angle data must also be considered. Due to its nature, a PWM signal is not very usable at high speeds, as you get only one reading per PWM period. Increasing the PWM frequency may improve the situation but causes problems for the receiving controller to resolve the PWM steps. The frequency on the AS5030 PWM output is typ. 1.95kHz with a resolution of 2µs/step.

A more suitable approach for high speed absolute angle measurement is using the serial interface. With a clock rate of up to 6MHz, a complete set of data (21bits) can be read in >3.5µs

Total Propagation Delay of the AS5030

The total propagation delay of the AS5030 is the delay in the analog signal path and the tracking rate of the ADC:

15.6µs + 1.15µs = 16.75µs

If only the SIN-/COS-outputs are used, the propagation delay is the analog signal path delay only (typ. 15.6µs).

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Position Error Over Speed

The angle error over speed caused by the propagation delay is calculated as:

(EQ4) $\Delta\varphi_{pd} = rpm * 6 * 16.75E^{-6}$

in degrees

In addition, the anti-aliasing filter causes an angle error calculated as:

(EQ5) $\Delta\varphi_{lpf} = ArcTan [rpm / (60*f_0)]$

Examples of the overall position error caused by speed, including both propagation delay and filter delay:

Figure 51:

Speed (rpm)	Total Position Error ($\Delta\varphi_{pd} + \Delta\varphi l_{pf}$)
100	0.0175°
1000	0.175°
10000	1.75°

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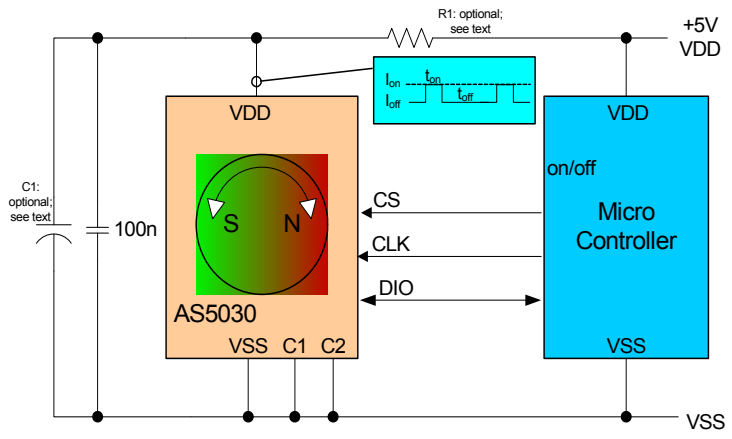
Reduced Power Modes

The AS5030 can be operated in 3 reduced power modes. All 3 modes have in common that they switch off or freeze parts of the chip during intervals between measurements. In Low Power Mode or Ultra-low Power Mode, the AS5030 is not operational, but due to the fast start-up, an angle measurement can be accomplished very quickly and the chip can be switched to reduced power immediately after a valid measurement has been taken. Depending on the intervals between measurements, very low average power consumption can be achieved using such a strobed measurement mode.

- Low Power Mode: Reduced current consumption, very fast start-up. Ideal for short sampling intervals (<3ms)
- Ultra-Low Power Mode: Further reduced current consumption, but slower start-up than Low Power Mode. Ideal for sampling intervals from 3….200ms.
- Power Cycle mode: zero power consumption (externally switched off) during sampling intervals, but slower start-up than Ultra-Low Power Mode. Ideal for sampling intervals 200ms.

Low Power Mode and Ultra-Low Power Mode

Figure 52:
Low Power Mode and Ultra-Low Power Mode Connection



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The AS5030 can be put in Low Power Mode or Ultra-Low Power Mode by simple serial commands, using the regular connection for 2-wire or 3-wire serial data transmission (see Figure 20 and Figure 26).

The required serial command is SET PWR MODE (11_H):

Figure 53:
Power Mode Configuration

ULP / LPn	PSM	Mode
0	0	Normal Operation
0	1	Low Power Mode
1	0	Normal Operation
1	1	Ultra-Low Power Mode

Note(s):

1. After returning from Low Power mode or Ultra-Low Power mode to normal operation (PSM = 0), if the Hysteresis is enabled (Hys=0), a general reset must be performed: set bit RST and then clear bit RST using command 15_H.

The two following cases describe the typical loop programmed in the software:

Hys = 0 (1 LSB hysteresis)

1. Wait for CPU interrupt or delay for next angle read (typ. <3ms in LP mode, typ>3ms in ULP mode)
2. Wake up (PSM = 0)
3. Set Reset (rst = 1)
4. Clear Reset (rst = 0)
5. Wait 1.5ms (Low Power Mode)
6. Check if Lock = 1 then read angle
7. Enable Low Power Mode or Ultra-Low Power Mode (PSM=1)
8. Return to 1

Hys = 1 (No hysteresis)

1. Wait for CPU interrupt or delay for next angle read (typ. <3ms in LP mode, typ>3ms in ULP mode)
2. Wake up (PSM = 0)
3. Wait 0.01ms (Low Power Mode)
4. Check if Lock = 1 then read angle
5. Enable Low Power Mode or Ultra-Low Power Mode (PSM=1)
6. Return to 1

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The difference between Low Power Mode and Ultra-Low Power Mode is the current consumption and the wake-up time to switch back to active operation.

Figure 54:
Current Consumption of Power Modes

Mode	Current Consumption (typ.)	Wake-Up Time to Active Operation
Active Operation	14 mA	1.0 ms (without AGC) 3.8 ms (with locked AGC)
Low Power Mode	1.4 mA	0.15 ms
Ultra-Low Power Mode	30 µA	0.5 ms

In both Reduced Power Modes, the AS5030 is inactive. The last state, e.g. the angle, AGC value, etc. is frozen and the chip starts from this frozen state when it resumes active operation. This method provides much faster start-up than a "cold start" from zero. If the AS5030 is cycled between active and reduced current mode, a substantial reduction of the average supply current can be achieved. The minimum dwelling time in active mode is the wake-up time. The actual active time depends on how much the magnet has moved while the AS5030 was in reduced power mode. The angle data is valid, when the status bit LOCK has been set. Once a valid angle has been measured, the AS5030 can be put back to reduced power mode. The average power consumption can be calculated as:

(EQ6)
$$I_{avg} = \frac{I_{active} \times t_{on} + I_{power-down} \times t_{off}}{t_{on} + t_{off}}$$

Sampling interval = $t_{on} + t_{off}$

I_{avg}: average current consumption

I_{active}: current consumption in active mode

I_{power_down}: current consumption in reduced power mode

t_{on}: time period during which the chip is operated in active mode

t_{off}: time period during which the chip is in reduced power mode

Example: Ultra-Low Power Mode; sampling period = one measurement every 10ms.
System constants = I_{active} = 14mA,
I_{power_down} = 30µA, t_{on}(min) = 500µs
(startup from Ultra-Low Power Mode)

(EQ7)
$$I_{avg} = \frac{14mA \times 500\mu s + 30\mu A \times 9.5ms}{500\mu s + 9.5ms} = 729\mu A$$

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See Figure 56 for an overview table of the average current consumption in the various reduced power modes.

Reducing Power Supply Peak Currents

An optional RC-filter (R1/C1) may be added to avoid peak currents in the power supply line when the AS5030 is toggled between active and reduced power mode. R1 must be chosen such that it can maintain a VDD voltage of 4.5V ~ 5.5V under all conditions, especially during long active periods when the charge on C1 has expired. C1 should be chosen such that it can support peak currents during the active operation period. For long active periods, C1 should be large and R1 should be small.

Power Cycling Mode

The power cycling method shown in Figure 55 cycles the AS5030 by switching it on and off, using an external PNP transistor high side switch.

This mode provides the least power consumption of all three modes; when the sampling interval is more than 400ms, as the current consumption in off-mode is zero.

It also has the longest start-up time of all modes, as the chip must always perform a "cold start" from zero, which takes about 1.9 ms.

The optional filter R1/C1 may again be added to reduce peak currents in the 5V power supply line.

Figure 55:
Application Example III: Ultra-low Power Encoder

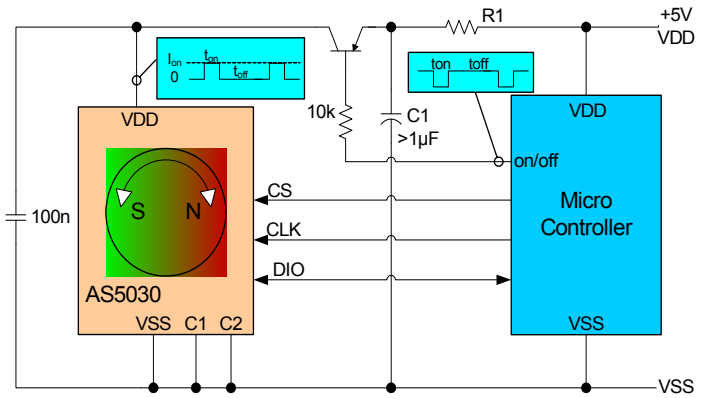

Figure 55 shows an overview of the average supply currents in the three reduced power modes, depending on the sampling interval. The graphs shows that the Low Power Mode is the best option for sampling intervals <4ms, while the Ultra-Low Power Mode is the best option for sampling intervals between 4~400ms.

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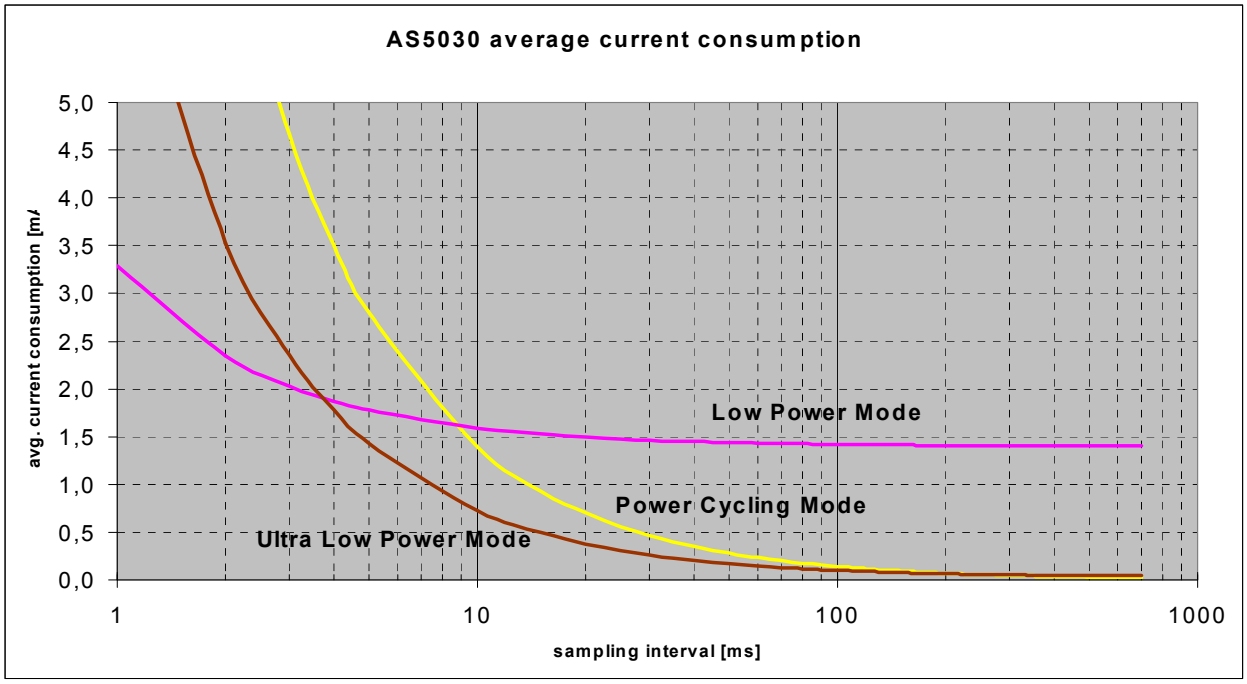
At sampling intervals > 400ms, the power cycling mode is the best method to minimize the average current consumption. The curves are based on the figures given in Low Power Mode and Ultra-Low Power Mode.

Figure 56:
Average Current Consumption of Reduced Power Modes



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Accuracy of the Encoder System

This chapter describes which individual factors influence the accuracy of the encoder system and how to improve them.

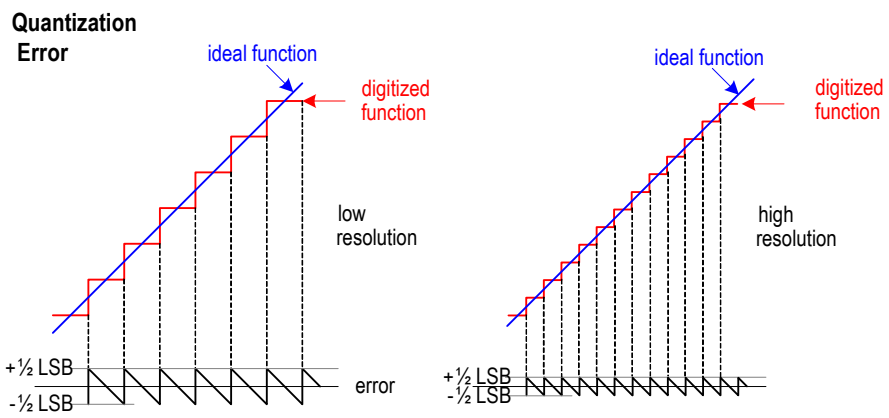
Accuracy is defined as the difference between measured angle and actual angle. This is not to be confused with resolution, which is the smallest step that the system can resolve.

The two parameters are not necessarily linked together. A high resolution encoder may not necessarily be highly accurate as well.

Quantization Error

There is however a direct link between resolution and accuracy, which is the quantization error:

Figure 57:
Quantization Error of a Low Resolution and a High Resolution System



The resolution of the encoder determines the smallest step size. The angle error caused by quantization cannot get better than ± ½ LSB. As shown in Figure 57, a higher resolution system (right picture) has a smaller quantization error, as the step size is smaller.

For the AS5030, the quantization error is ± ½ LSB = ± 0.7°

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Figure 58:
Typical INL Error Over 360°

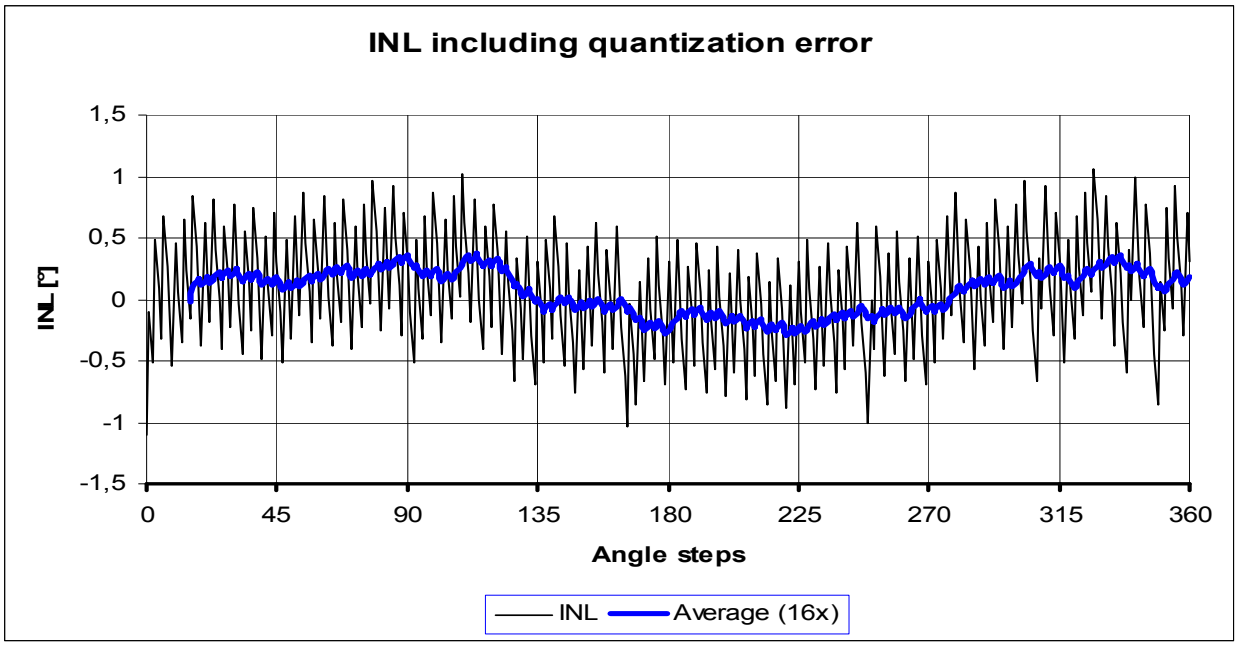

Figure 58 shows a typical example of an error curve over a full turn of 360° at a given X-Y displacement. The curve includes the quantization error, transition noise and the system error. The total error is ~2.2° peak/peak (± 1.1°).

The sawtooth-like quantization error (see also Figure 57) can be reduced by averaging, provided that the magnet is in constant motion and there are an adequate number of samples available. The solid bold line in Figure 58 shows the moving average of 16 samples. The INL (intrinsic non-linearity) is reduced to from ~± 1.1° down to ~± 0.3°. The averaging however, also increases the total propagation delay, therefore it may be considered for low speeds only or adaptive; depending on speed (see Position Error Over Speed on page 42).

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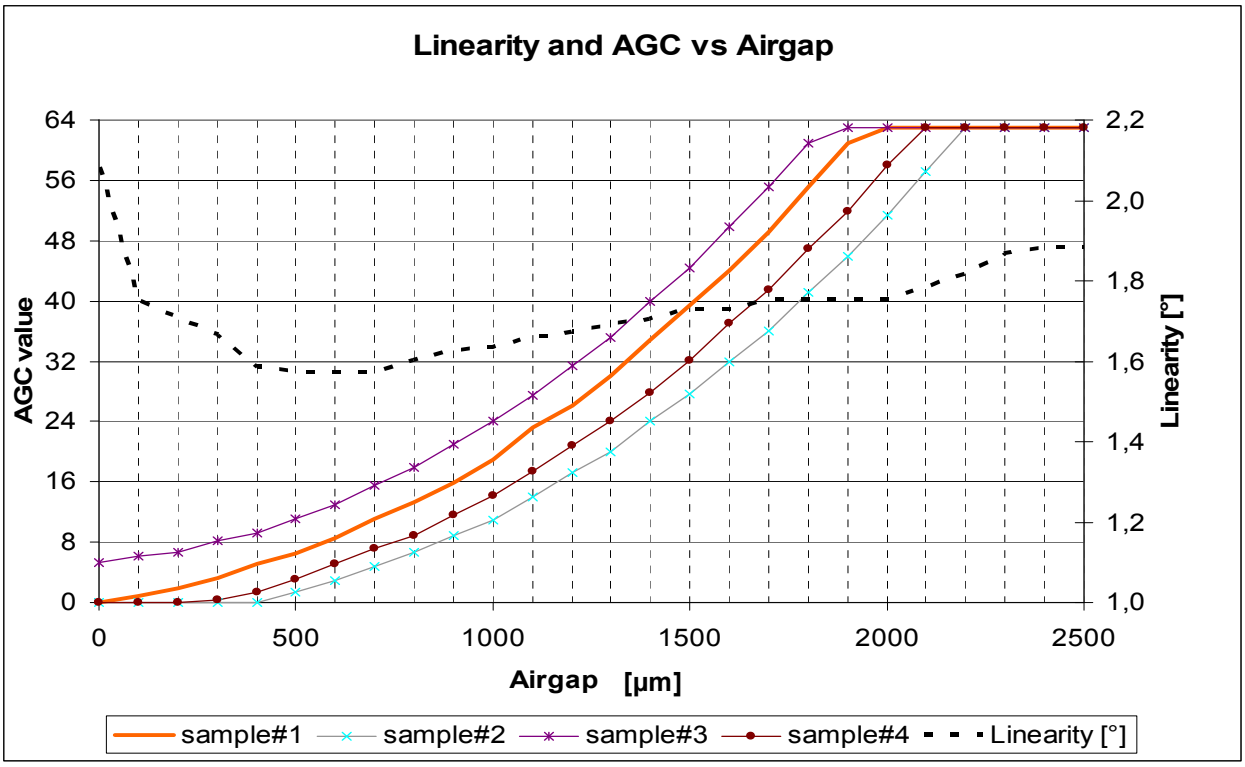
Vertical Distance of the Magnet

The chip-internal automatic gain control (AGC) regulates the input signal amplitude for the tracking-ADC to a constant value. This improves the accuracy of the encoder and enhances the tolerance for the vertical distance of the magnet.

Figure 59:
Typical Curves for Vertical Distance Versus ACG Value on Several Untrimmed Samples



As shown in Figure 59, the AGC value (left Y-axis) increases with vertical distance of the magnet.

Consequently, it is a good indicator for determining the vertical position of the magnet, for example as a push-button feature, as an indicator for a defective magnet or as a preventive warning (e.g. for wear on a ball bearing etc.) when the nominal AGC value drifts away.
If the magnet is too close or the magnetic field is too strong, the AGC will be reading 0.

If the magnet is too far away (or missing) or if the magnetic field is too weak, the AGC will be reading 63 ($3F_H$).

The AS5030 will still operate outside the AGC range, but the accuracy may be reduced as the signal amplitude can no longer be kept at a constant level.

The linearity curve in Figure 59 (right Y-axis) shows that the accuracy of theAS5030 is best within the AGC range, even slightly better at small airgaps (0.4mm ~ 0.8mm).

At very short distances (0mm ~ 0.1mm) the accuracy is reduced, mainly due to nonlinearities in the magnetic field.

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At larger distances, outside the AGC range (~2.0mm ~ 2.5mm and more) the accuracy is still very good, only slightly decreased from the nominal accuracy.

Since the field strength of a magnet changes with temperature, the AGC will also change when the temperature of the magnet changes. At low temperatures, the magnetic field will be stronger and the AGC value will decrease. At elevated temperatures, the magnetic field will be weaker and the AGC value will increase.

Sensitivity Trimming

As the curves for the 4 samples in Figure 59 show, the AGC value will not show exactly the same value at a given airgap on each part. For example, at 1mm vertical distance, the AGC may read a value between ~11 ~ 24. This is because for normal operation an exact trimming is not required since the AGC is part of a closed loop system.
However, the AS5030 offers an optional user trimming in the OTP to allow an even tighter AGC tolerance for applications where the information about magnetic field strength is also utilized, e.g. for rotate-and-push types of knobs, etc.

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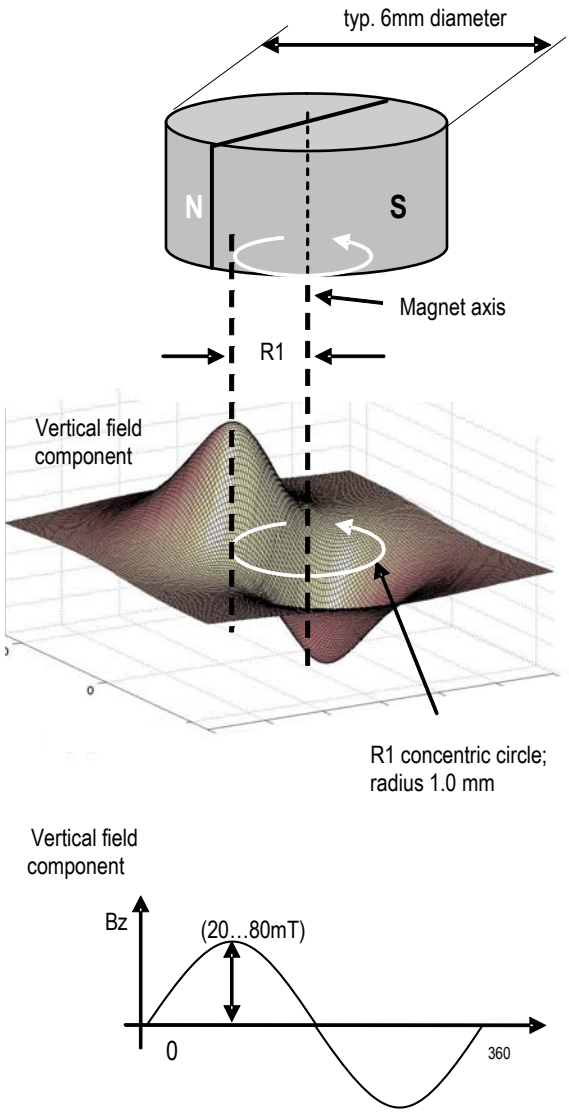
Choosing the Proper Magnet

Figure 60:
Vertical Magnetic Fields of a Rotating Magnet



Note(s):

1. There is no strict requirement on the type or shape of the magnet to be used with the AS5030. It can be cylindrical as well as square in shape. The key parameter is that the vertical magnetic field B_z, measured at a radius of 1mm from the rotation axis is sinusoidal with a peak amplitude of 20 ~ 80mT.

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Magnet Placement

Ideally, the center of the magnet, the diagonal center of the IC and the rotation axis of the magnet should be in one vertical line.

The lateral displacement of the magnet should be within ± 0.25mm from the IC package center or ± 0.5mm from the IC center, including the placement of the chip within the IC package.

The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits. The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 2.5mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits. A magnetic field outside the specified range may still produce acceptable results, but with reduced accuracy. The out-of-range condition will be indicated, when the AGC is at the limits (AGC= 0: field too strong;

AGC=63=(3F_H): field too weak or missing magnet.

Figure 61:
Bz Field Distribution Along the X-Axis of a 6mmØ Diametric Magnetized Magnet

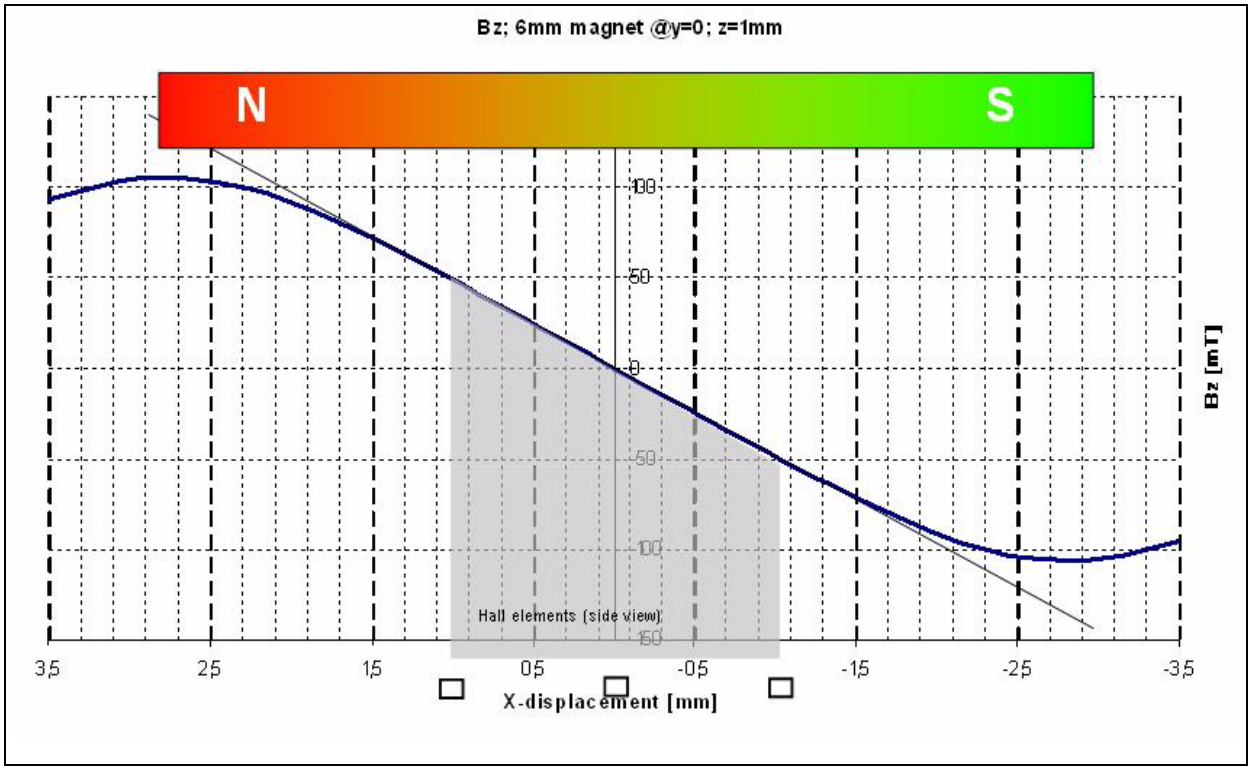

Figure 61 shows a cross sectional view of the vertical magnetic field component Bz between the north and south pole of a 6mm diameter magnet, measured at a vertical distance of 1mm. The poles of the magnet (maximum level) are about 2.8mm from the magnet center, which is almost at the outer magnet edges. The magnetic field reaches a peak amplitude of ~± 106mT at the poles.

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The Hall elements are located at a radius of 1mm (indicated as squares at the bottom of the graph). Due to the side view, the two Hall elements at the Y-axis are overlapping at X = 0mm, therefore only 3 Hall elements are shown.

At 1mm radius, the peak amplitude is ~± 46mT, respectively a differential amplitude of 92mT.

The vertical magnetic field B_z follows a fairly linear pattern up to about 1.5mm radius. Consequently, even if the magnet is not perfectly centered, the differential amplitude will be the same as for a centered magnet.

For example, if the magnet is misaligned in X-axis by -0.5mm, the two X-Hall sensors will measure 70mT (@x = -1.5mm) and -22mt (@x = -0.5mm). Again, the differential amplitude is 92mT.

At larger displacements however, the B_z amplitude becomes nonlinear, which results in larger errors that mainly affect the accuracy of the system (see also Figure 63)

Figure 62:
Vertical Magnetic Field Distribution of a Cylindrical 6mm Ø Diametric Magnetized Magnet at 1mm Gap

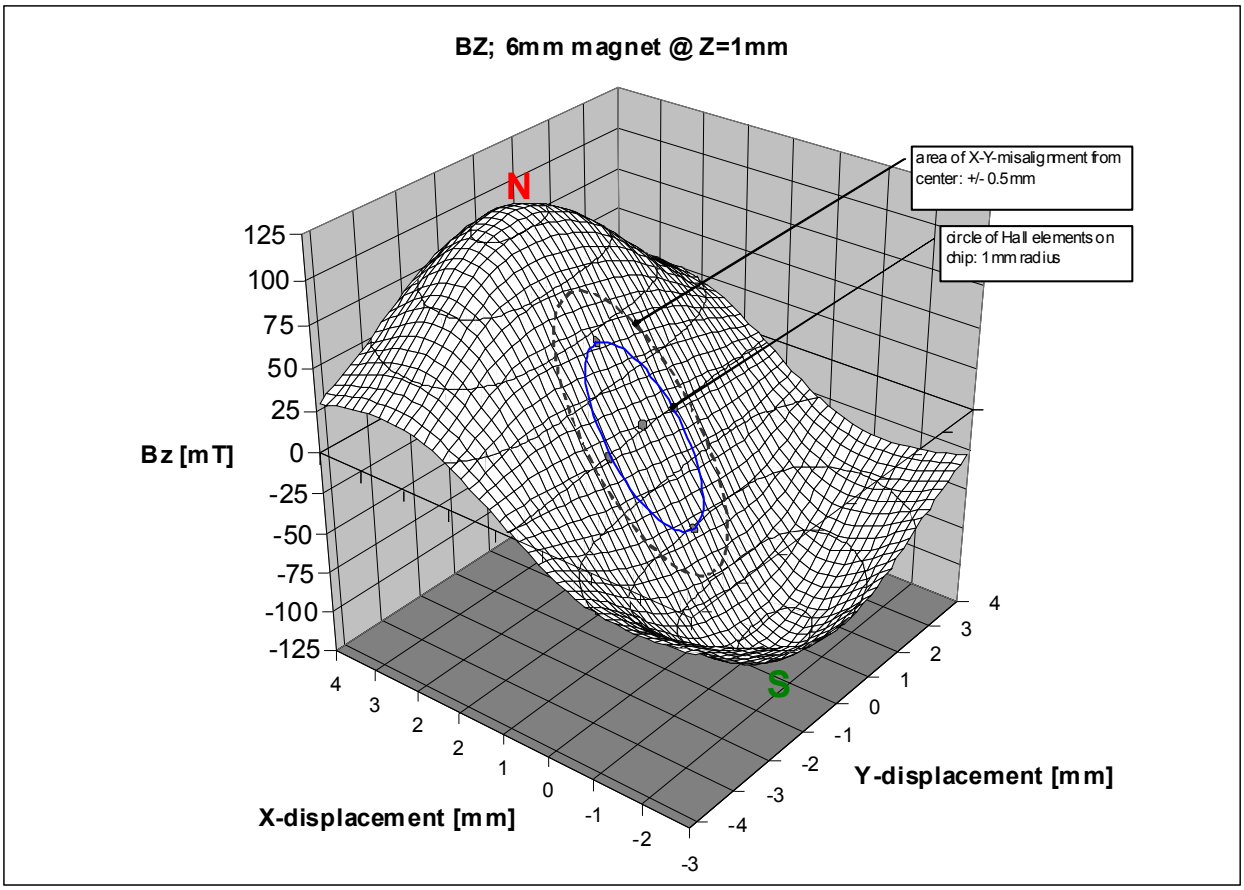

Figure 62 shows the same vertical field component as Figure 61, but in a 3-dimensional view over an area of ± 4mm from the rotational axis.

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Lateral Displacement of the Magnet

As shown in the magnet specifications Figure 9, the recommended horizontal position of the magnet axis with respect to the IC package center is within a circle of 0.25mm radius. This includes the placement tolerance of the IC within the package.

Figure 63 shows a typical error curve at a medium vertical distance of the magnet around 1.2mm (AGC = 24).

The X- and Y- axis of the graph indicate the lateral displacement of the magnet center with respect to the IC center.

At X = Y = 0, the magnet is perfectly centered over the IC. The total displacement plotted on the graph is for ± 1mm in both directions.

The Z-axis displays the worst case INL error over a full turn at each given X-and Y- displacement. The error includes the quantization error of ± 0.7°. For example, the accuracy for a centered magnet is between 1.0 ~ 1.5° (spec = 2° over full temperature range). Within a radius of 0.5mm, the accuracy is better than 2.0° (spec = 3° over temperature).

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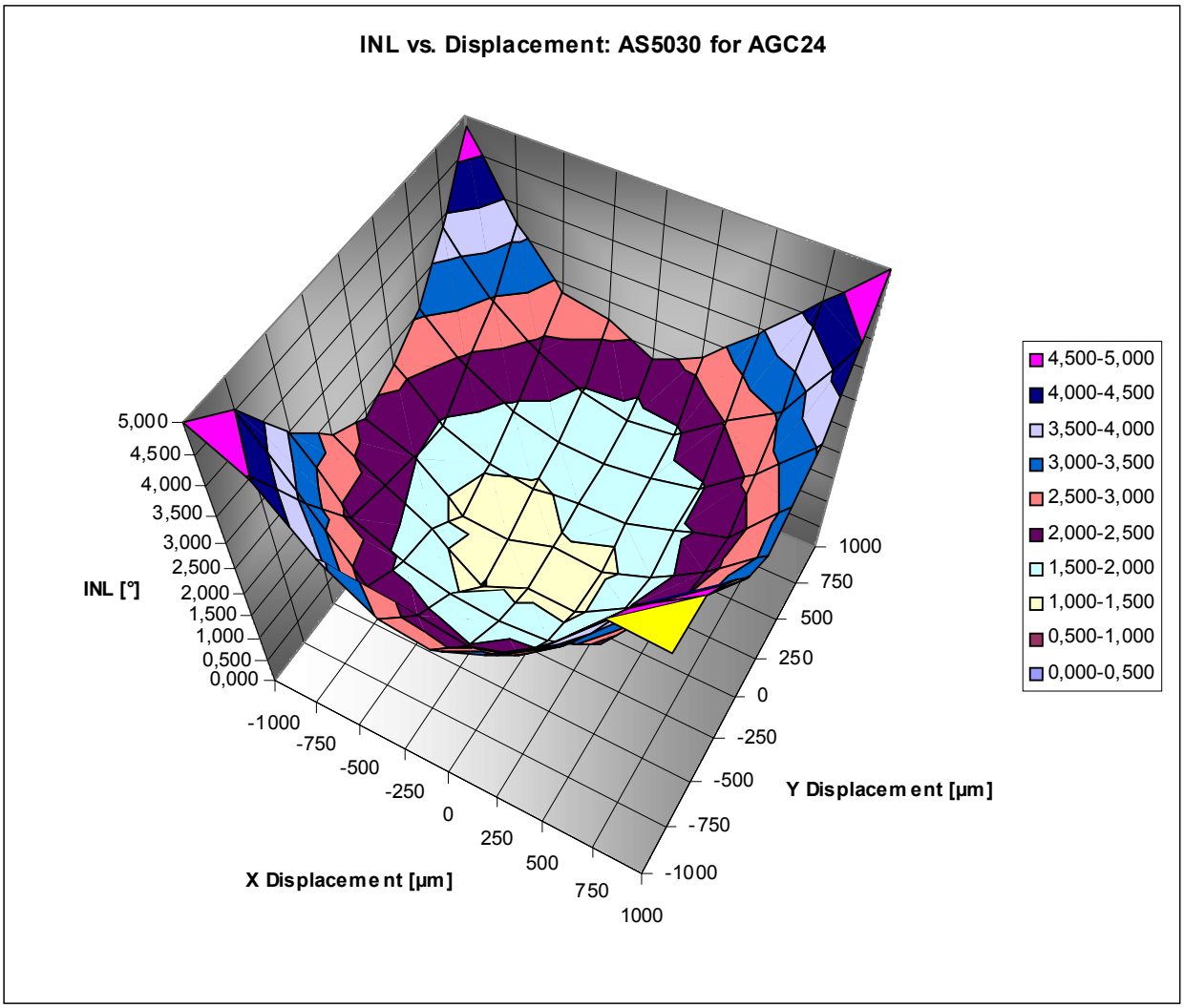
Figure 63:
Typical Error Curve of INL Error Over Lateral Displacement (including quantization error)



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Magnet Size

Figure 61 to Figure 63 in this chapter describe a cylindrical magnet with a diameter of 6mm. Smaller magnets may also be used, but since the poles are closer together, the linear range will also be smaller and consequently the tolerance for lateral misalignment will also be smaller.

If the ± 0.25mm lateral misalignment radius (rotation axis to IC package center) is too tight, a larger magnet can be used. Larger magnets have a larger linear range and allow more misalignment. However at the same time the slope of the magnet is more flat which results in a lower differential amplitude.

This requires either a stronger magnet or a smaller gap between IC and magnet in order to operate in the amplitude-controlled area (AGC > 0 and AGC < 63).
In any case, if a magnet other than the recommended 6mm diameter magnet is used, two parameters should be verified:

Verify that the magnetic field produces a sinusoidal wave, when the magnet is rotated. Note that this can be done with the SIN-/COS- outputs of the AS5030, e.g. rotate the magnet at constant speed and analyze the SIN- (or COS-) output with an FFT-analyzer.

It is recommended to disable the AGC for this test.

Verify that the B_z-Curve between the poles is as linear as possible. This curve may be available from the magnet supplier(s). Alternatively, the SIN- or COS- output of the AS5030 may also be used together with an X-Y- table to get a B_z-scan of the magnet. Furthermore, the sinewave tests described above may be re-run at defined X-and Y- misplacements of the magnet to determine the maximum acceptable lateral displacement range.

It is recommended to disable the AGC for both these tests.

Note(s): For preferred magnet suppliers, please refer to the **ams** website (Position Sensor section).

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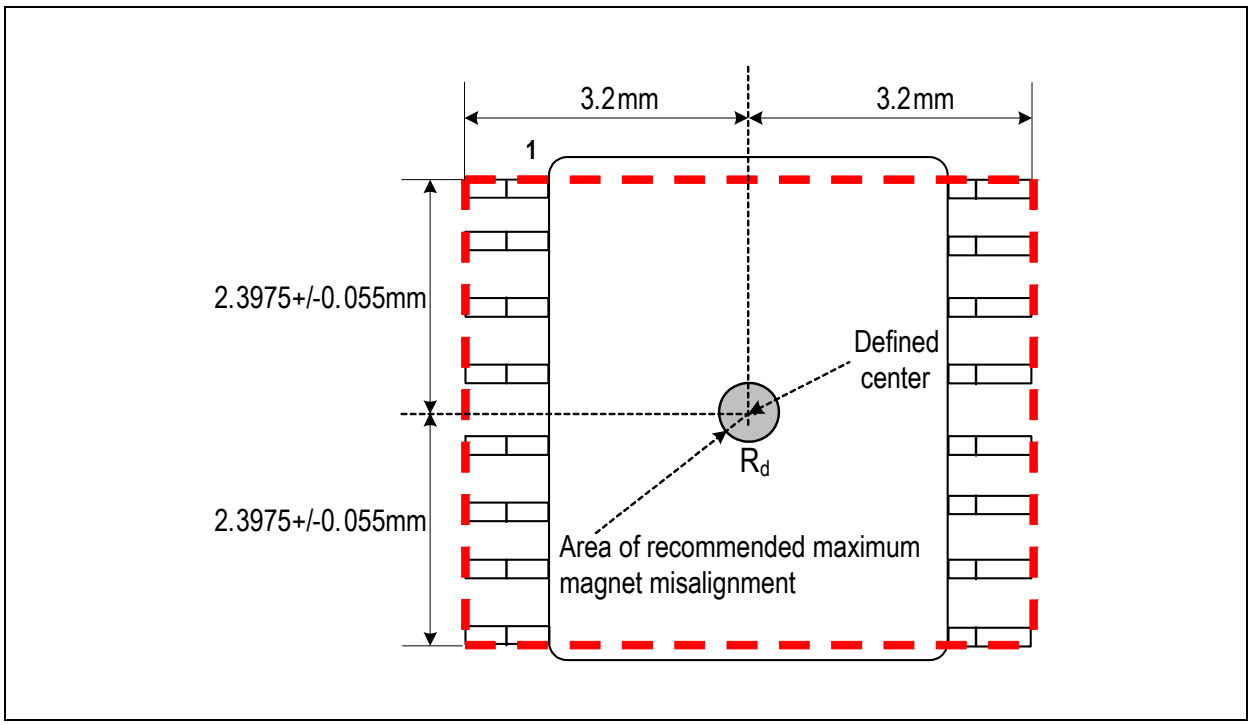
Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:

Figure 64:
Defined Chip Center and Magnet Displacement Radius



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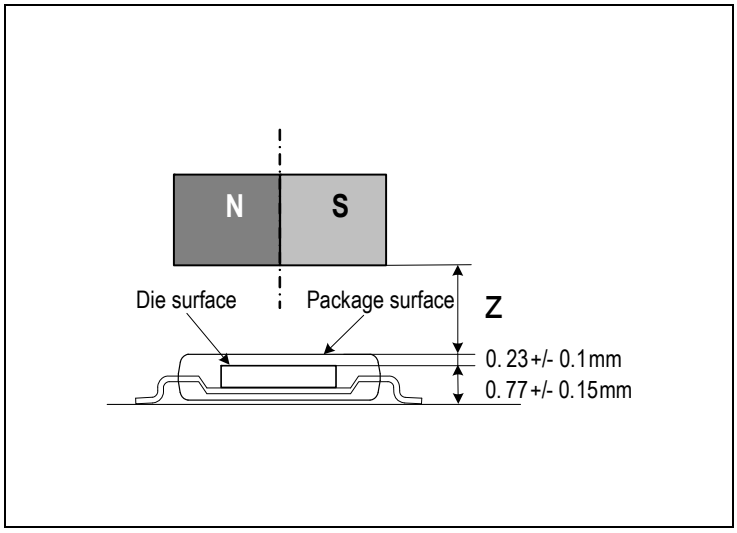
Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits. The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagRngn (pin 1).

Figure 65:
Vertical Placement of the Magnet



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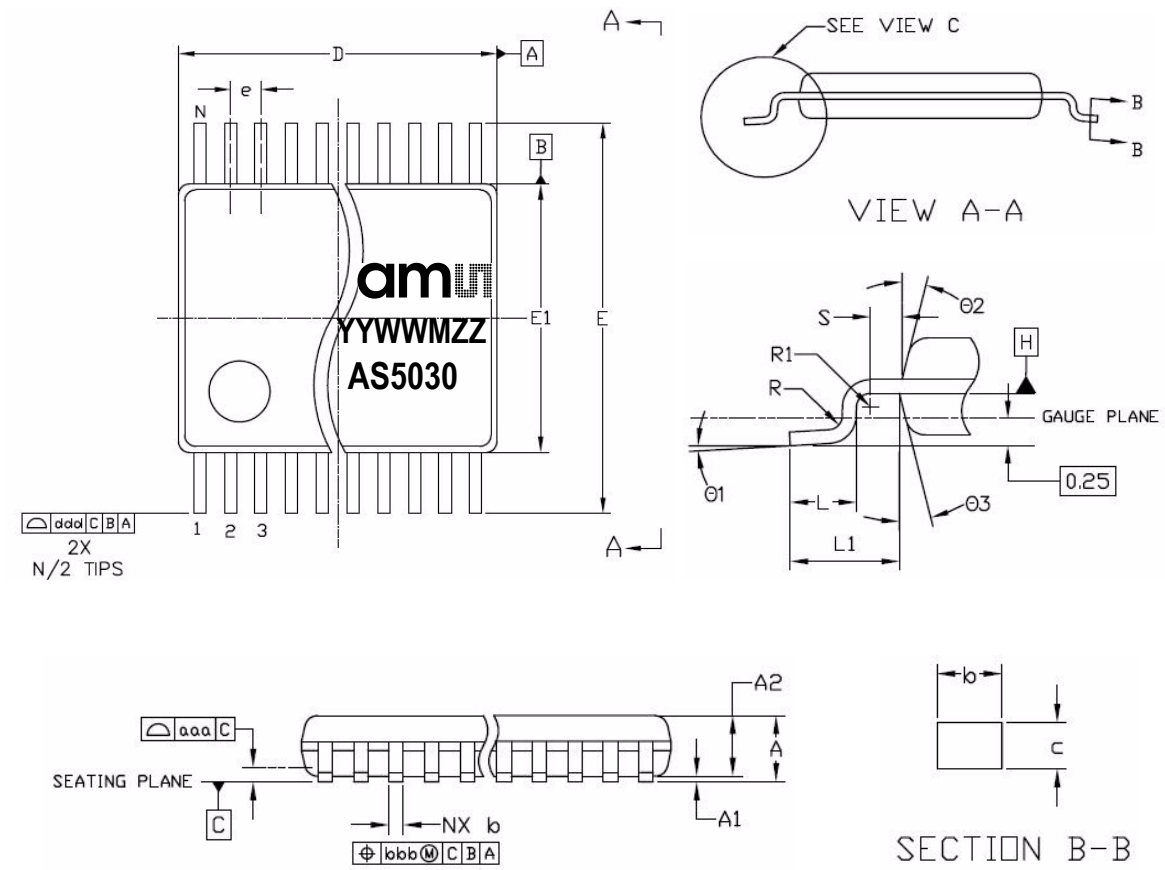
Package Drawings & Markings

The device is available in a 16-Pin TSSOP package.

Figure 66:
16-Pin TSSOP Package



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40 BSC	-
E1	4.30	4.40	4.50
e	-	0.65 BSC	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-

Symbol	Min	Nom	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Q1	0°		8°
Θ2	-	12 REF	-
Θ3	-	12 REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N	16		

Note(s):

1. Dimensioning & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.

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Figure 67:
Package Code: YYWWMZZ

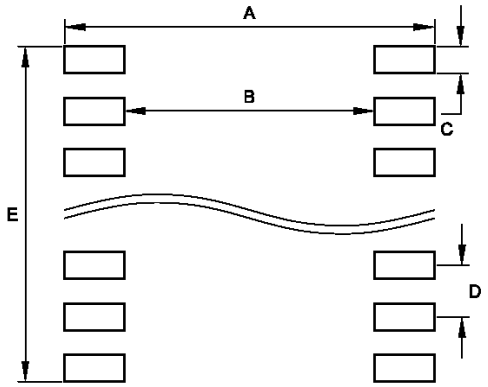
YY	WW	M	ZZ
Last two digits of the year	Manufacturing week	Assembly plant identifier	Assembly traceability code

JEDEC Package Outline Standard: MO - 153 AB

Thermal Resistance $R_{th(j-a)}$: 89 K/W in still air, soldered on PCB

Recommended PCB Footprint

Figure 68:
PCB Footprint



Recommended Footprint Data		
Symbol	mm	inch
A	7.26	0.286
B	4.93	0.194
C	0.36	0.014
D	0.65	0.0256
E	4.91	0.193

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Ordering & Contact Information

The devices are available as the standard products shown in Figure 69.

Figure 69:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5030-ATST	16-Pin TSSOP	AS5030	Tape & Reel	500 pcs/reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

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Revision Information

Changes from 2.4 to current revision 3-00 (2018-Mar-08)	Page
Content was updated to latest **ams** design	
Added benefits to Key Features	1
Updated Figure 69	62

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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