To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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2SK3161(L), 2SK3161(S)

Silicon N Channel MOS FET
High Speed Power Switching

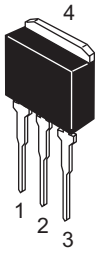
REJ03G1086-0300
(Previous: ADE-208-734A)
Rev.3.00
Sep 07, 2005

Features

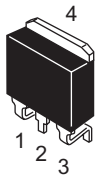
- Low on-resistance
  R_{DS} =90 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

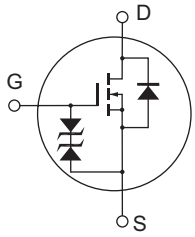
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK(L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK(S)-(1))





1. Gate
2. Drain
3. Source
4. Drain

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Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$ Note1	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP} Note3	15	A
Avalanche energy	E_{AR} Note3	15	mJ
Channel dissipation	Pch Note2	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

(Ta = 25°C)

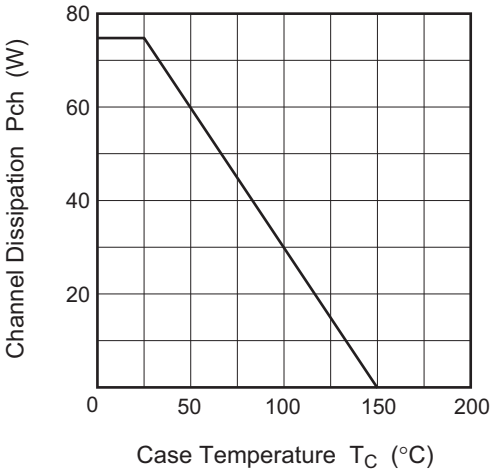
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	90	115	mΩ	I_D = 8 A, V_{GS} = 10V Note4
	$R_{DS(on)}$	—	95	125	mΩ	I_D = 8 A, V_{GS} = 4 V Note4
Forward transfer admittance	$\|y_{fs}\|$	16	20	—	S	I_D = 8 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	1600	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	510	—	pF	
Reverse transfer capacitance	Crss	—	250	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 8 A, V_{GS} = 10 V, R_L = 3.75 Ω
Rise time	t_r	—	120	—	ns	
Turn-off delay time	$t_{d(off)}$	—	400	—	ns	
Fall time	t_f	—	170	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A /µs

Note: 4. Pulse test

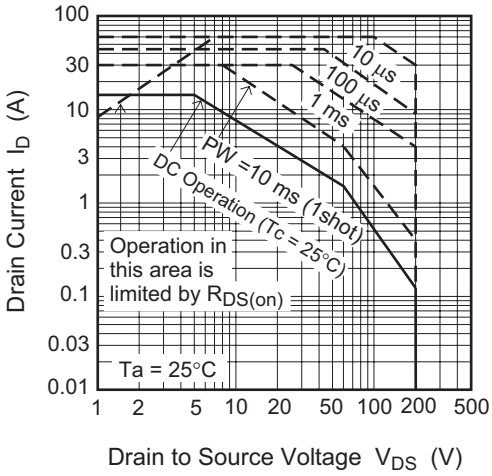
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Main Characteristics

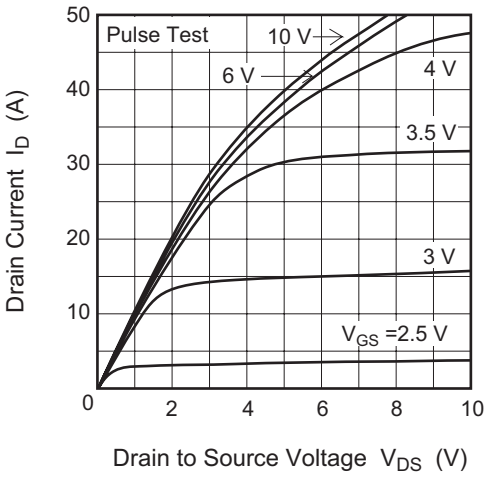
Power vs. Temperature Derating



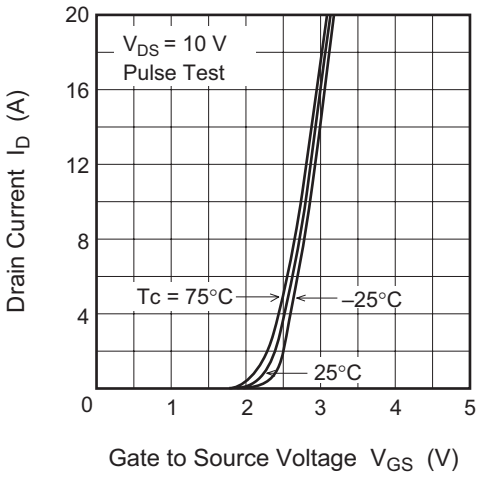
Maximum Safe Operation Area



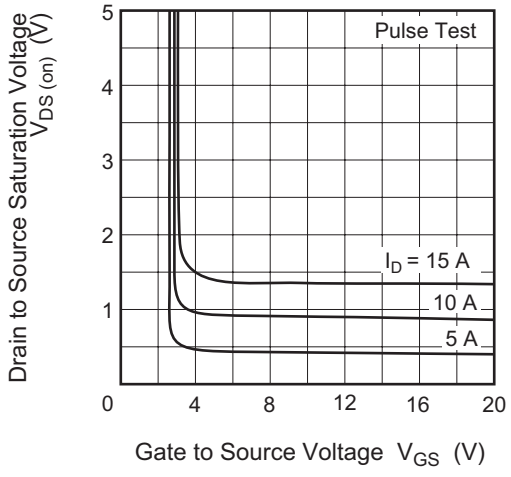
Typical Output Characteristics



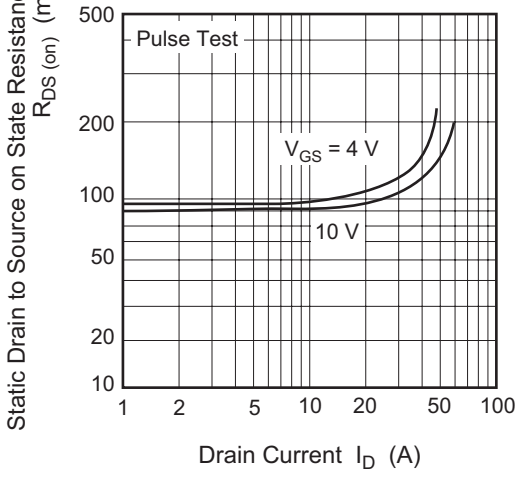
Typical Transfer Characteristics



Drain to Source Saturation Voltage vs. Gate to Source Voltage

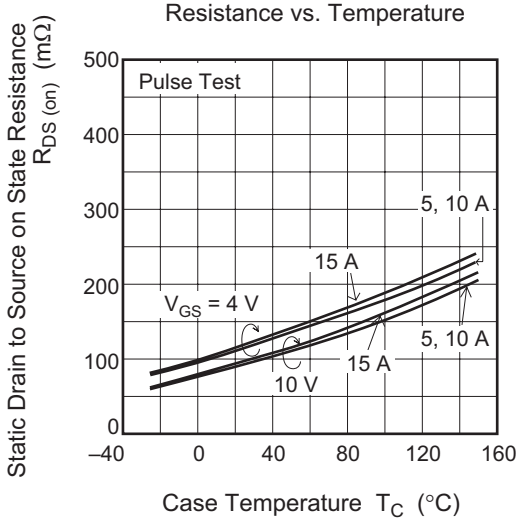


Static Drain to Source on State Resistance vs. Drain Current

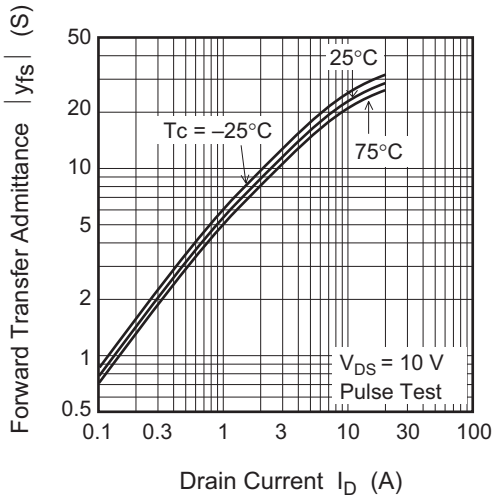


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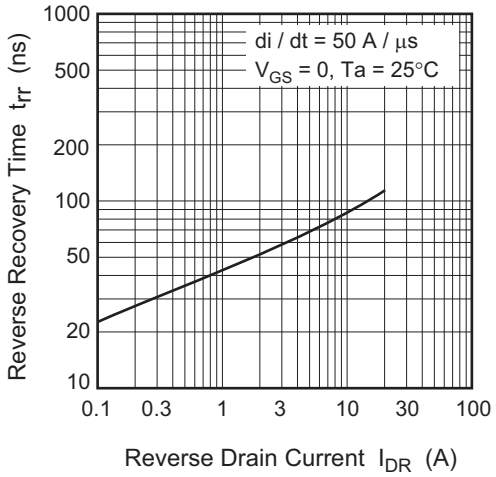
Static Drain to Source on State Resistance vs. Temperature



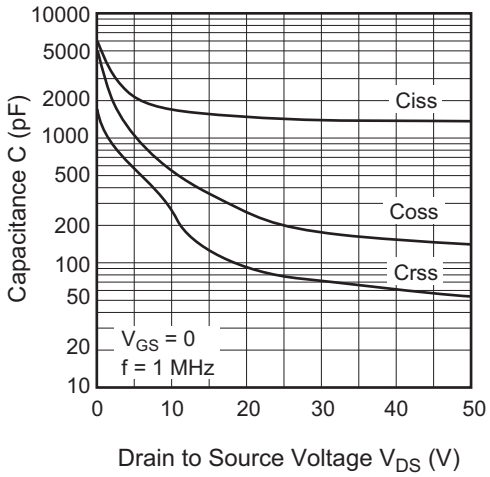
Forward Transfer Admittance vs. Drain Current



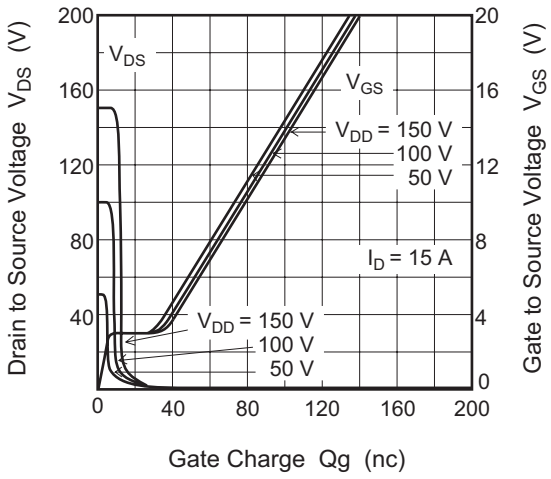
Body to Drain Diode Reverse Recovery Time



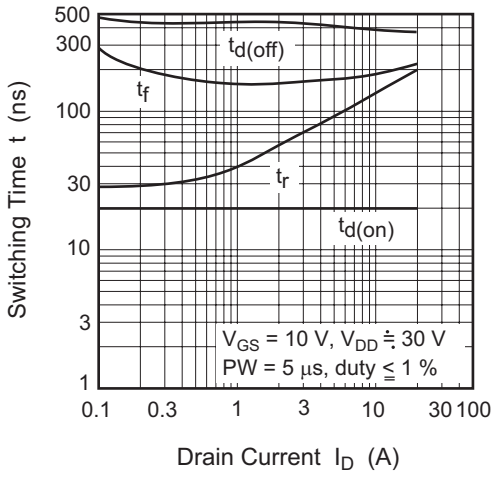
Typical Capacitance vs. Drain to Source Voltage



Dynamic Input Characteristics

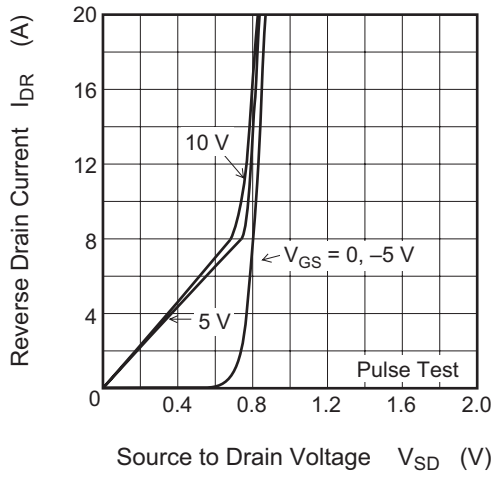


Switching Characteristics

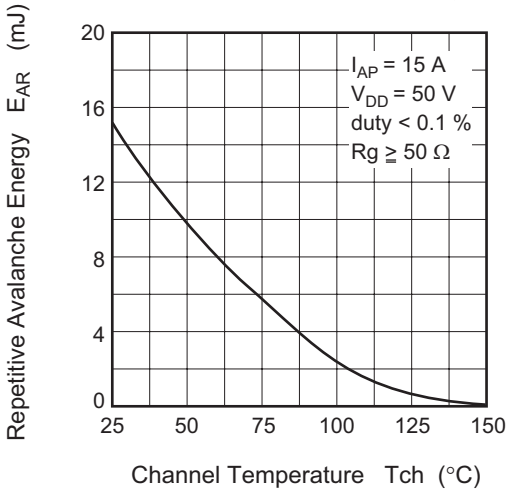


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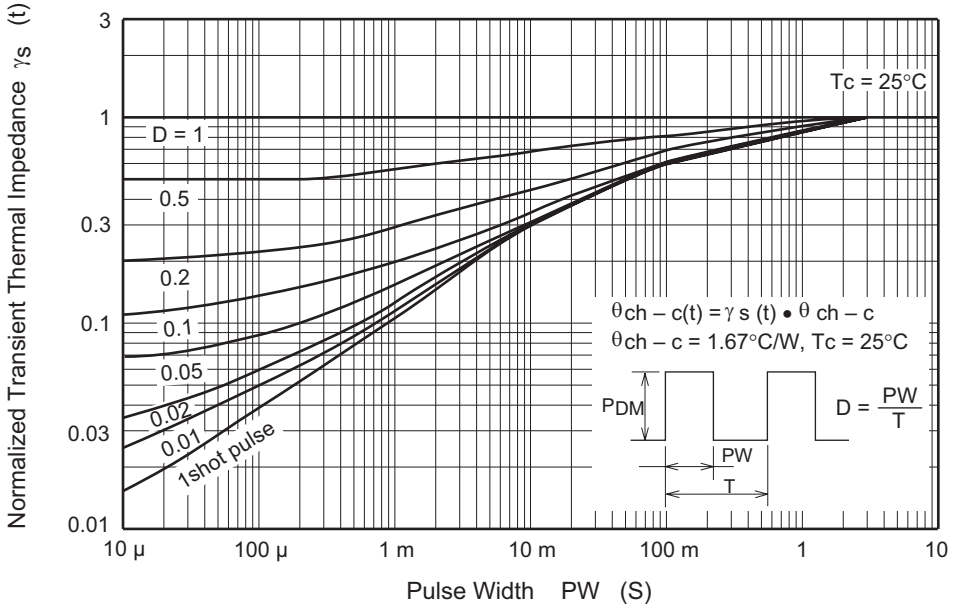
Reverse Drain Current vs. Source to Drain Voltage



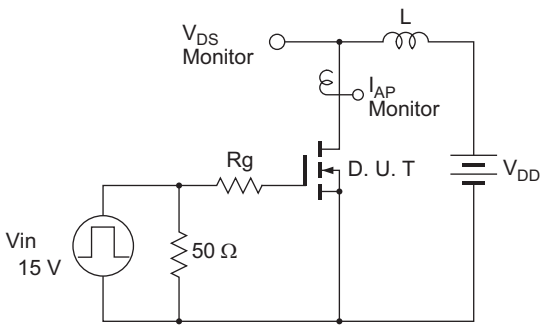
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

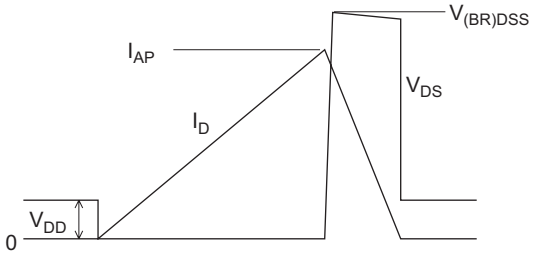


Avalanche Test Circuit



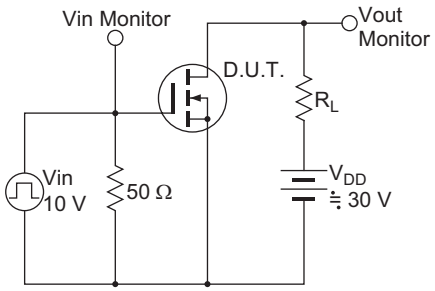
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

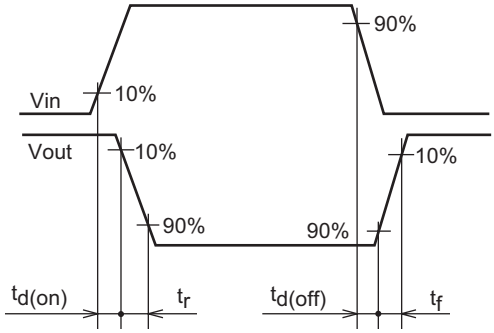


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Switching Time Test Circuit



Switching Time Waveforms

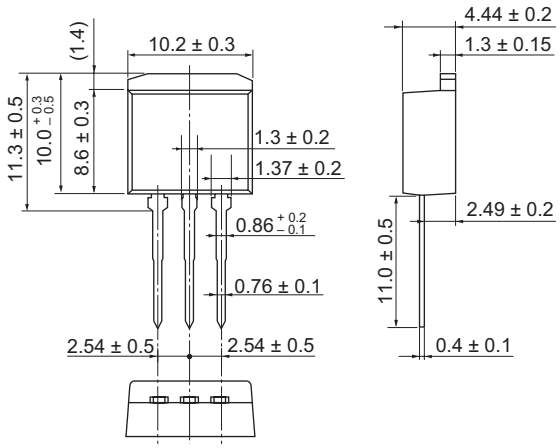


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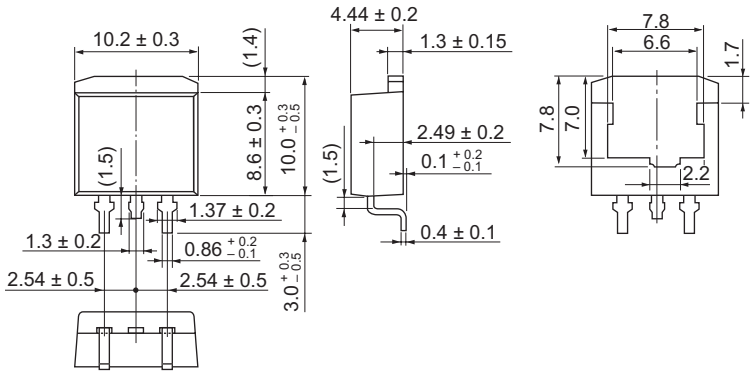
JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
—	PRSS0004AE-A	LDPAK(L) / LDPAK(L)V	1.40g

Unit: mm



JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g

Unit: mm



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2SK3161-E	500 pcs	Box (Sack)
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