CYW20737S

Bluetooth Low Energy System-in-Package (SiP) Module

The CYW20737S is a compact, highly integrated Bluetooth Low Energy (BLE) system-in-package (SiP) module. The CYW20737S SiP includes an embedded BLE antenna, 24 MHz clock, and 512 Kb EEPROM, so only a minimal set of external components is needed to create a standalone BLE device.

The CYW20737S is designed to accelerate time to market. The Bluetooth stack and several application profiles are built into the module, allowing customers to focus on their core applications. To further reduce application development time, the CYW20737S includes integrated software support, with one-click installation of the complete environment and a one-click compile/build/link/load cycle. All this, coupled with an ultrasmall form factor and support for a wide voltage range, makes the CYW20737S well suited for virtually any Bluetooth Smart application.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20737S	CYW20737S

Features

- ARM Cortex-M3 microcontroller unit (MCU)
- Embedded 512 Kb EEPROM
- Broadcom Serial Control (BSC), SPI, and UART interfaces
- FCC and CE compliant
- RoHS compliant, certified lead- and halogen-free
- Moisture Sensitivity Level (MSL) 3 compliant
- 6.5 mm × 6.5 mm × 1.2 mm Land Grid Array (LGA) 48-pin package

Applications

Profiles supported in ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- Blood glucose monitor
- Support for RSA security library
- Support for LE Audio
- Support for pairing using NFC tags

Additional profiles supported in RAM:

- Blood glucose monitor
- Temperature alarm
- Location
- Other custom profiles

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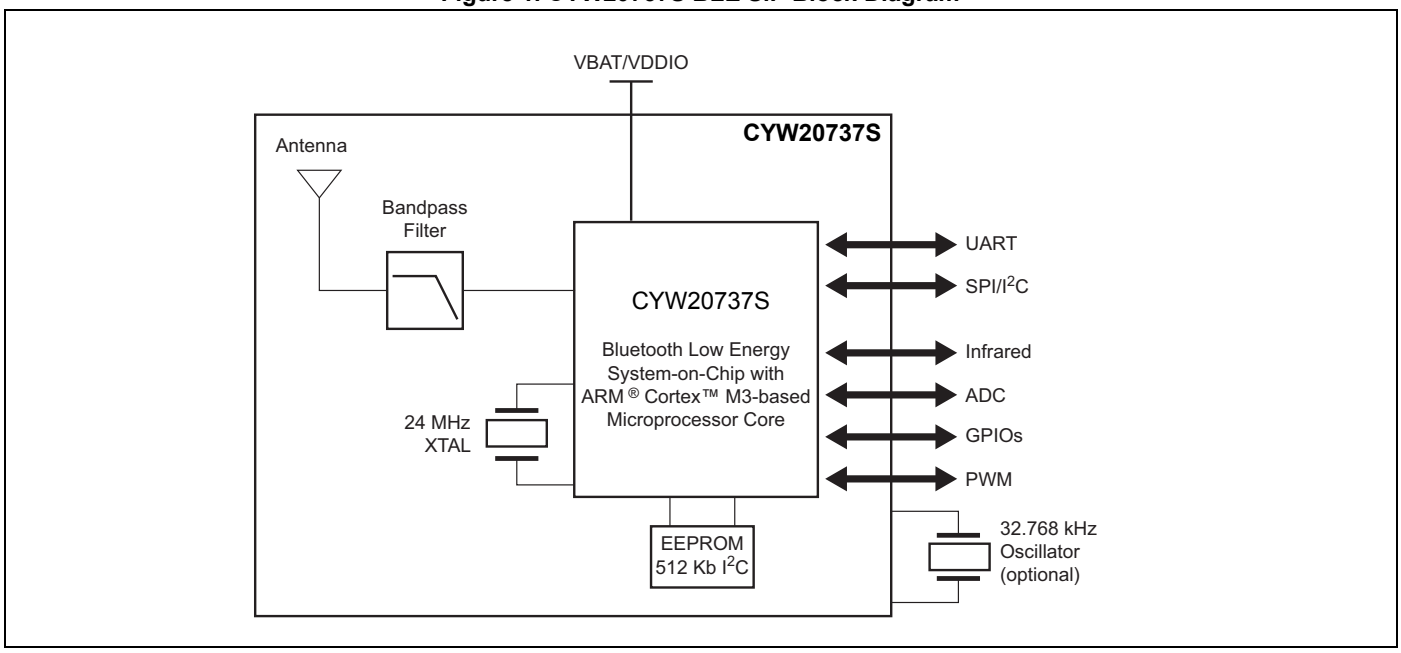
Figure 1. CYW20737S BLE SiP Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

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Contents

1. Functional Description 4
1.1 External Reset 4
1.2 32.768 kHz Oscillator 4
2. Pin Map and Signal Descriptions 5
3. Electrical Specifications 10
4. RF Specifications 11
5. ADC Specifications 12
6. Timing and AC Characteristics 13
6.1 SPI Timing 13
6.2 BSC Interface Timing 14
6.3 UART Timing 15
7. PCB Design and Manufacturing Recommendations 16
7.1 Pad and Solder Mask Opening Dimensions 16
7.2 PCB Layout Recommendations 16
7.3 PCB Stencil 17
7.4 Solder Reflow 17
8. Packaging and Storage Information 18
9. Mechanical Information 20
10. Ordering Information 22
Document History 23

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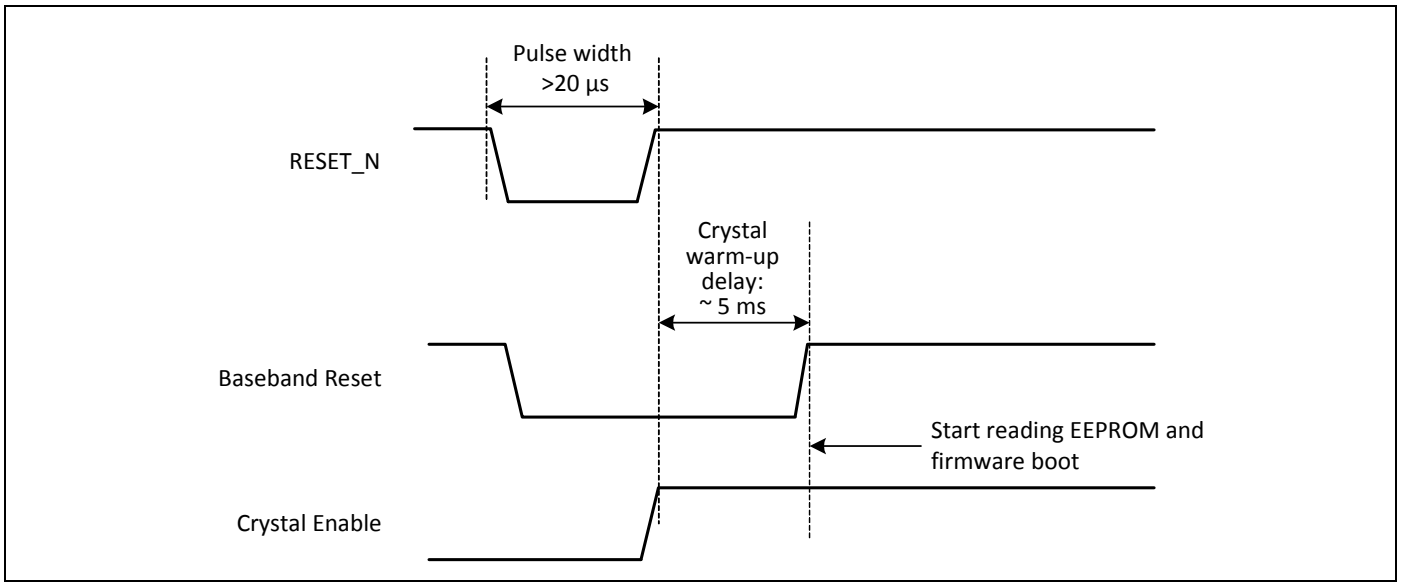
1. Functional Description

1.1 External Reset

External reset timing for the CYW20737S is illustrated in Figure 2.

Figure 2. External Reset Timing



1.2 32.768 kHz Oscillator

The CYW20737S includes a standard Pierce oscillator. The oscillator circuit includes a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis eliminates chatter when the input is near the comparator threshold (~100 mV). The oscillator circuit can is designed for a 32 kHz or 32.768 kHz crystal oscillator, and can also be driven by an external clock input with a similar frequency. Characteristics for a 32 kHz oscillator are defined in Table 2.

Table 2. 32 kHz Crystal Oscillator Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	F_{tol}	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	µs
Crystal drive level	P_{drv}	For crystal selection	0.5	–	–	µW
Crystal series resistance	R_{series}	For crystal selection	–	–	70	kΩ
Crystal shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

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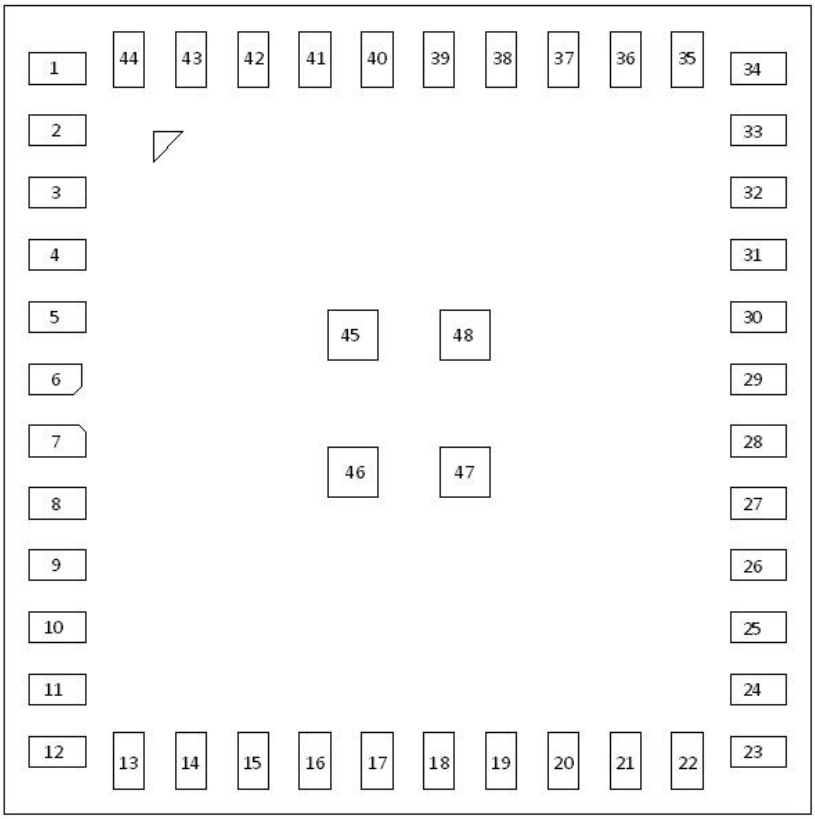
2. Pin Map and Signal Descriptions

The CYW20737S pin map is shown in Figure 3.

Figure 3. CYW20737S (TOP View)



The signal name, type, and description of each pin in the CYW20737S is listed in Table 3 on page 6. The symbols shown under I/O Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

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Table 3. Pin Descriptions

Pin	Name	I/O Type	Description
1	GPIO: P27 PWM1	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: MOSI (master and slave) for SPI_2
2	GND	GND	GND
3	VBAT	I	Battery supply input.
4	GND	GND	GND
5	GND	GND	GND
6	GND	GND	GND
7	GND	GND	GND
8	GND	GND	GND
9	GND	GND	GND
10	Reserved	–	Leave floating
11	GND	GND	GND
12	GND	GND	GND
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	UART_RX	I	UART_RX. This pin is pulled low through an internal 10 kΩ resistor.
19	UART_TX	O, PU	UART_TX
20	GND	GND	GND
21	SCL	I/O, PU	SCL I/O, PU clock signal for an external I^2C device
22	SDA	I/O, PU	SDA I/O, PU data signal for an external I^2C device
23	GND	GND	GND
24	GND	GND	GND
25	GPIO: P1	I	Default direction: Input. After POR state: Input floating. This pin is tied to the WP pin of the embedded EEPROM. Requires an external 10K pull-up
26	TMC	I	Test mode control. Pull this pin high to invoke test mode; leave it floating if not used. This pin is connected to GND through an internal 10 kΩ resistor.
27	RESET_N	I/O PU	Active-low system reset with open-drain output

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Table 3. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
28	GPIO: P0	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ Peripheral UART TX (PUART_TX) ■ MOSI (master and slave) for SPI_2 ■ IR_RX ■ 60Hz_main
29	GND	GND	GND
30	GPIO: P3	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART CTS (PUART_CTS) ■ SPI_CLK (master and slave) for SPI_2
31	GPIO: P2	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ SPI_CS (slave only) for SPI_2 ■ SPI_MOSI (master only) for SPI_2
32	GPIO: P4	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ MOSI (master and slave) for SPI_2. ■ IR_TX
33	GPIO: P8	I	Default direction: Input. After POR state: Input floating. Alternate functions: A/D converter input.
34	GPIO: P33	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (slave only) for SPI_2 ■ Auxiliary clock output (ACLK1) ■ Peripheral UART RX (PUART_RX)

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Table 3. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
35	GPIO: P32	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ SPI_CS (slave only) for SPI_2. ■ Auxiliary clock output (ACLK0) ■ Peripheral UART TX (PUART_TX)
36	GPIO: P25	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ MISO (master and slave) for SPI_2 ■ Peripheral UART RX (PUART_RX)
37	GPIO: P24	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ SPI_CLK (master and slave) for SPI_2 ■ Peripheral UART TX (PUART_TX)
38	NC	NC	No Connection (N/C).
39	GPIO: P13 PWM3	I	Default Direction: Input After POR State: Input Floating Drain current: 16 mA Alternate function: A/D converter input
	GPIO: P28 PWM2	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate functions: ■ A/D converter input ■ LED1 ■ IR_TX
40	GPIO: P14 PWM2	I	Default direction: Input. After POR state: Input floating. Alternate function: A/D converter input
	GPIO: P38	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (master and slave) for SPI_2 ■ IR_TX
41	GPIO: P15	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ IR_RX ■ 60 Hz_main

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Table 3. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
42	GPIO: P26 PWM0	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: SPI_CS (slave only) for SPI_2
43	GPIO: P12	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALO32K
	XTALO32K	O	Low-power oscillator (LPO) output. Alternate functions: P12 P26
44	GPIO: P11	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALI32K
	XTALI32K	I	Low-power oscillator (LPO) input. Alternate functions: ■ P11 ■ P27
45	GND	GND	GND
46	GND	GND	GND
47	GND	GND	GND
48	GND	GND	GND

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3. Electrical Specifications

Absolute maximum ratings are defined in Table 4.

Table 4. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply power	NA	3.63	V
Storage temperature	–40	125	°C
Voltage ripple	0	±2	%
Power supply (VBAT absolute maximum rating)	1.62	3.63	V

Power for the CYW20737S module is provided by the host through the power pins.

Table 5. Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	Battery voltage	1.62	–	3.63	V

Table 6. Current Consumption

Operating Mode	Condition	Nominal	Maximum	Unit
Receive	Receiver and baseband are both operating, 100%	24.0	28.0	mA
Transmit	Transmitter and baseband are both operating, 100%	24.0	28.0	mA
Sleep	Wake in < 5 ms	55.0	60.0	µA
Deep Sleep	Wake on interrupt	2.0	2.5	µA

Note: All measurements taken at 25°C

Based on the current measurements in Table 6 on page 10, CYW20737S peak power values are:

- RX: 101.6 mW
- TX: 101.6 mW
- Sleep mode: 217.8 µW
- Deep Sleep mode: 9.1 µW

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4. RF Specifications

CYW20737S receiver specifications are defined in Table 7.

Table 7. Receiver Specifications

Parameter	Mode and Conditions	Min.	Typ.	Max.	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity (standard)	Packets: 200 Payload: PRBS 9 Length: 37 Bytes Dirty Transmitter: off. PER: 30.8%	–	–94	–	dBm
Maximum input	–	–10	–	–	dBm

Note: All measurements taken at 3.0V (default voltage)

RF transmitter specifications are defined in Table 8.

Table 8. Transmitter Specifications

Parameter	Min.	Typ.	Max.	Unit
Transmitter				
Frequency range[a]	2402	–	2480	MHz
Output power adjustment range	–20	–	4	dBm
Output power	–	2	–	dBm
Output power variation	–	2.5	–	dB
LO Performance				
Initial carrier frequency tolerance	–	–	±150	kHz
Frequency Drift				
Frequency drift	–	–	±50	kHz
Drift rate	–	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence: 00001111)	225	–	275	kHz
Average deviation in payload (sequence: 10101010)	185	–	–	kHz
Channel spacing	–	2	–	MHz

a. This parameter is taken from the Bluetooth 4.0 specification.

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5. ADC Specifications

CYW20737S ADC specifications are defined in Table 9.

Table 9. ADC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Number of input channels	–	–	–	9	–	-
Channel switching rate	f_{ch}	–	–	–	133.33	Kch/s
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	Charging refsel	7.5	–	–	µs
Input resistance	R_{inp}	Effective, single-ended	–	500	–	kΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	F_c	–	5.859	–	187	kHz
Conversion time	T_c	–	5.35	–	170.7	µs
Resolution	R	–		16		Bits
Absolute voltage measurement error	–	Using on–chip ADC firmware driver	–	±2	–	%
Current	I	$I_{avdd1p2} + I_{avdd3p3}$	–	–	1	mA
Power	P	–	–	1.5	–	mW
Leakage Current	$I_{leakage}$	T = 25°C	–	–	100	nA
Power-up time	$T_{powerup}$	–	–	–	200	µs
Integral nonlinearity	I_{NL}	In the guaranteed performance range	–1	–	1	LSB[a]
Differential nonlinearity	D_{NL}	In the guaranteed performance range	–1	–	1	LSB[a]

a. LSBs are expressed at the 10-bit level.

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6. Timing and AC Characteristics

6.1 SPI Timing

SPI interface timing is illustrated in Figure 4 and Figure 5 and defined in Table 10 on page 14.

Figure 4. SPI Timing—Modes 0 and 2

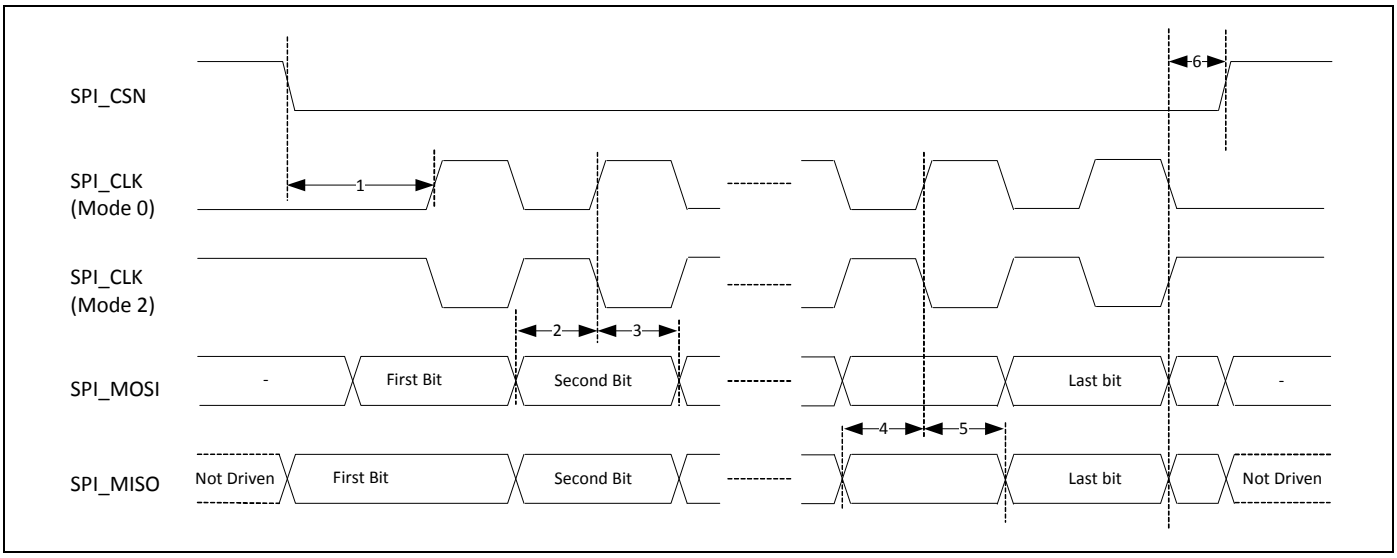

Figure 5. SPI Timing—Modes 1 and 3

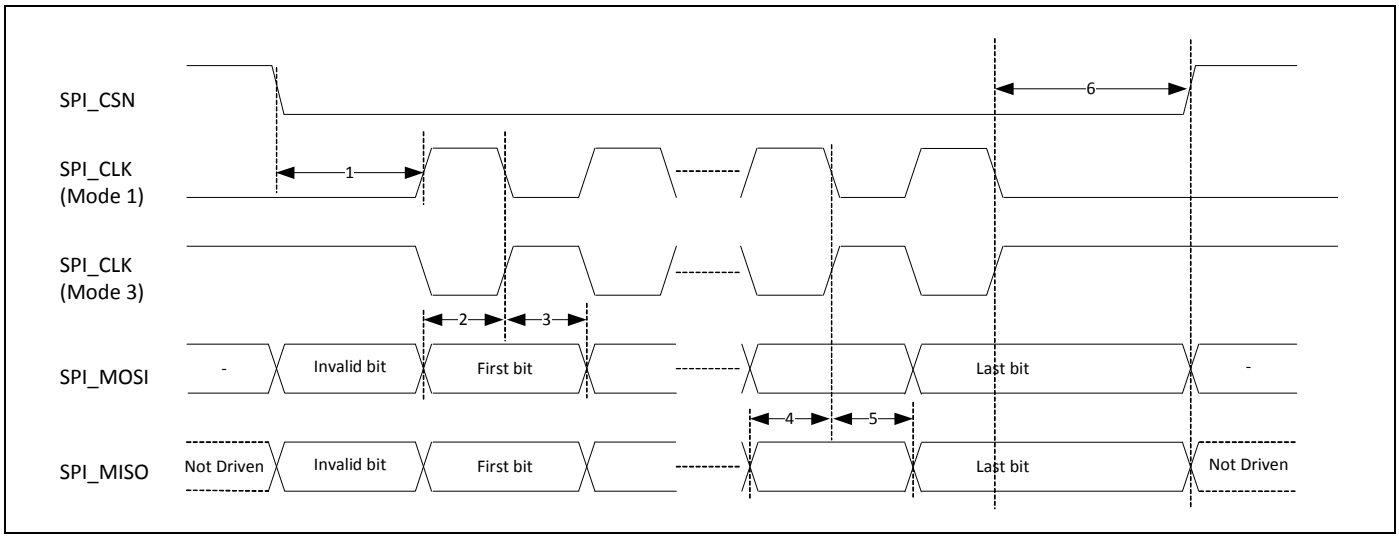

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Table 10. SPI Interface Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.
1	Time from CSN asserted to first clock edge	1 SCK	100	∞
2	Master setup time	–	1/2SCK	–
3	Master hold time	1/2SCK	-	–
4	Slave setup time	–	1/2 SCK	–
5	Slave hold time	1/2 SCK	–	–
6	Time from last clock edge to CSN deasserted	SCK	10 SCK	100

6.2 BSC Interface Timing

BSC interface timing is illustrated in Figure 6 and is defined in Table 11.

Figure 6. BSC Interface Timing

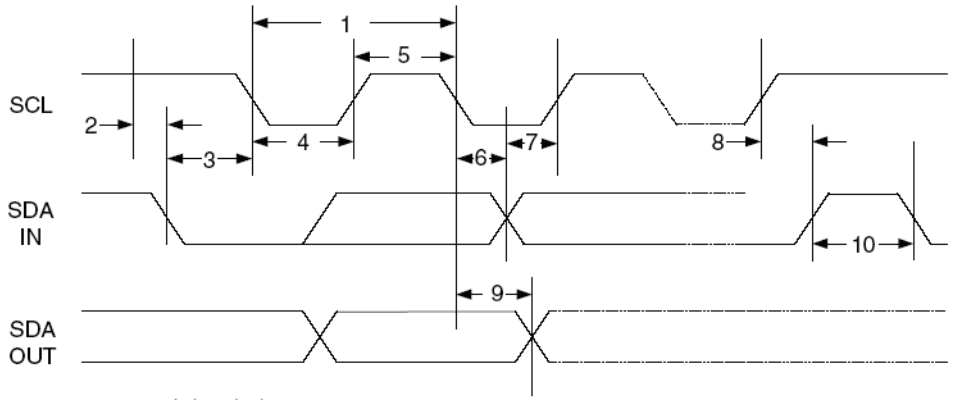

Table 11. BSC Interface Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Clock frequency	–	100, 400, 800, 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time	650	–	ns

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6.3 UART Timing

UART timing is illustrated in Figure 7 and defined in Table 12.

Figure 7. UART Timing

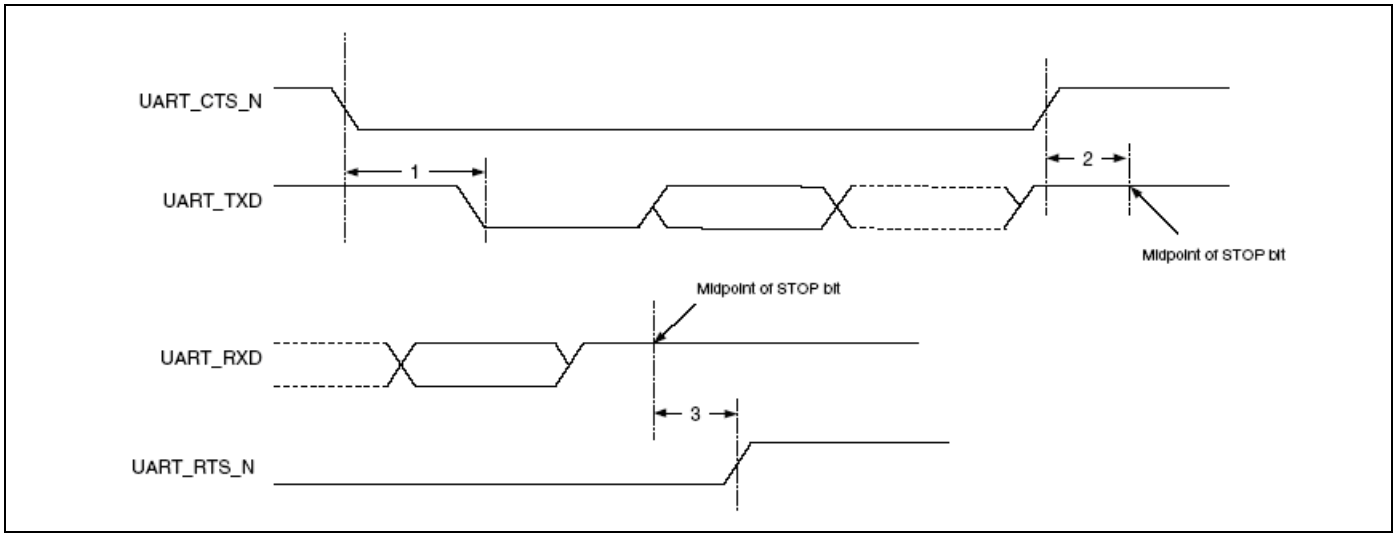

Table 12. UART Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baudout cycles

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7. PCB Design and Manufacturing Recommendations

7.1 Pad and Solder Mask Opening Dimensions

CYW20737S pad and solder mask opening dimensions are defined in Table 13.

Table 13. Pad and Solder Mask Dimensions

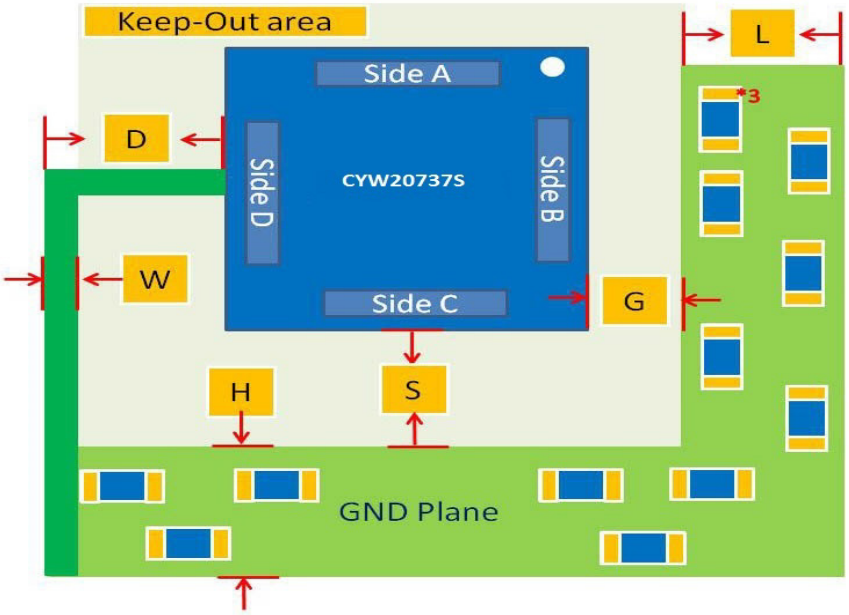
Pad Type	Pad Dimensions	Solder Mask Opening Dimensions	Unit
Type A	0.6 × 0.25	0.7 × 0.35	mm
Type B	0.55 × 0.3	0.65 × 0.4	
Type C	0.4 × 0.4	0.5 × 0.5	

7.2 PCB Layout Recommendations

The following layout recommendations are referenced to Figure 8 on page 16.

- Connect to system ground from side D of the module (pins 13–22).
- The L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- An L-shaped ground plane is required. If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout in Figure 8 on page 16 and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)
- Route signal traces out of the module from side C (between pins 27 and 30) or side D (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or side B.

Figure 8. PCB Layout Example



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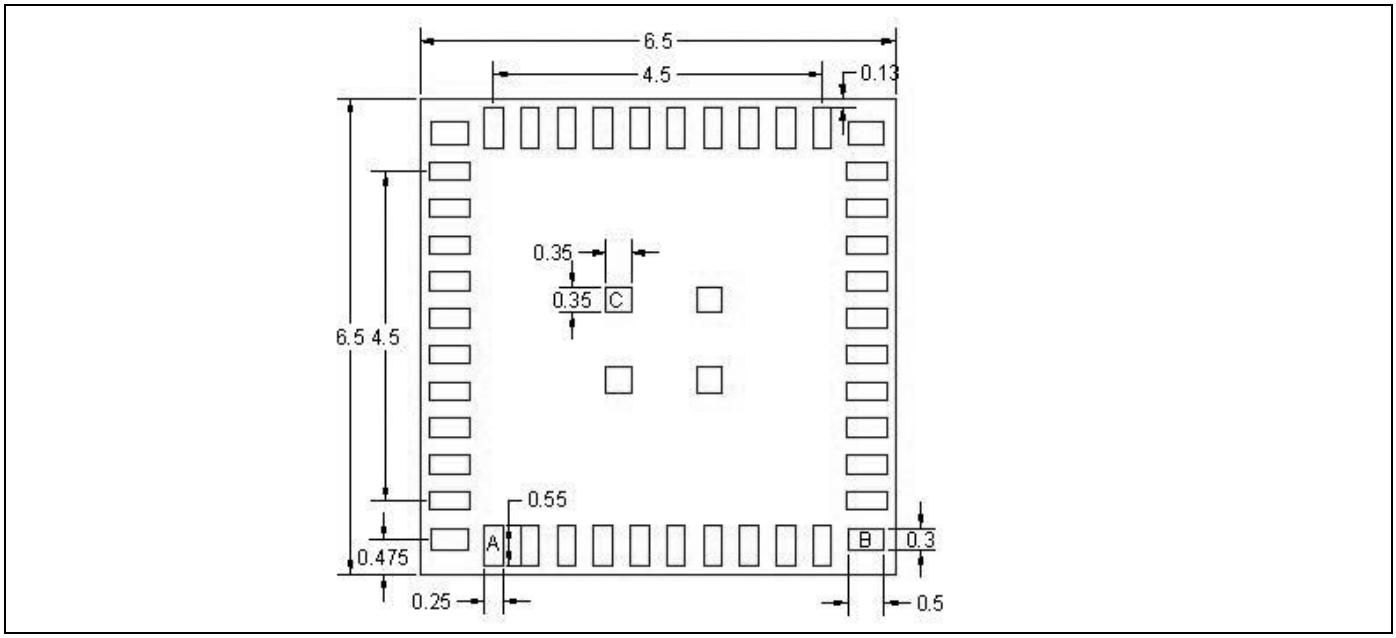
7.3 PCB Stencil

The recommended PCB stencil is shown in Figure 9 (all measurements in mm). Use an unsolder mask to set the module footprint.

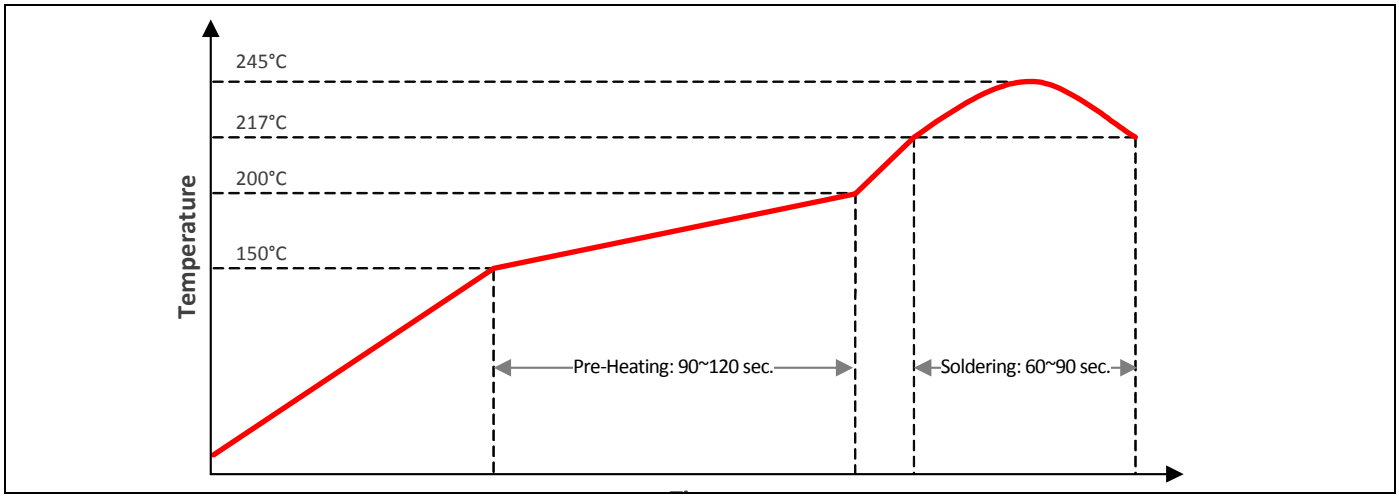
Figure 9. CYW20737S Stencil (Bottom View)



7.4 Solder Reflow

The recommended solder reflow profile for the CYW20737S is defined in Figure 10.

Figure 10. Solder Reflow Profile



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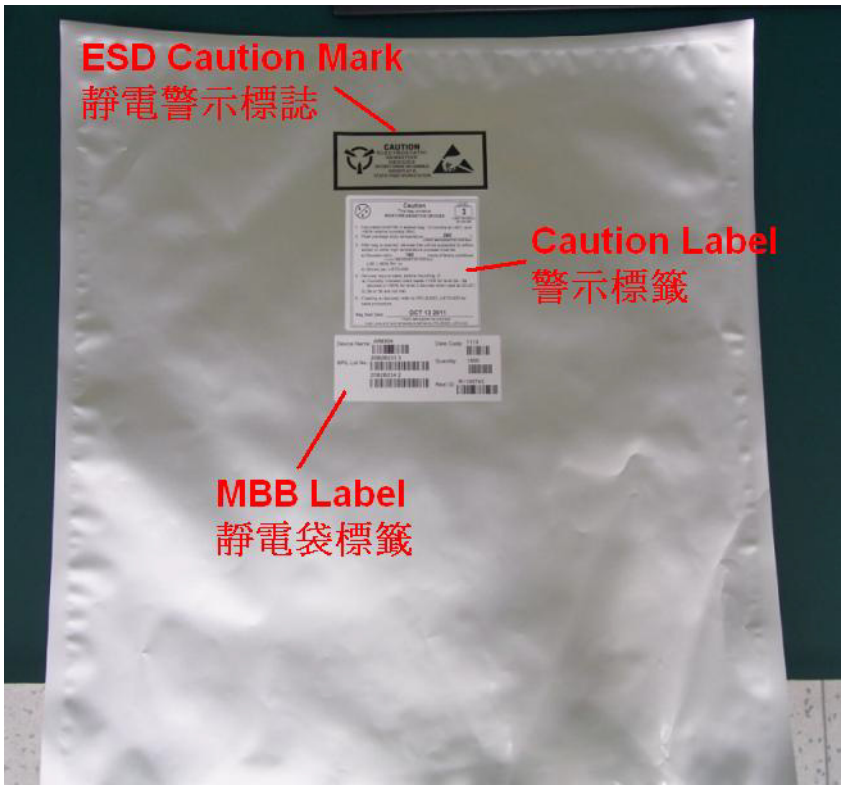
8. Packaging and Storage Information

The CYW20737S is available in a tape and reel package and is shipped in an ESD-protected moisture-resistant (MSL-3) bag as shown in Figure 11. The storage temperature range is –40°C to +125°C.

Figure 11. CYW20737S ESD/Moisture Packaging



The moisture sensitivity label on the CYW20737S shipping bag is shown in Figure 12 on page 19.

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Figure 12. CYW20737S Moisture Sensitivity Label

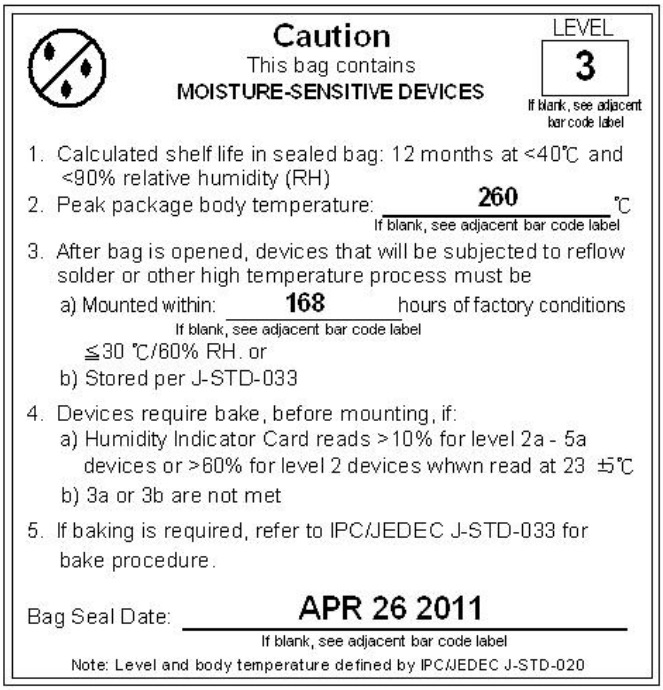
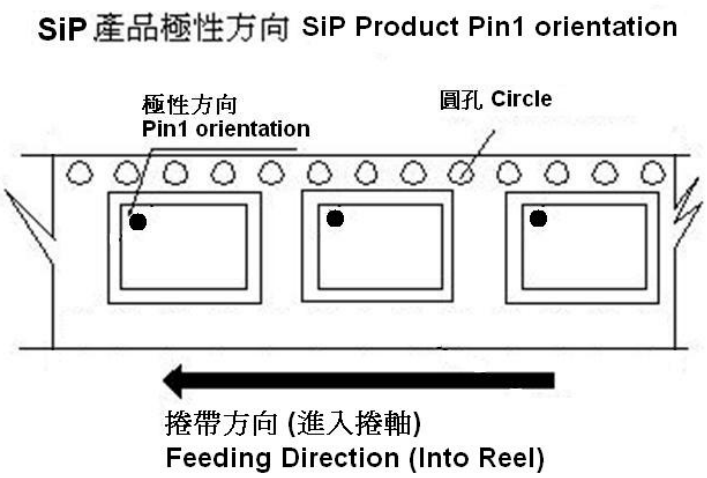


Figure 13 shows the location of pin 1 on the CYW20737S relative to its orientation on the tape packaging.

Figure 13. CYW20737S Tape and Reel Pin 1 Location



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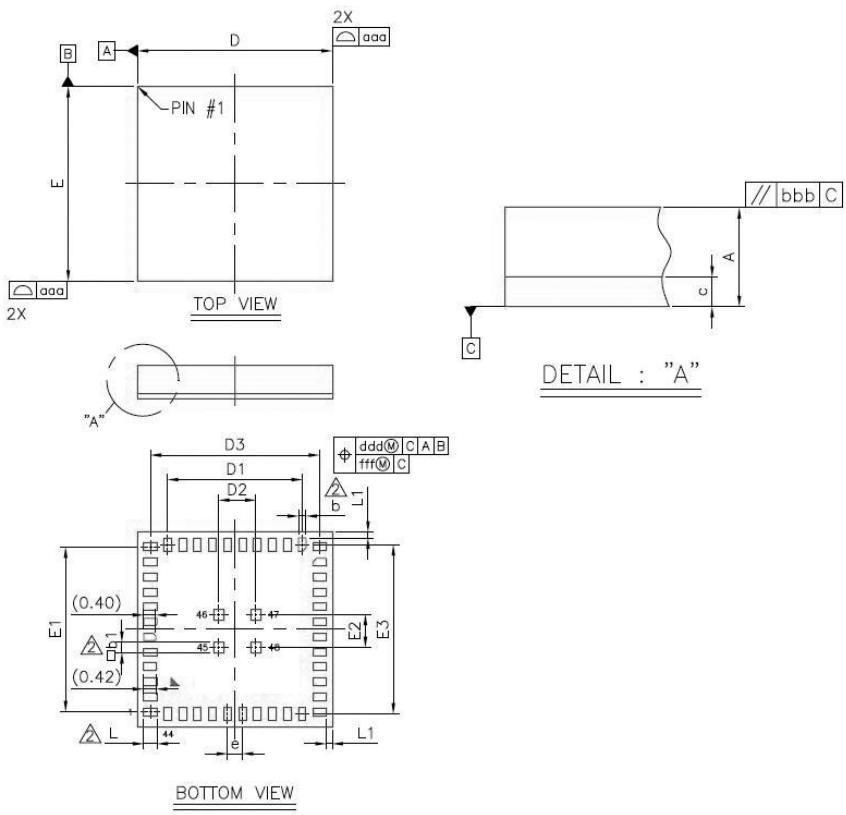
9. Mechanical Information

Package dimensions for the CYW20737S are shown in Figure 14.

Figure 14. CYW20737S Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.18	---	---	0.046
c	0.17	0.20	0.23	0.007	0.008	0.009
D/E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	4.50	---	---	0.177	---
E1	---	5.50	---	---	0.217	---
D2	---	1.24	---	---	0.049	---
E2	---	1.10	---	---	0.043	---
D3/E3	---	5.65	---	---	0.222	---
e	---	0.50	---	---	0.020	---
b	---	0.25	---	---	0.010	---
L	---	0.45	---	---	0.018	---
b1	---	0.35	---	---	0.014	---
L1	---	0.20	---	---	0.008	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.10			0.004		
fff	0.05			0.002		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b,b1,L IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.

Additional CYW20737S package dimensions are shown in Figure 15 on page 21.

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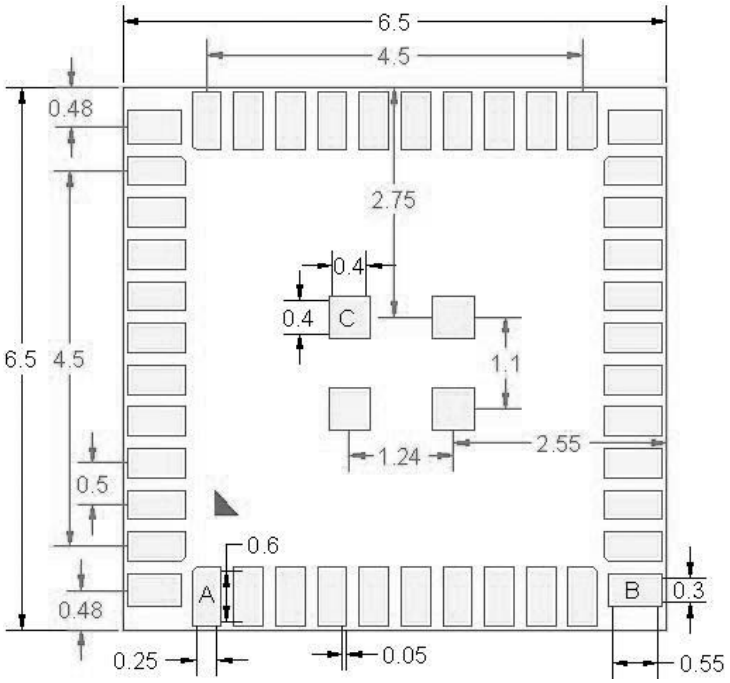
Figure 15. CYW20737S Pin Dimensions (Bottom View)



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10. Ordering Information

Table 14. Ordering Information

Part Number	Package	Operating Temperature	Humidity
CYW20737S	48-pin LGA	–40°C to +85°C	95% max., noncondensing

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Document History

Document Title: CYW20737S Bluetooth Low Energy System-in-Package (SiP) Module Document Number: 002-14888				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	09/26/2014	20737S-DS100-R: Initial release
*A	–	UTSV	11/06/2015	20737S-DS101-R: Updated • Table 5 on page 14
*B	5444054	UTSV	09/23/2016	Updated to Cypress Template
*C	5688156	AESATMP7	04/21/2017	Updated Cypress Logo and Copyright.

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