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KAF-16200

4500 (H) x 3600 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−16200 is a single output, high performance CCD (charge coupled device) image sensor with 4500 (H) x 3600 (V) photoactive pixels designed for a wide range of color or monochrome image sensing applications. Each pixel contains anti−blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.0 μm square pixels of the color version are selectively covered with red, green or blue pigmented filters for color separation. Microlenses are added for improved sensitivity on both color and monochrome sensors.

The sensor utilizes a transparent gate electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD with Square Pixels
Total Number of Pixels	4641 (H) x 3695 (V) = 17.0 M
Number of Effective Pixels	4540 (H) x 3640 (V) = 16.5 M
Number of Active Pixels	4500 (H) x 3600 (V) = 16.2 M
Pixel Size	6.0 μm (H) x 6.0 μm (V)
Active Image Size	27.0 mm (H) x 21.6 mm (V) 34.6 mm Diag., APS−H Optical Format
Aspect Ratio	5:4
Output Sensitivity (Q/V)	31 μV/e⁻
Charge Capacity (24 MHz)	41 ke⁻
Read Noise (f = 24 MHz)	14 e⁻ rms
Dark Current (60°C)	112 e⁻/s
Dynamic Range	69 dB linear
Quantum Efficiency (Peak) Color (600, 549, 480 nm) Monochrome (540 nm)	 33%, 40%, 33% 56%
Maximum Frame Rate	1.23 fps
Maximum Data Rate	24 MHz
Blooming Protection	2000 X Saturation Exposure

NOTE: Unless noted, all parameters are specified at 25°C.

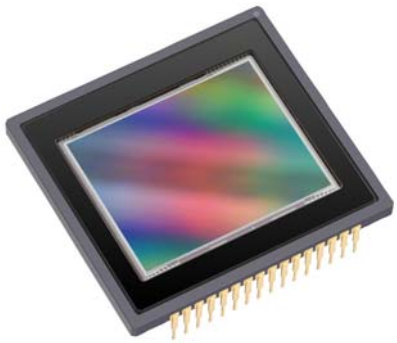


Figure 1. KAF−16200 CCD Image Sensor

Features

- Transparent Gate Electrode for High Sensitivity
- High Resolution, 35 mm Diagonal Format
- Broad Dynamic Range
- Low Noise
- Large Image Area

Applications

- Astrophotography
- Scientific Imaging

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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January, 2017 − Rev. 2
Publication Order Number:
KAF−16200/D

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ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAF−16200−ABA−CD−B1	Monochrome, Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Grade 1	KAF−16200−ABA Serial Number
KAF−16200−ABA−CD−B2	Monochrome, Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Grade 2	
KAF−16200−ABA−CD−AE	Monochrome, Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Engineering Grade	
KAF−16200−FXA−CD−B1	Gen2 Color (Bayer RGB), Special Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Grade 1	KAF−16200−FXA Serial Number
KAF−16200−FXA−CD−B2	Gen2 Color (Bayer RGB), Special Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Grade 2	
KAF−16200−FXA−CD−AE	Gen2 Color (Bayer RGB), Special Microlens, CERDIP Package, Sealed Clear Cover Glass with AR Coating (both sides), Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

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DEVICE DESCRIPTION

Architecture

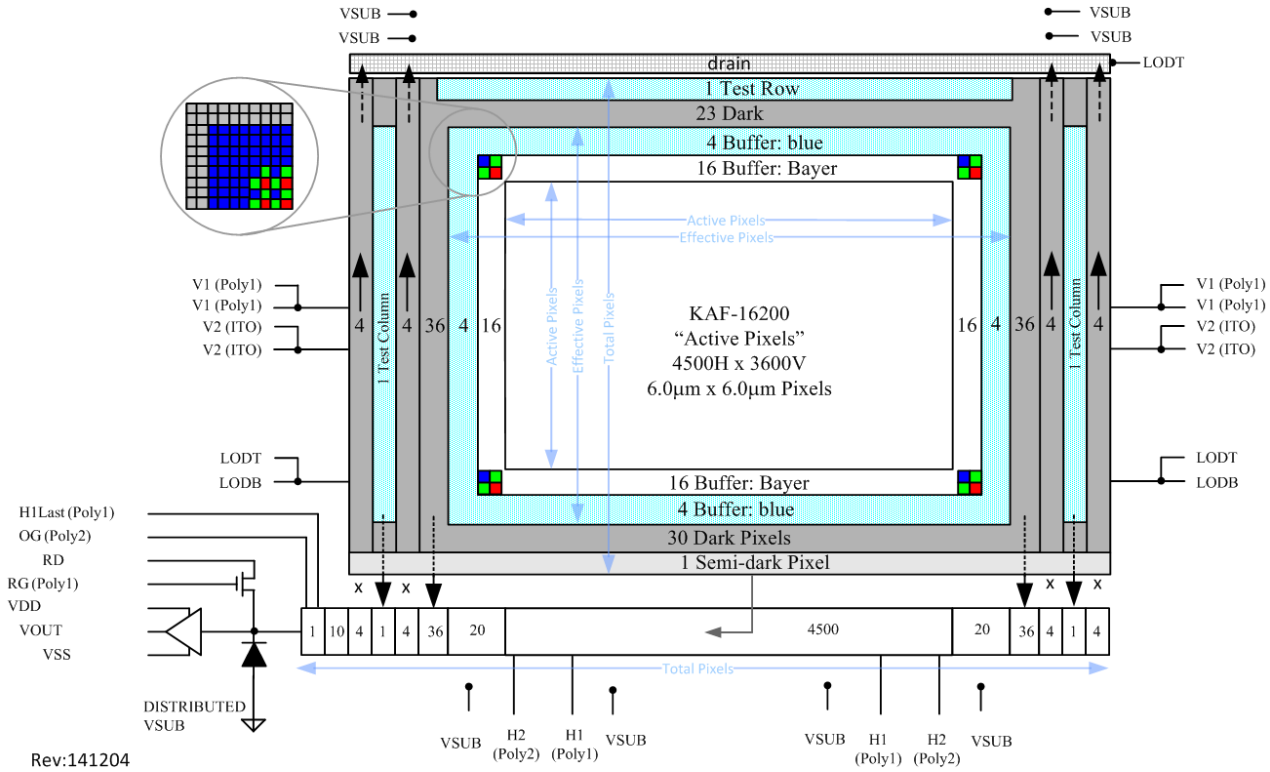


Figure 2. Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region are light shielded pixels that include 36 leading dark pixels on every line. There are also 30 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dummy Pixels

Within each horizontal shift register there are 20 leading additional shift phases 1 + 10 + 4 + 1 + 4 (See Figure 2). These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 20 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non−uniformities. For the leading 20 active column pixels, the first 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B).

CTE Monitor Pixels

Two CTE test columns, one on each of the leading and trailing ends and one CTE test row are included for manufacturing test purposes.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the device. These photon−induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non−linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

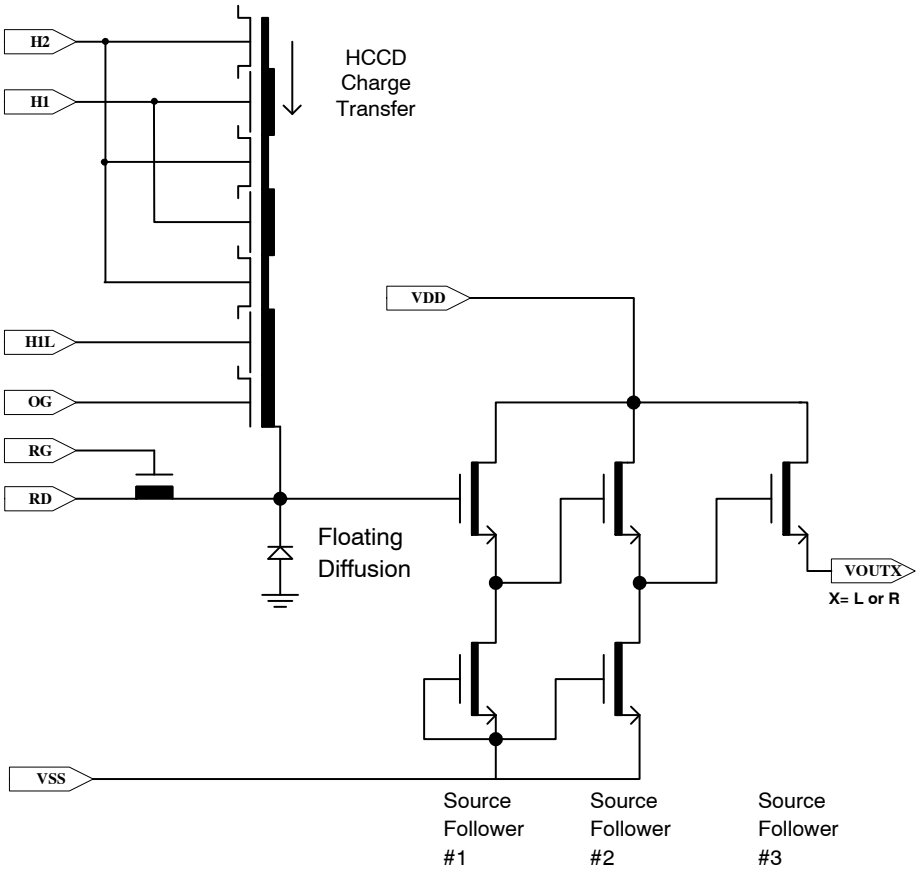
Charge Transport

The integrated charge from each photogate (pixel) is transported to the output using a two−step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented with a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion output amplifier. On each falling edge of H1L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

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HORIZONTAL REGISTER

Output Structure



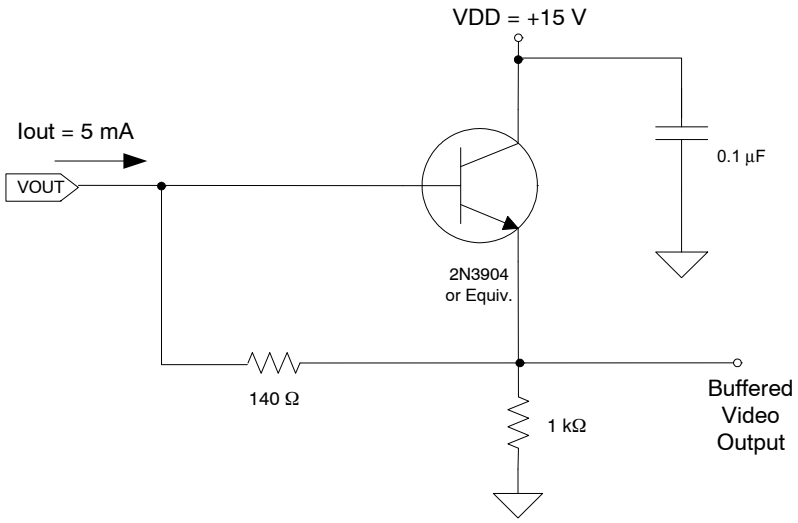
Note: Represents either the left or the right output. The designation is omitted in the figure.

Figure 3. Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three−stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off−chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off−chip current source must be added to the VOUT pins of the device. See Figure 4.

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Output Load



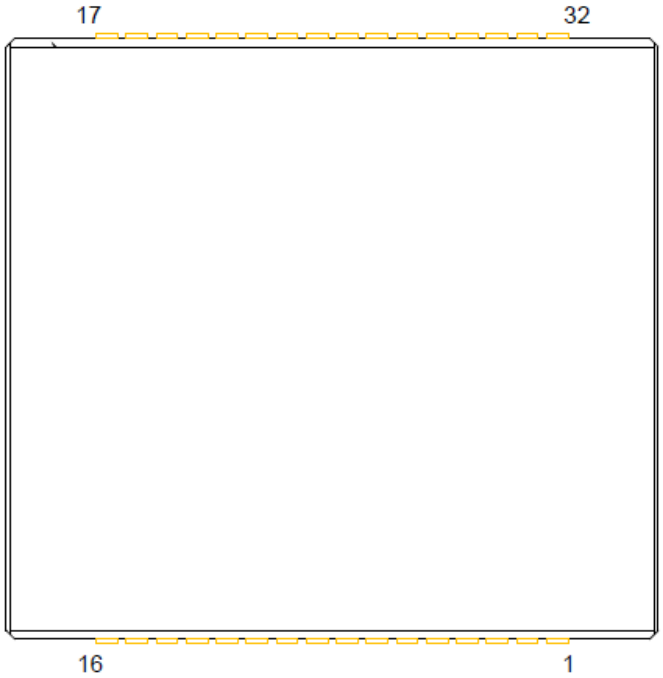
Note: Component values may be revised based on operating conditions and other design considerations.

Figure 4. Recommended Output Structure Load Diagram

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PHYSICAL DESCRIPTION

Pin Description and Device Orientation



Note: As viewed from the bottom.

Figure 5. Pinout Diagram

Table 3. PINOUT

Pin	Name	Description
1	VSUB	Substrate
2	H1LAST	Last Horizontal Phase
3	OG	Output Gate
4	RG	Reset Gate
5	RD	Reset Drain
6	VSS	Amplifier Return
7	VOUT	Video Output
8	VDD	Amplifier Supply
9	H2	Horizontal Phase 2
10	H1	Horizontal Phase 1
11	VSUB	Substrate
12	VSUB	Substrate
13	VSUB	Substrate
14	H1	Horizontal Phase 1
15	H2	Horizontal Phase 2
16	VSUB	Substrate

Pin	Name	Description
17	VSUB	Substrate
18	LODB	Lateral Overflow Drain, Bottom of Die
19	V1	Vertical Phase 1
20	V1	Vertical Phase 1
21	V2	Vertical Phase 2
22	V2	Vertical Phase 2
23	LODT	Lateral Overflow Drain, Top of Die
24	VSUB	Substrate
25	VSUB	Substrate
26	LODT	Lateral Overflow Drain, Top of Die
27	V2	Vertical Phase 2
28	V2	Vertical Phase 2
29	V1	Vertical Phase 1
30	V1	Vertical Phase 1
31	LODB	Lateral Overflow Drain, Bottom of Die
32	VSUB	Substrate

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IMAGING PERFORMANCE

Table 4. TYPICAL OPERATIONAL CONDITIONS

Description	Condition	Notes
Readout Time ($t_{READOUT}$)	652 ms	Includes Overclock Pixels
Integration Time (t_{INT})	Varies per Test: Bright Field 250 ms, Dark Field 1 sec, Saturation 250 ms, Low Light 33 ms	
Horizontal Clock Frequency	24 MHz	
Temperature	25°C	Room Temperature
Mode	Integrate − Readout Cycle	
Operation	Typical Operating Conditions	

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Table 5. SPECIFICATIONS

Description	Symbol	Min	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal	Ne^-_{SAT}	35	41		ke^-		Design[10]
Charge to Voltage Conversion	Q/V		31		$\mu V/e^-$	1	Design[10]
Quantum Efficiency at Peak Red Green Blue	QE_{MAX}		 33 40 33		%		Design[10]
Quantum Efficiency at Peak − Mono	QE_{MAX}		56		%		Design[10]
Photo Response Non-Linearity (10−90% Nsat)	PRNL		4	10	%		Die[9]
Green difference (color devices only)	Gr/Gb		2	4.4	%		Die[9]
Photo Response Non-Uniformity	PRNU		10	25	%p−p	2	Die[9]
Readout Dark Current (at 60°C)	Jd		175	233	pA/cm^2	3	Die[9]
Integration Dark Current (at 60°C)	Jd		62	100	pA/cm^2	12	Die[9]
Dark Signal Non-Uniformity	DSNU		0.26	4	mV p−p	5	Die[9]
Dark Signal Doubling Temperature	ΔT		4.7		°C	11	Design[10]
Read Noise	N_R		14	21	e^- rms		Die[9]
Dynamic Range	DR		69.3		dB	4	Design[10]
Horizontal Charge Transfer Efficiency	HCTE	0.999995	0.999999			5	Die[9]
Vertical Charge Transfer Efficiency	VCTE	0.999999	0.999999				Die[9]
Blooming Protection	X_{AB}		2000		x V_{SAT}	6	Design[10]
DC Offset, Output Amplifier	V_{ODC}	7.0	8.2	9.3	V	7	Die[9]
Output Amplifier Bandwidth	f_{-3dB}		220		MHz		Design[10]
Output Impedance, Amplifier	R_{OUT}	100	124	145	Ω		Die[9]
Reset Feedthru	V_{RFT}		0.5		V		Design[10]

1. Increasing output load currents to improve bandwidth will decrease the conversion factor (Q/V).
2. Difference between the maximum and minimum average signal levels of 168 × 168 blocks within the sensor on a per color basis as a % of average signal level.
3. Readout dark current is measured at T = 60°C, with t_{INT} = 0, from the average non-illuminated signal with respect to the over-clocked horizontal register signal.
4. 20log (Ne^-_{SAT} / N_R). Specified at T = 60°C.
5. Measured per transfer above and below (~70% V_{SAT} min) saturation exposure levels. Typically, no degradation in HCCD CTE is observed up to 24 MHz.
6. X_{AB} is the number of times above the V_{SAT} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_{AB} is measured at 4 ms.
7. Video level offset with respect to ground.
8. Total dark signal = ($V_{DARK,INT}$ * t_{INT}) + $V_{DARK,READ}$ * $t_{READOUT}$.
9. A parameter that is measured on every sensor during production testing.
10. A parameter that is quantified during the design verification activity.
11. This value is valid only near 25°C.
12. Integration dark current is measured at T = 60°C, from the average non−illuminated signal signal with respect to the over−clocked vertical register signal.

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TYPICAL PERFORMANCE CURVES

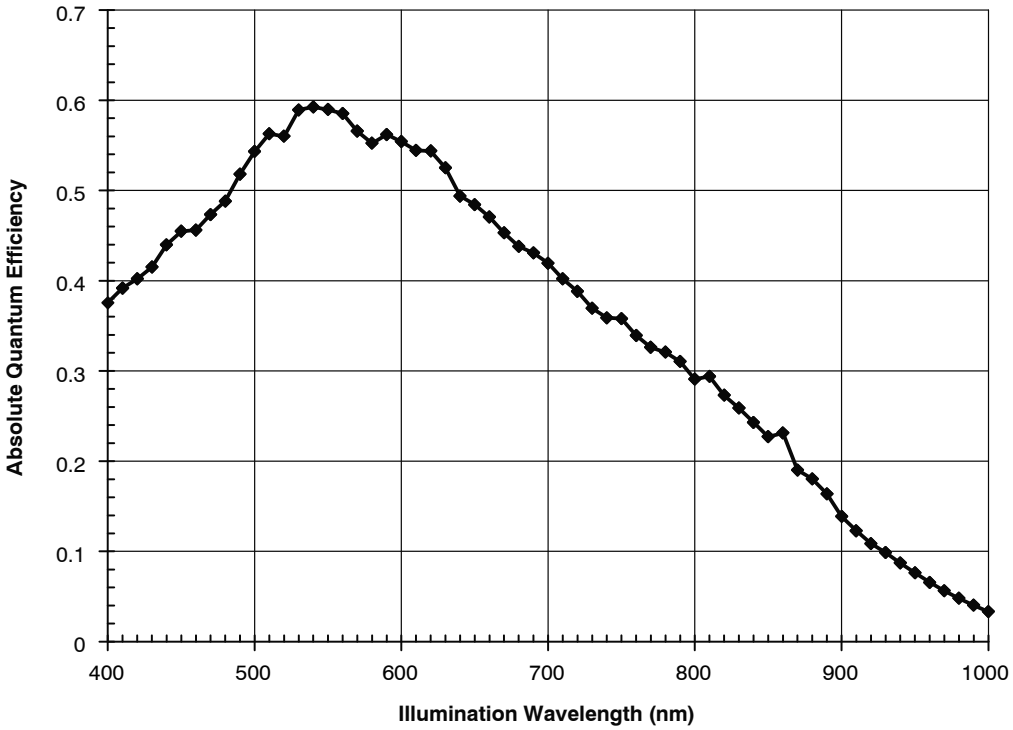


Figure 6. Typical Monochrome Quantum Efficiency

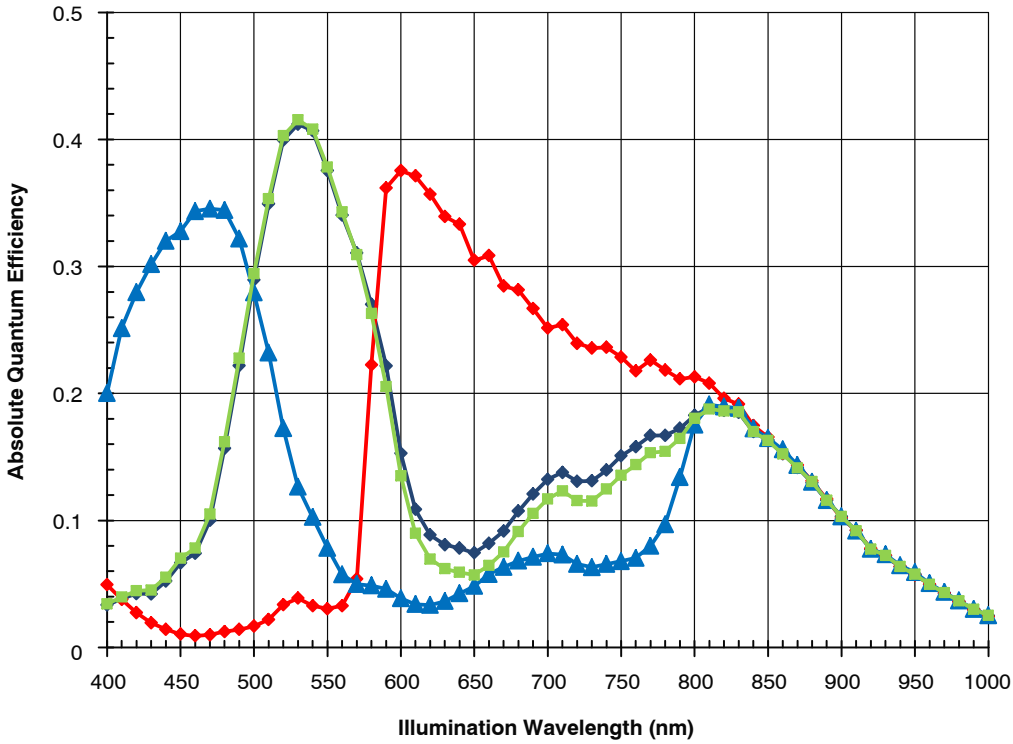


Figure 7. Typical Color Quantum Efficiency

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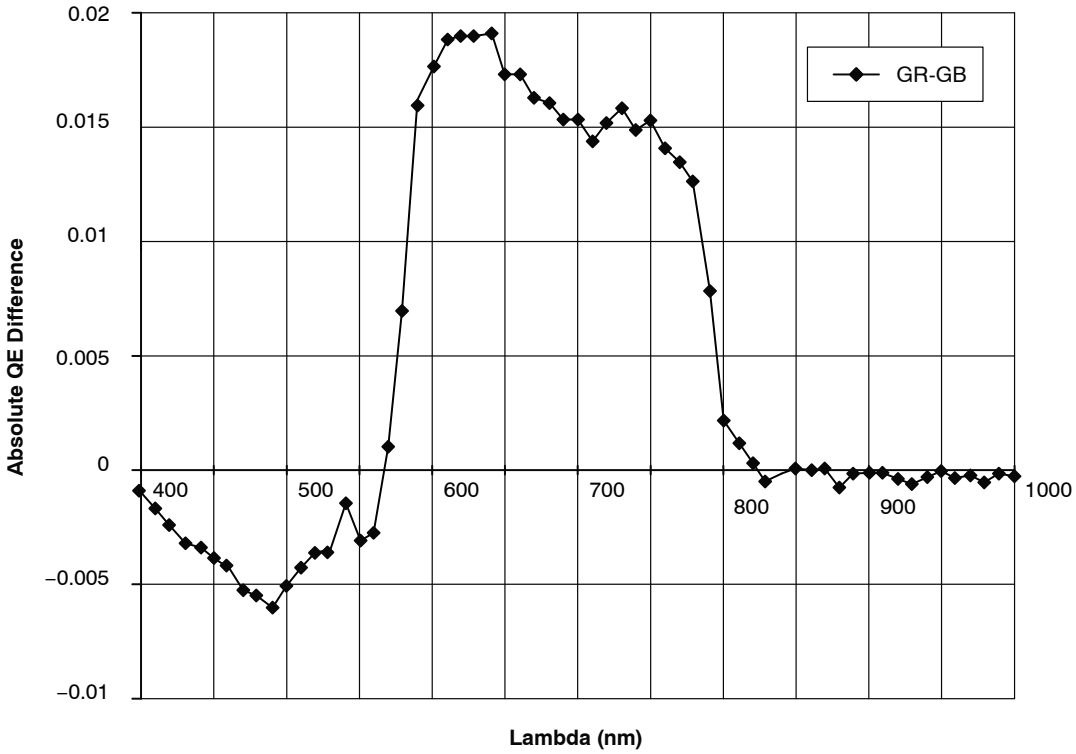


Figure 8. Typical Green (Red) − Green (Blue) Quantum Efficiency Difference

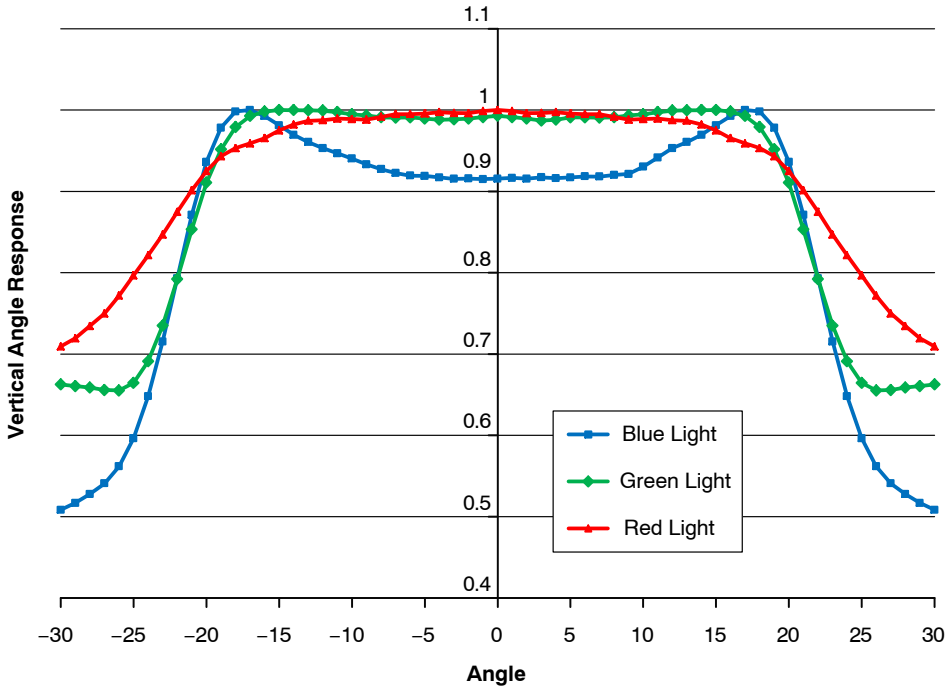


Figure 9. Typical Vertical Angular Dependance of Quantum Efficiency for Monochrome Devices

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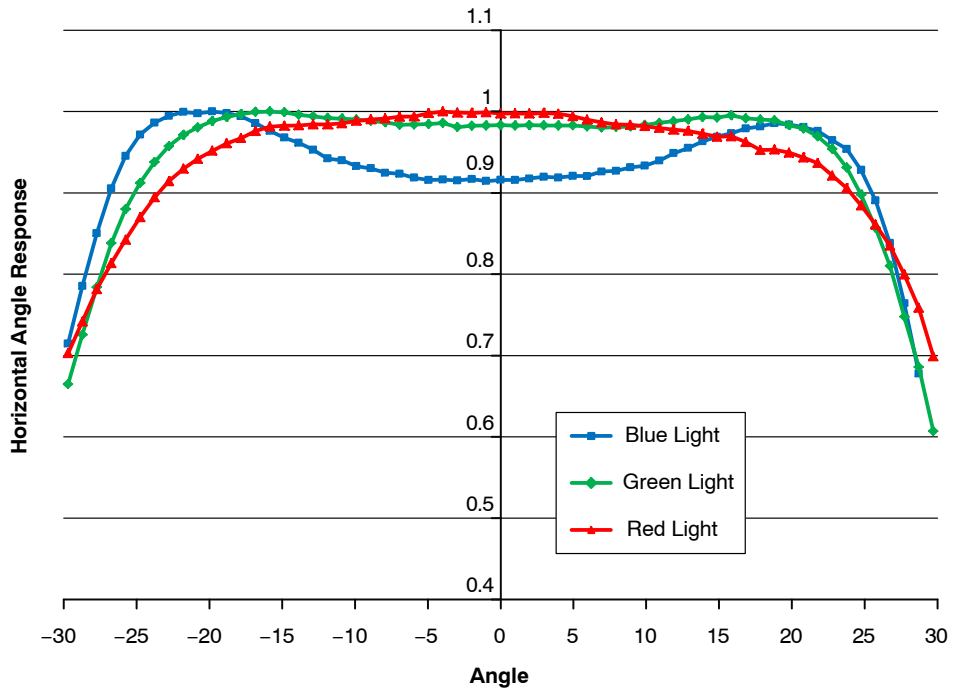


Figure 10. Typical Horizontal Angular Dependance of Quantum Efficiency for Monochrome Devices

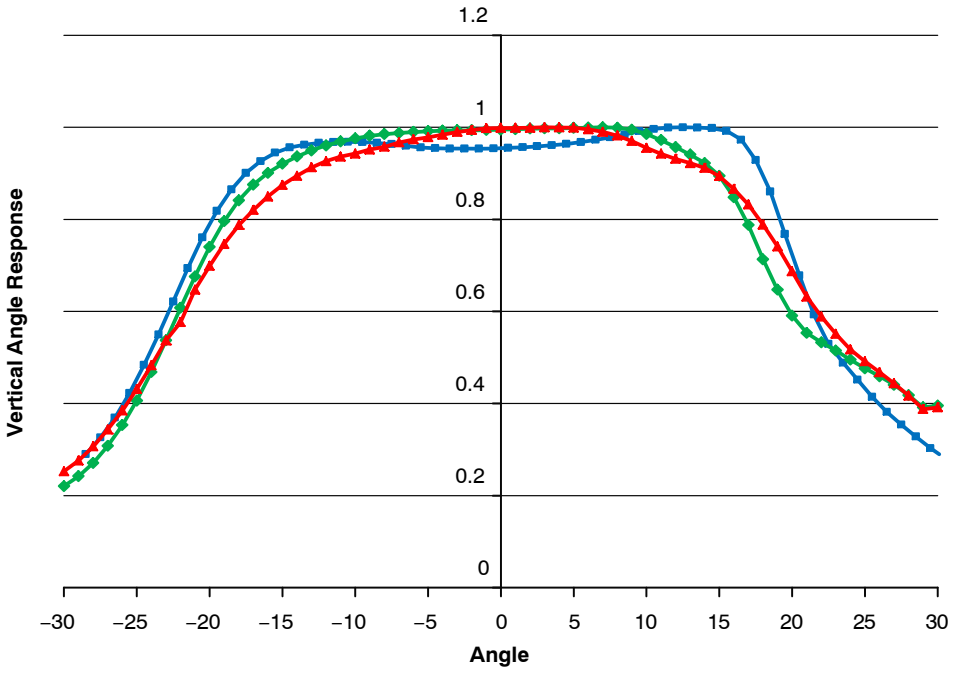


Figure 11. Typical Vertical Angular Dependance of Quantum Efficiency for Color Devices

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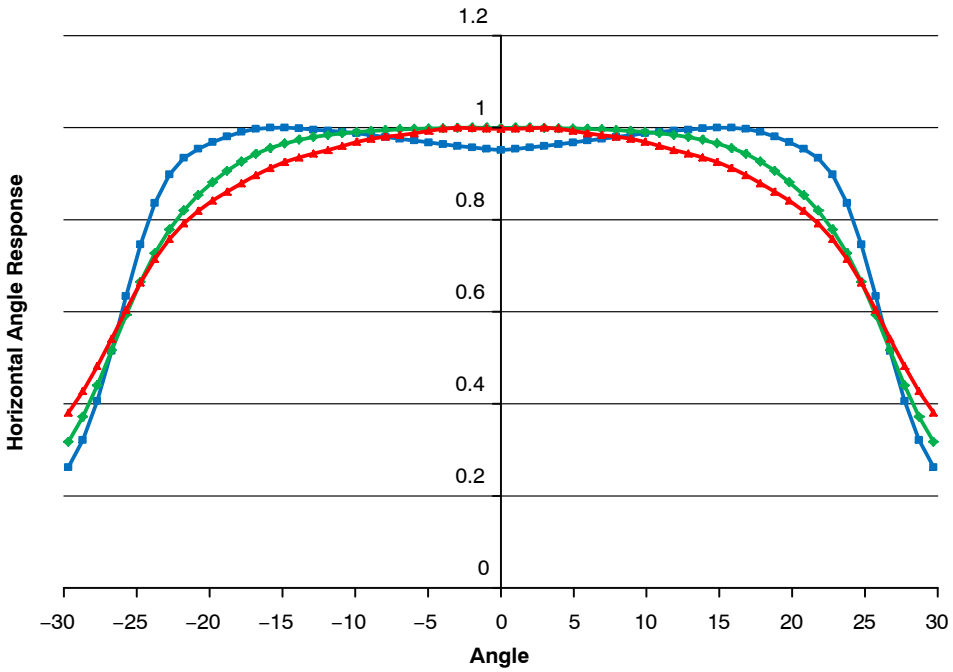


Figure 12. Typical Horizontal Angular Dependance of Quantum Efficiency for Color Devices

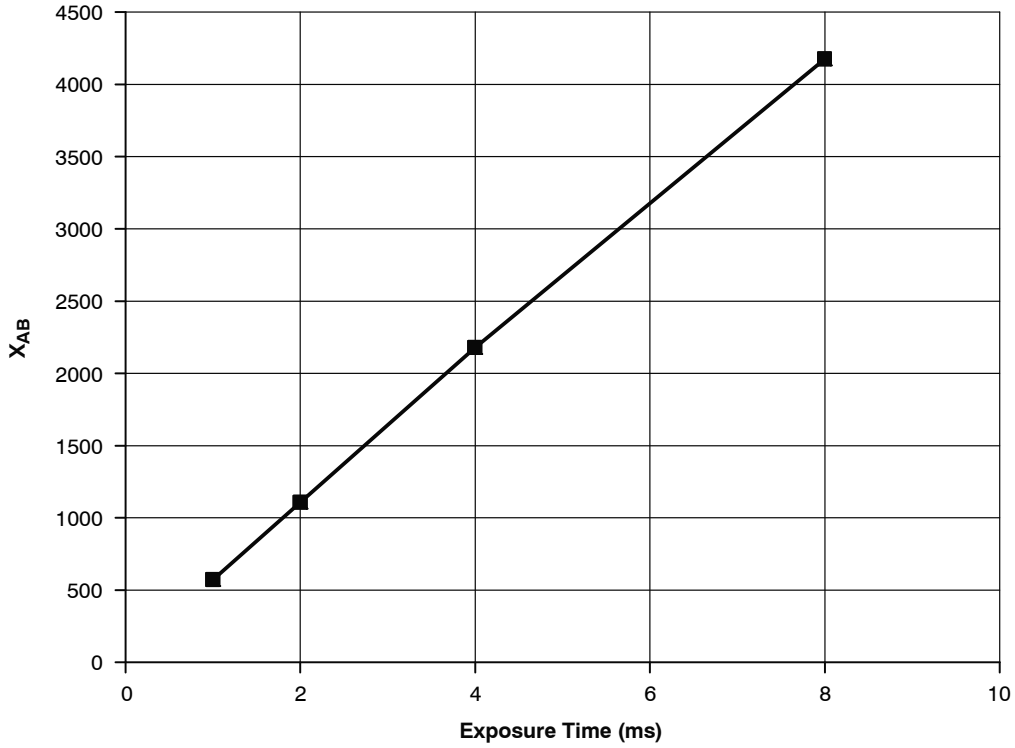


Figure 13. Typical Anti-Blooming Performance: Signal vs. Exposure

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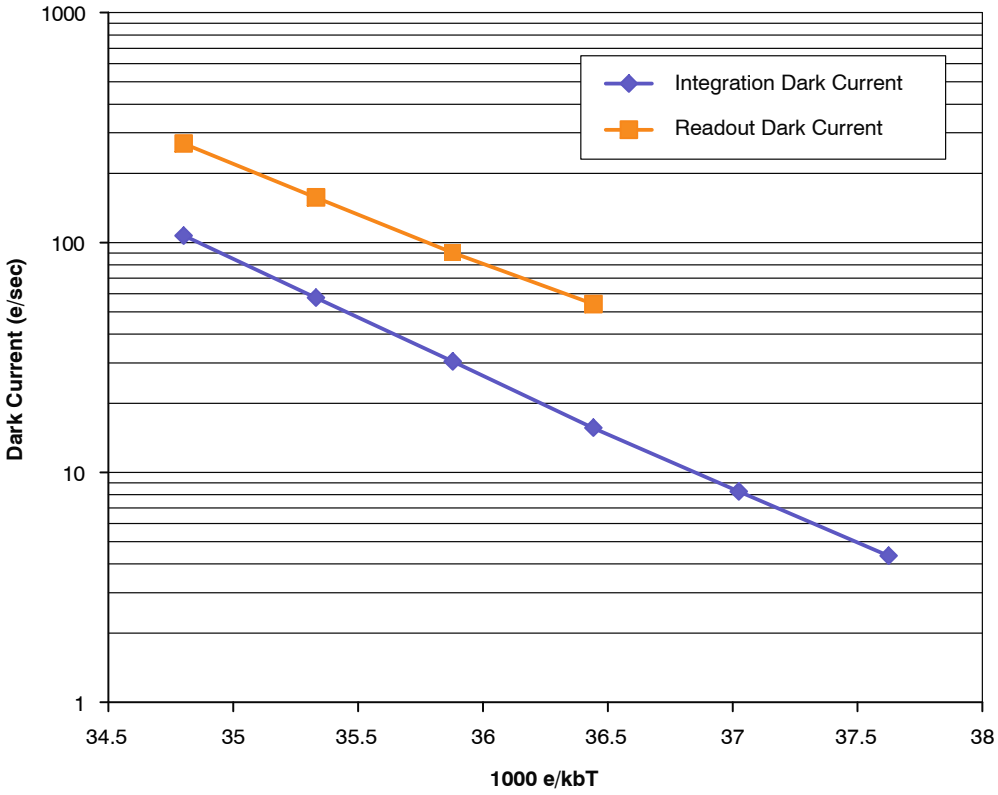


Figure 14. Typical Dark Current Performance vs. Temperature

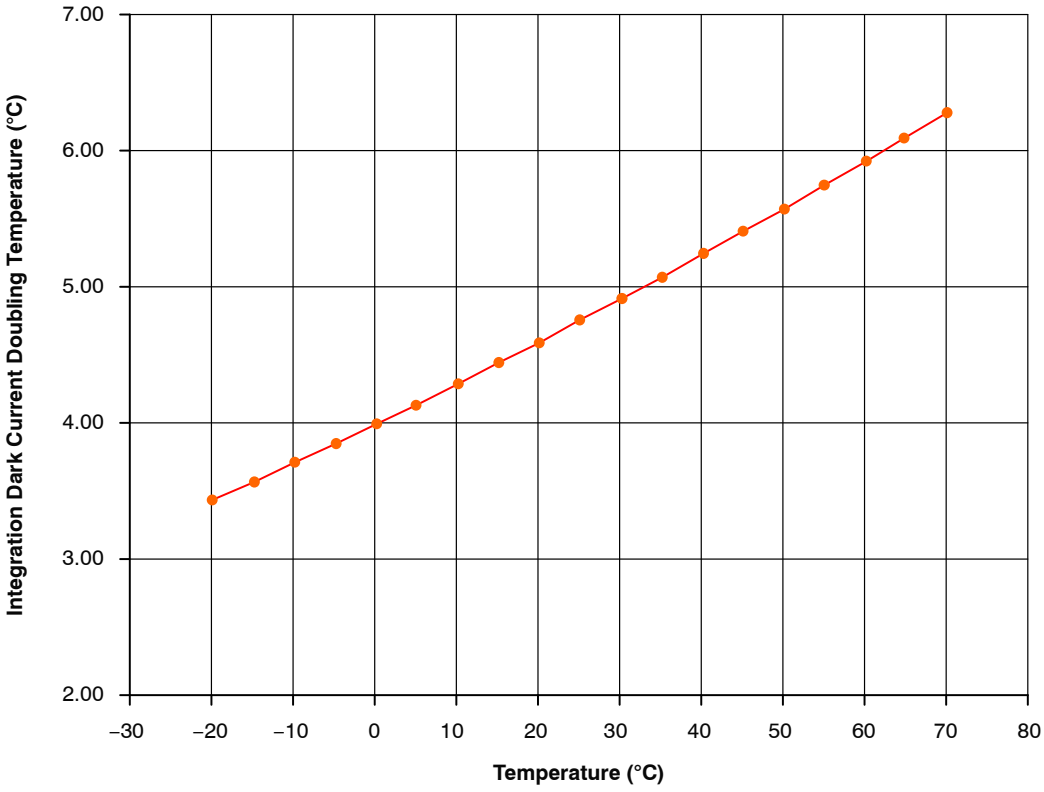


Figure 15. Dark Current Doubling Temperature Dependence

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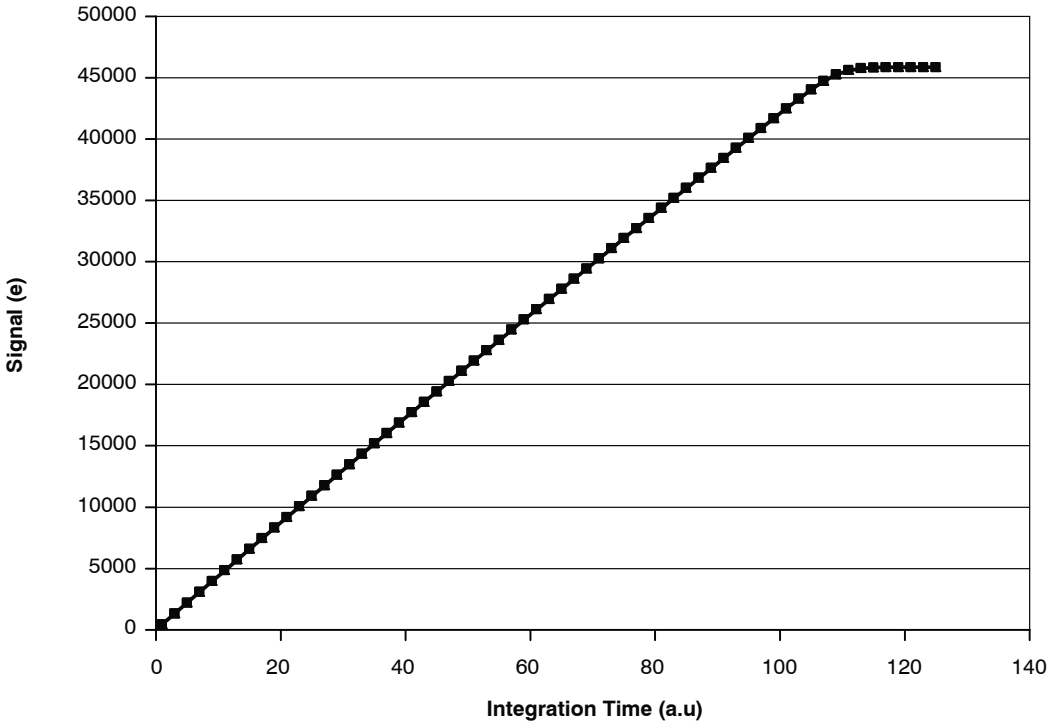


Figure 16. Typical Linearity Performance

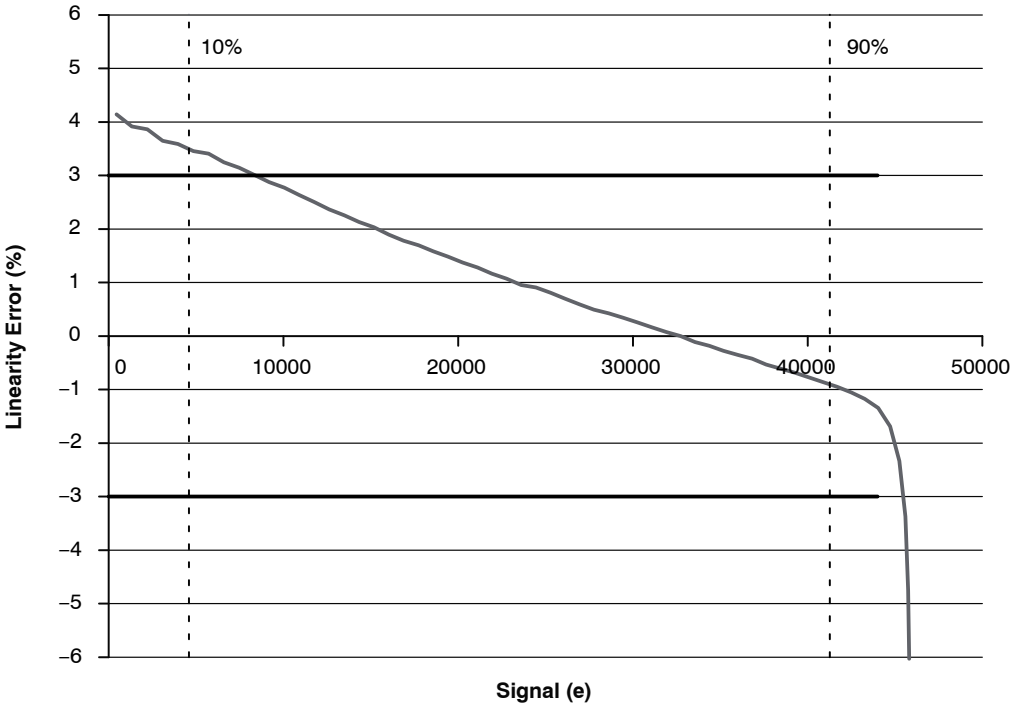


Figure 17. Typical Non-Linearity Plot

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DEFECT DEFINITIONS

Operating Conditions

Bright defect tests performed at T = 25°C
Dark defect tests performed at T = 25°C

Table 6. SPECIFICATIONS

Classification	Points	Clusters	Columns
Class 1	≤ 2,000	≤ 40	0
Class 2	≤ 2,000	≤ 40	≤ 15

Point Defects

A pixel that deviates by more than 9 mV above neighboring pixels under non−illuminated conditions.

−or−

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions.

Cluster Defect

A grouping of not more than 10 adjacent point defects. Cluster defects are separated by no less than 4 good pixels in any direction.

Column Defect

A grouping of more than 10 point defects along a single column

−or−

A column that deviates by more than 1.2 mV above or below neighboring columns under non−illuminated conditions.

−or−

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions.

Column and cluster defects are separated by at least 4 good columns in the x direction. No multiple column defects (double or more) will be permitted.

Saturated Columns

A column that deviates by more than 100 mV above neighboring columns under non−illuminated conditions. No saturated columns are allowed.

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OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	−0.5	+20.0	V	1, 2
Gate Pin Voltages	V_{gate1}	−14.3	+14.5	V	1, 3
Reset Gate Pin Voltages	V_{RG}	−0.5	+14.5	V	1
Overlapping Gate Voltages	$V_{1−2}$	−14.3	+14.5	V	4
Non−Overlapping Gate Voltages	$V_{o−o}$	−14.3	+14.5	V	5
Output Bias Current	I_{out}		−30	mA	6
LOD Diode Voltage	V_{LOD}	−0.5	+13.5	V	1
Operating Temperature	T_{OP}	0	60	°C	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, H2L, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2, H1/H1L to H2, H1L to OG, V1 to H2.
5. Voltage difference between non−overlapping gates. Includes: V1 to H1/H1L.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF (Mean Time to Failure).
7. Noise performance will degrade at higher temperatures.

Power−Up Sequence

The sequence chosen to perform an initial power−up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Reset Drain	RD	11.3	11.5	11.7	V	
Output Amplifier Return	VSS		0.7		V	
Output Amplifier Supply	VDD	14.5	15.0		V	
Substrate	SUB		0		V	
Output Gate	OG	−2.3	−2.5	−2.7	V	
Lateral Drain/Guard	LOD	10.8	11.0	11.2	V	
Video Output Load Current	I_{OUT}		−5	−10	mA	1

1. An output load sink must be applied to each of the four VOUT pins to activate output amplifier – see Figure 4.

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AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
Vertical CCD Clock −Phase 1	V1	Low	−8.8	−9.0	−9.2	V		1, 2, 3
		High	2.3	2.5	2.7	V		
Vertical CCD Clock −Phase 2	V2	Low	−8.8	−9.0	−9.2	V		1, 2, 3
		High	3.3	3.5	3.7	V		
Horizontal CCD Clock − Phase 1	H1	Low	−3.8	−4.0	−4.2	V		1, 2, 3
		High	1.8	2.0	2.2	V		
Horizontal CCD Clock − Phase 2	H2	Low	−3.8	−4.0	−4.2	V		1, 2, 3
		High	1.8	2.0	2.2	V		
Horizontal CCD Clock − Phase 1 (Last)	H1L	Low	−5.8	−6.0	−6.2	V		1, 2, 3
		High	1.8	2.0	2.2	V		
Reset Gate	RG	Low	0.8	1.0	1.2	V		1, 2, 3
		High	7.8	8.0	8.2	V		

1. All pins draw less than 10 A DC current.
2. Capacitance values relative to SUB (substrate).
3. Capacitance values of left and right pins combined where appropriate.

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TIMING

Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			24	MHz	1, 2
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	2			μs	
V1 − V2 Cross−Over	V_{VCR}	0	1	2	V	
H1 − H2 Cross−Over	V_{HCR}	−2	−1	0	V	
H1L Rise − H2 Fall Crossover	V_{H1LCR}		−1		V	
Vccd to Hccd Transfer	T_{vh}	5			μs	
V1, V2 Clock Pulse Width	t_V	8			μs	
Pixel Period (1 Count)	t_e	41.67			ns	2
Line Time	t_{line}	219			μs	
Readout Time	$t_{readout}$	0.81			s	3
Frame Rate	t_{frame}	1.23			fps	
Integration Time	t_{int}					4

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. $t_{readout} = t_{line} * 3695$ lines
4. Integration time is user specified.

Edge Alignment

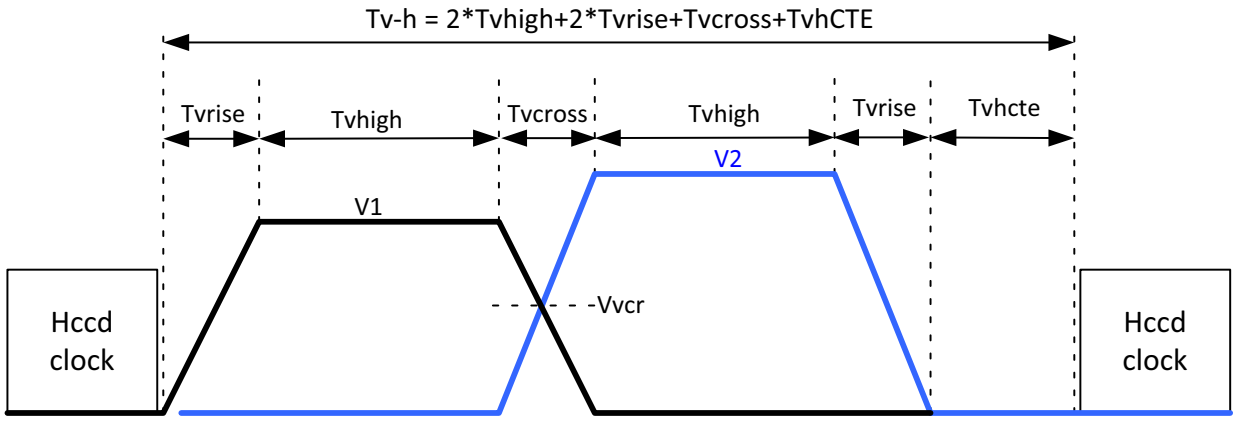


Figure 18. Detail of Vertical Clock Timing

The falling edge of V1 transfers charge between rows. The falling edge of V2 transfers the Vccd charge packet from V2 into Hccd phase H1. To allow for full charge transfer from the Vccd to the Hccd, a delay tv_{hcte} is required between the falling edge of V2 and the start of Hccd clocking.

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Frame Timing

Row annotation: [row# transferred to Hccd] : row assignment.

Row #3695 is the last row (optical injection). Any overclock beyond that sends null values to the Hccd.

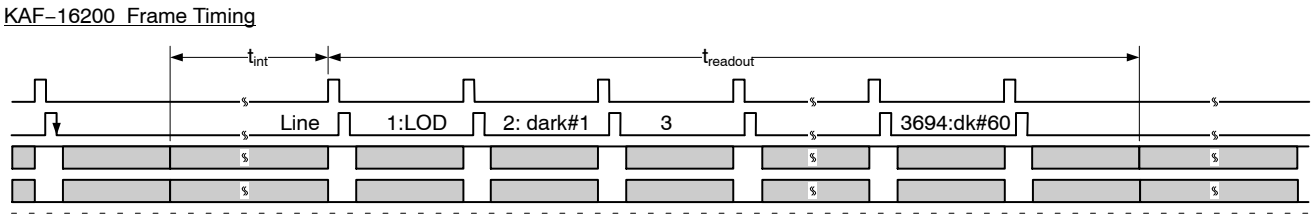
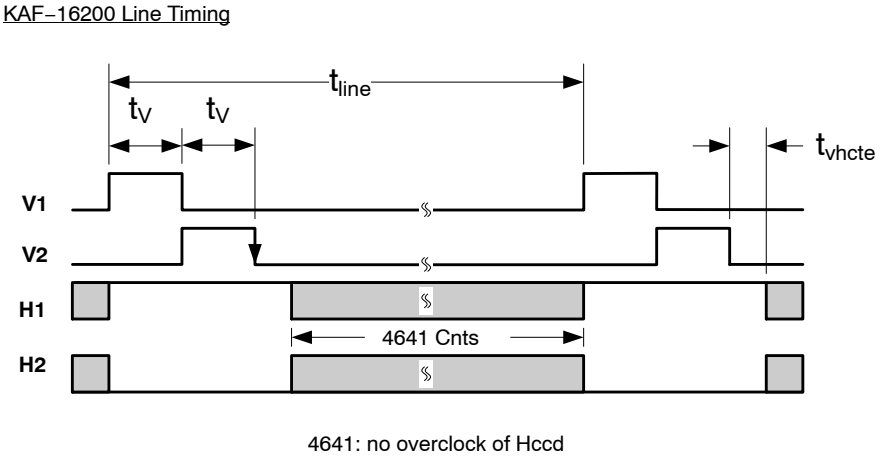


Figure 19. Frame Timing

The integration of dark and photo−signal in the Vccd is continuous, as there is no pixel reset mechanism. "t_{int}" may refer to the time the Vccd clocks are static, and therefore avoid image smear during readout.

Line Timing



4641: no overclock of Hccd

Figure 20. Line Timing

Pixel Timing

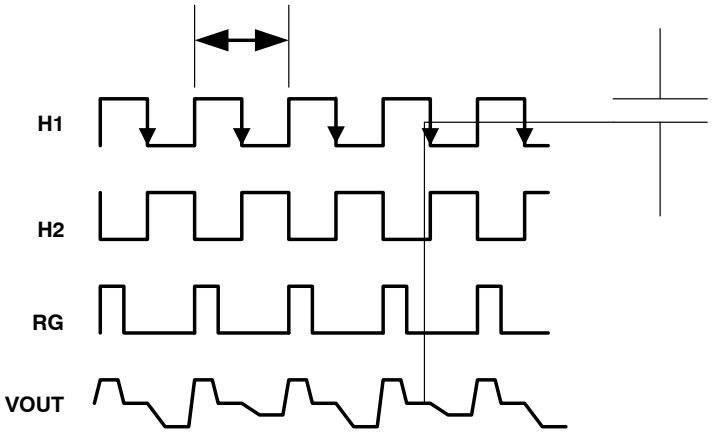


Figure 21. Pixel Timing

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REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

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MECHANICAL INFORMATION

Completed Assembly

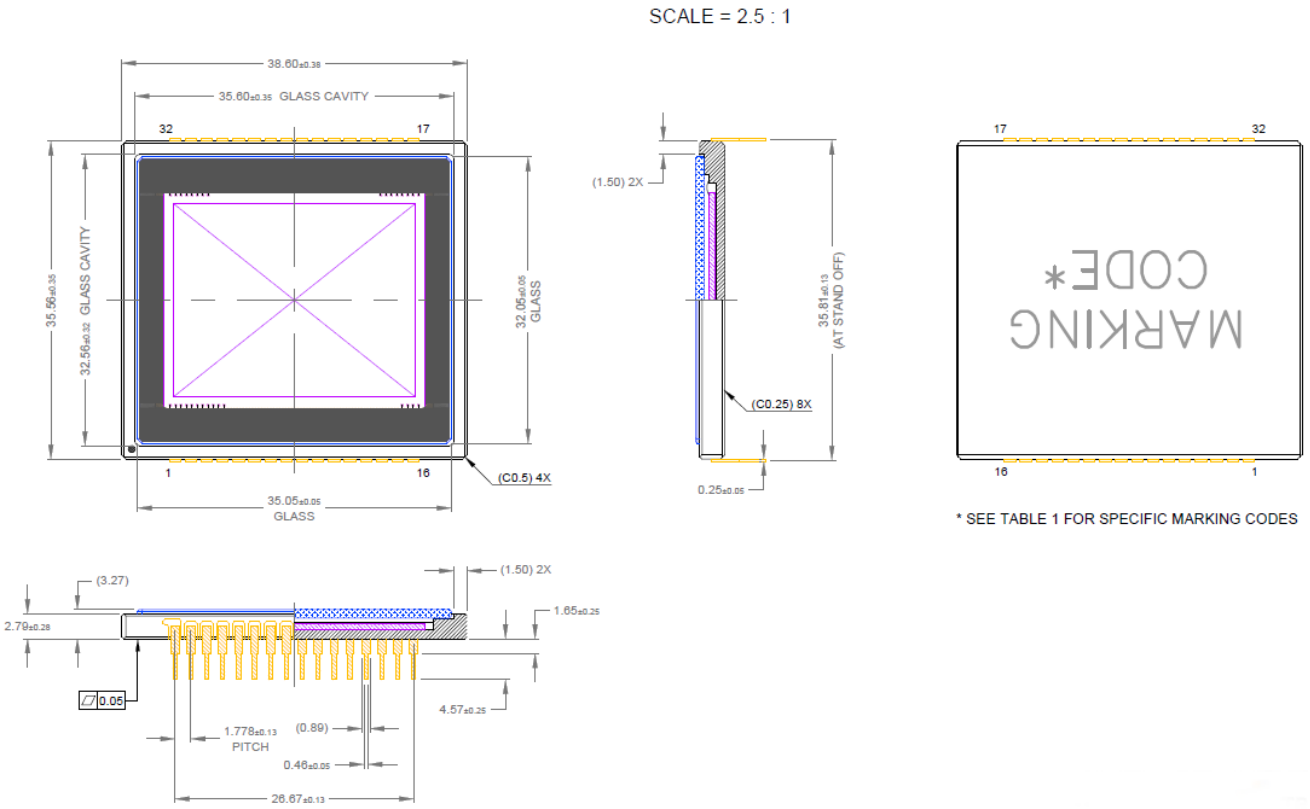


Figure 22. Completed Assembly Drawing

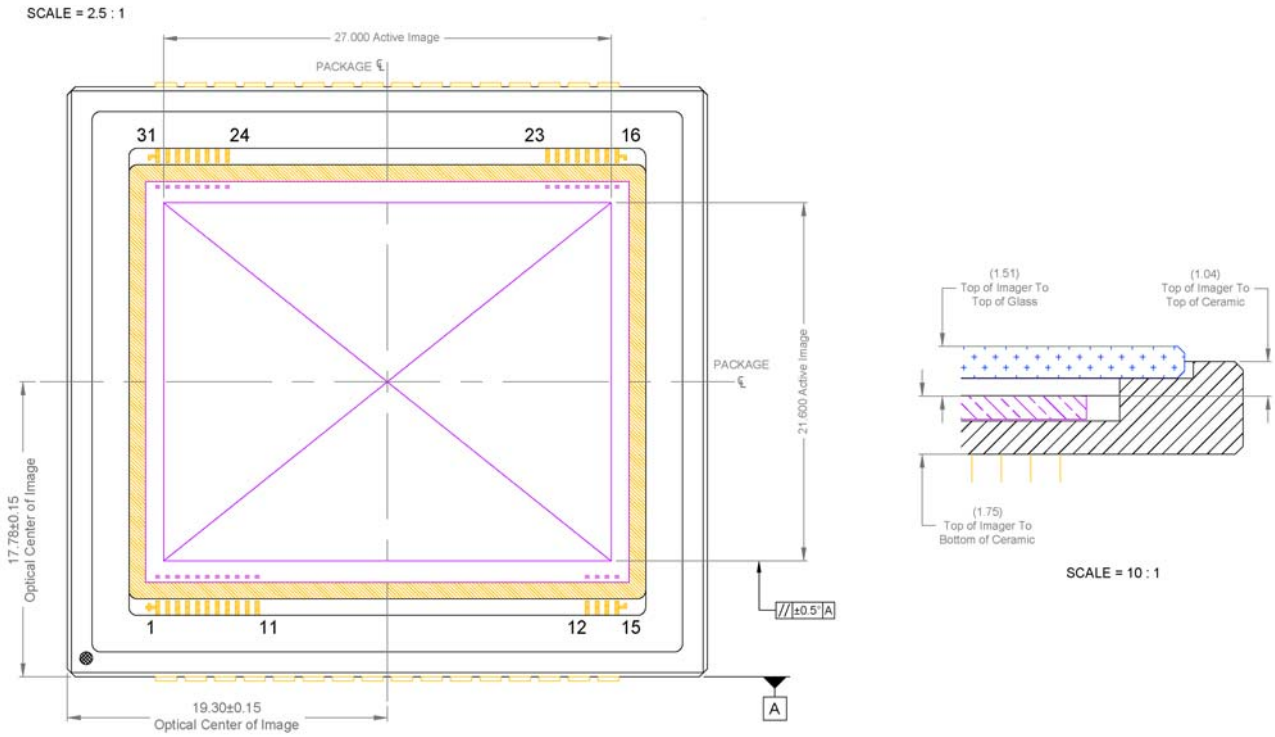


Figure 23. Die Placement

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Cover Glass Specification

1. Scratch and dig: 20 micron max
2. Substrate material: Schott D263T eco @ 1 mm thickness
3. Multilayer anti−reflective coating.

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