



# PSMN2R0-40YLD

N-channel 40 V, 2.1 mΩ, 180 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

25 September 2019

Product data sheet

## 1. General description

180 A, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- 180 A continuous  $I_{D(max)}$  rating
- Avalanche rated, 100% tested at  $I_{AS} = 160$  A
- Strong SOA (linear-mode) rating
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low  $Q_{rr}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low  $V_{SD}$ , low  $Q_{rr}$ , soft recovery and low  $I_{DSS}$  leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- Brushless DC motor control
- Battery protection
- Load-switch and eFuse
- Inrush management, hotswap

## 4. Quick reference data

Table 1. Quick reference data

| Symbol                        | Parameter                        | Conditions                                                                                     | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $V_{DS}$                      | drain-source voltage             | $25\text{ °C} \leq T_J \leq 175\text{ °C}$                                                     | -   | -   | 40  | V    |
| $I_D$                         | drain current                    | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>                      | [1] | -   | 180 | A    |
| $P_{tot}$                     | total power dissipation          | $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>                                               | -   | -   | 166 | W    |
| $T_J$                         | junction temperature             |                                                                                                | -55 | -   | 175 | °C   |
| <b>Static characteristics</b> |                                  |                                                                                                |     |     |     |      |
| $R_{DS(on)}$                  | drain-source on-state resistance | $V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 10</a>  | -   | 1.8 | 2.1 | mΩ   |
|                               |                                  | $V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 10</a> | -   | 2.3 | 2.7 | mΩ   |

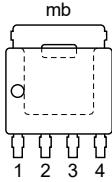
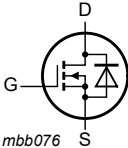
N-channel 40 V, 2.1 mΩ, 180 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

| Symbol                  | Parameter         | Conditions                                                              | Min | Typ | Max | Unit |
|-------------------------|-------------------|-------------------------------------------------------------------------|-----|-----|-----|------|
| Dynamic characteristics |                   |                                                                         |     |     |     |      |
| Q <sub>GD</sub>         | gate-drain charge | I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; | 2.2 | 7.3 | 15  | nC   |
| Q <sub>G(tot)</sub>     | total gate charge | Fig. 12; Fig. 13                                                        | 20  | 30  | 42  | nC   |

[1] 180A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline                                                                                              | Graphic symbol                                                                                |
|-----|--------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| 1   | S      | source                            | <br>LPAK56; Power-SO8 (SOT669) | <br>mbb076 |
| 2   | S      | source                            |                                                                                                                 |                                                                                               |
| 3   | S      | source                            |                                                                                                                 |                                                                                               |
| 4   | G      | gate                              |                                                                                                                 |                                                                                               |
| mb  | D      | mounting base; connected to drain |                                                                                                                 |                                                                                               |

6. Ordering information

Table 3. Ordering information

| Type number   | Package           |                                                            |         |
|---------------|-------------------|------------------------------------------------------------|---------|
|               | Name              | Description                                                | Version |
| PSMN2R0-40YLD | LPAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669  |

7. Marking

Table 4. Marking codes

| Type number   | Marking code |
|---------------|--------------|
| PSMN2R0-40YLD | 2D0L40Y      |

8. Limiting values

Table 5. Limiting values

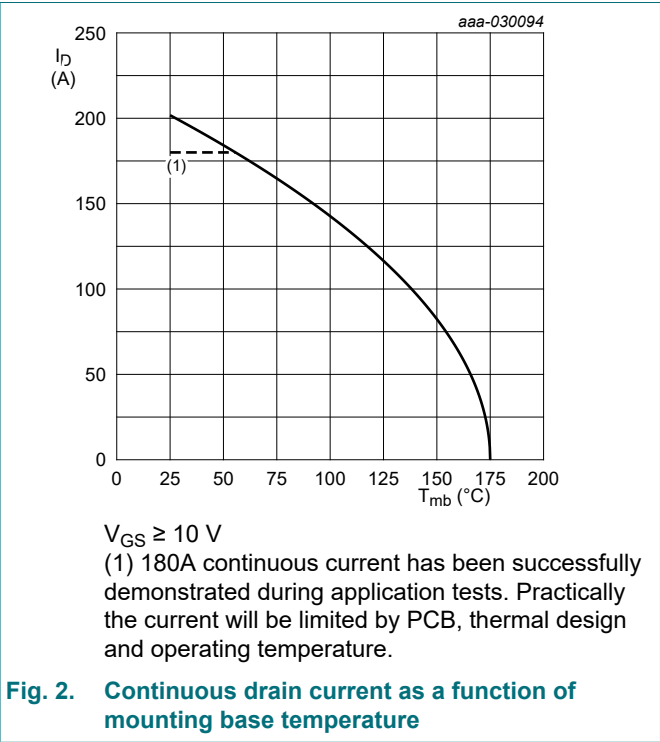
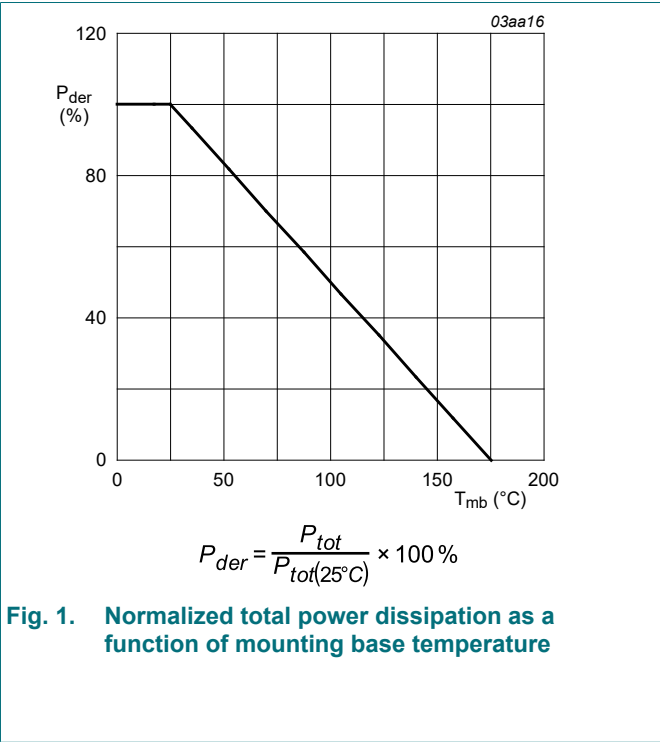
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter                 | Conditions                                                                | Min | Max | Unit |
|------------------|---------------------------|---------------------------------------------------------------------------|-----|-----|------|
| V <sub>DS</sub>  | drain-source voltage      | 25 °C ≤ T <sub>j</sub> ≤ 175 °C                                           | -   | 40  | V    |
| V <sub>DSM</sub> | peak drain-source voltage | t <sub>p</sub> ≤ 20 ns; f ≤ 500 kHz; E <sub>DS(AL)</sub> ≤ 200 nJ; pulsed | -   | 45  | V    |
| V <sub>DGR</sub> | drain-gate voltage        | 25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ                  | -   | 40  | V    |
| V <sub>GS</sub>  | gate-source voltage       |                                                                           | -20 | 20  | V    |
| P <sub>tot</sub> | total power dissipation   | T <sub>mb</sub> = 25 °C; Fig. 1                                           | -   | 166 | W    |
| I <sub>D</sub>   | drain current             | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2                   | [1] | 180 | A    |
|                  |                           | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2                  | -   | 143 | A    |
| I <sub>DM</sub>  | peak drain current        | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3           | -   | 807 | A    |

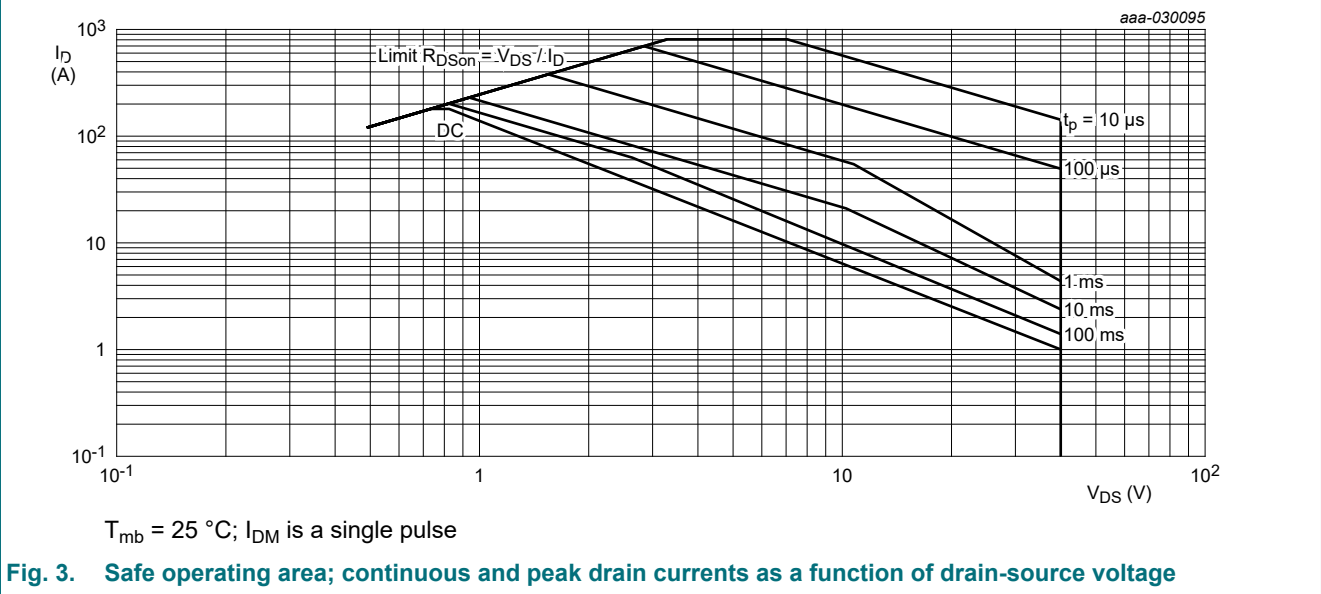
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| Symbol               | Parameter                                    | Conditions                                                                                                                                                         |     | Min | Max | Unit |
|----------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| T <sub>stg</sub>     | storage temperature                          |                                                                                                                                                                    |     | -55 | 175 | °C   |
| T <sub>j</sub>       | junction temperature                         |                                                                                                                                                                    |     | -55 | 175 | °C   |
| T <sub>slid(M)</sub> | peak soldering temperature                   |                                                                                                                                                                    |     | -   | 260 | °C   |
| Source-drain diode   |                                              |                                                                                                                                                                    |     |     |     |      |
| I <sub>S</sub>       | source current                               | T <sub>mb</sub> = 25 °C                                                                                                                                            |     | -   | 166 | A    |
| I <sub>SM</sub>      | peak source current                          | pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C                                                                                                            |     | -   | 807 | A    |
| Avalanche ruggedness |                                              |                                                                                                                                                                    |     |     |     |      |
| E <sub>DS(AL)S</sub> | non-repetitive drain-source avalanche energy | I <sub>D</sub> = 53.5 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 182 μs | [2] | -   | 253 | mJ   |
|                      |                                              | I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 937 μs   | [2] | -   | 609 | mJ   |
| I <sub>AS</sub>      | non-repetitive avalanche current             | V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω                                                              | [2] | -   | 160 | A    |

- [1] 180A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



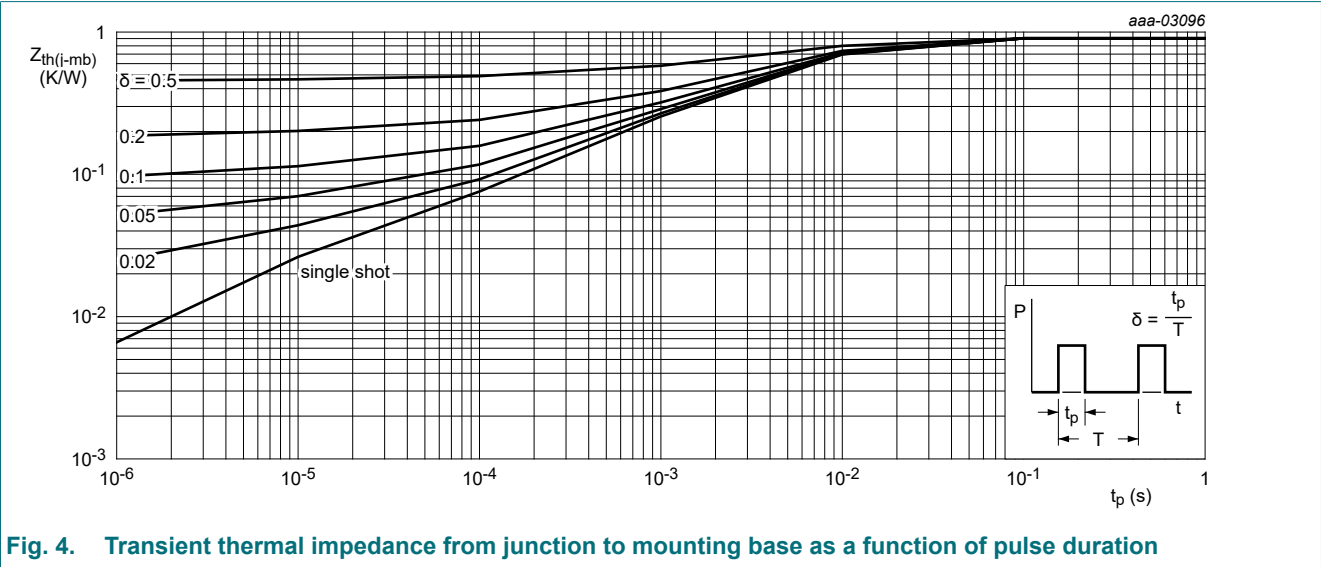
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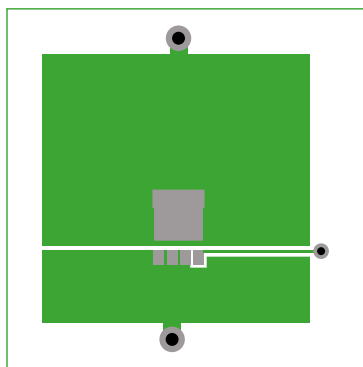
## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter                                         | Conditions | Min | Typ | Max | Unit |
|----------------|---------------------------------------------------|------------|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4     | -   | 0.8 | 0.9 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | Fig. 5     | -   | 42  | -   | K/W  |
|                |                                                   | Fig. 6     | -   | 85  | -   | K/W  |

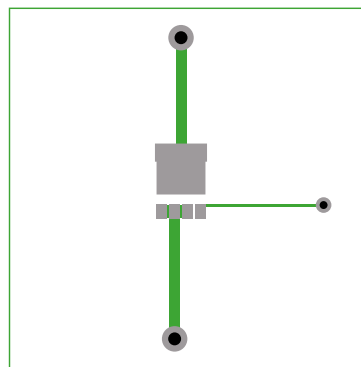


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Copper area 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

**Fig. 5. PCB layout for thermal resistance from junction to ambient**



70 μm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

## 10. Characteristics

**Table 7. Characteristics**

| Symbol                         | Parameter                                                | Conditions                                                     | Min  | Typ   | Max  | Unit |
|--------------------------------|----------------------------------------------------------|----------------------------------------------------------------|------|-------|------|------|
| <b>Static characteristics</b>  |                                                          |                                                                |      |       |      |      |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage                           | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$              | 40   | -     | -    | V    |
|                                |                                                          | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$             | 36   | -     | -    | V    |
| $V_{GS(th)}$                   | gate-source threshold voltage                            | $I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$                | 1.35 | 1.73  | 2.05 | V    |
| $\Delta V_{GS(th)}/\Delta T$   | gate-source threshold voltage variation with temperature | $25^\circ C \leq T_j \leq 150^\circ C$                         | -    | -4.3  | -    | mV/K |
| $I_{DSS}$                      | drain leakage current                                    | $V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25^\circ C$                | -    | 0.007 | 1    | μA   |
|                                |                                                          | $V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125^\circ C$               | -    | 2     | -    | μA   |
| $I_{GSS}$                      | gate leakage current                                     | $V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$                | -    | 2     | 100  | nA   |
|                                |                                                          | $V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$               | -    | 2     | 100  | nA   |
| $R_{DS(on)}$                   | drain-source on-state resistance                         | $V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$ ; Fig. 10        | -    | 1.8   | 2.1  | mΩ   |
|                                |                                                          | $V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C$ ; Fig. 11       | -    | -     | 4.1  | mΩ   |
|                                |                                                          | $V_{GS} = 4.5 V; I_D = 25 A; T_j = 25^\circ C$ ; Fig. 10       | -    | 2.3   | 2.7  | mΩ   |
|                                |                                                          | $V_{GS} = 4.5 V; I_D = 25 A; T_j = 175^\circ C$ ; Fig. 11      | -    | -     | 5.2  | mΩ   |
| $R_G$                          | gate resistance                                          | $f = 1 MHz; T_j = 25^\circ C$                                  | 0.3  | 0.8   | 2    | Ω    |
| <b>Dynamic characteristics</b> |                                                          |                                                                |      |       |      |      |
| $Q_{G(tot)}$                   | total gate charge                                        | $I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V$ ; Fig. 12; Fig. 13 | 20   | 30    | 42   | nC   |
|                                |                                                          | $I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V$ ; Fig. 12; Fig. 13  | 43   | 66    | 92   | nC   |
|                                |                                                          | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$                       | -    | 35    | -    | nC   |

N-channel 40 V, 2.1 mΩ, 180 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

| Symbol                    | Parameter                         | Conditions                                                                                                                                |     | Min  | Typ  | Max  | Unit |
|---------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|------|
| $Q_{GS}$                  | gate-source charge                | $I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ;<br><a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>             |     | 6.6  | 11   | 17   | nC   |
| $Q_{GS(th)}$              | pre-threshold gate-source charge  |                                                                                                                                           |     | 4.1  | 6.9  | 10.4 | nC   |
| $Q_{GS(th-pl)}$           | post-threshold gate-source charge |                                                                                                                                           |     | 2.5  | 4.1  | 6    | nC   |
| $Q_{GD}$                  | gate-drain charge                 |                                                                                                                                           |     | 2.2  | 7.3  | 15   | nC   |
| $V_{GS(pl)}$              | gate-source plateau voltage       | $I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>                                          |     | -    | 2.7  | -    | V    |
| $C_{iss}$                 | input capacitance                 | $V_{DS} = 20\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a>                   |     | 3056 | 4701 | 6581 | pF   |
| $C_{oss}$                 | output capacitance                |                                                                                                                                           |     | 680  | 1047 | 1466 | pF   |
| $C_{rss}$                 | reverse transfer capacitance      |                                                                                                                                           |     | 54   | 181  | 398  | pF   |
| $t_{d(on)}$               | turn-on delay time                | $V_{DS} = 20\text{ V}$ ; $R_L = 0.8\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ;<br>$R_{G(ext)} = 5\text{ }\Omega$                           |     | -    | 26   | -    | ns   |
| $t_r$                     | rise time                         |                                                                                                                                           |     | -    | 29   | -    | ns   |
| $t_{d(off)}$              | turn-off delay time               |                                                                                                                                           |     | -    | 29   | -    | ns   |
| $t_f$                     | fall time                         |                                                                                                                                           |     | -    | 18   | -    | ns   |
| $Q_{oss}$                 | output charge                     | $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $f = 1\text{ MHz}$ ;<br>$T_j = 25\text{ °C}$                                             |     | -    | 33   | -    | nC   |
| <b>Source-drain diode</b> |                                   |                                                                                                                                           |     |      |      |      |      |
| $V_{SD}$                  | source-drain voltage              | $I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 15</a>                                              |     | -    | 0.8  | 1    | V    |
| $t_{rr}$                  | reverse recovery time             | $I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;<br>$V_{DS} = 20\text{ V}$ ; <a href="#">Fig. 16</a> |     | -    | 32   | -    | ns   |
| $Q_r$                     | recovered charge                  |                                                                                                                                           | [1] | -    | 27   | -    | nC   |
| $t_a$                     | reverse recovery rise time        |                                                                                                                                           |     | -    | 17   | -    | ns   |
| $t_b$                     | reverse recovery fall time        |                                                                                                                                           |     | -    | 15   | -    | ns   |

[1] includes capacitive recovery

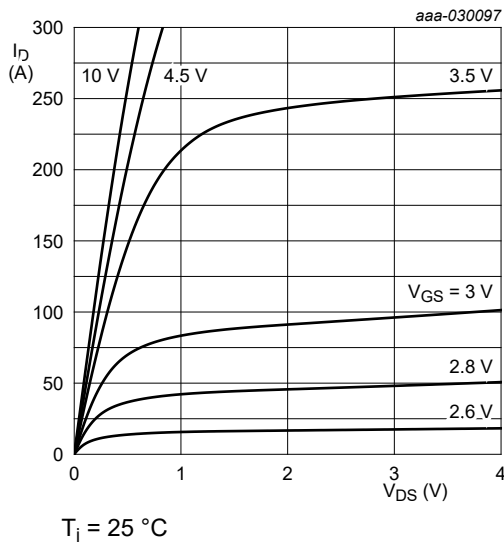


**Fig. 7.** Output characteristics; drain current as a function of drain-source voltage; typical values

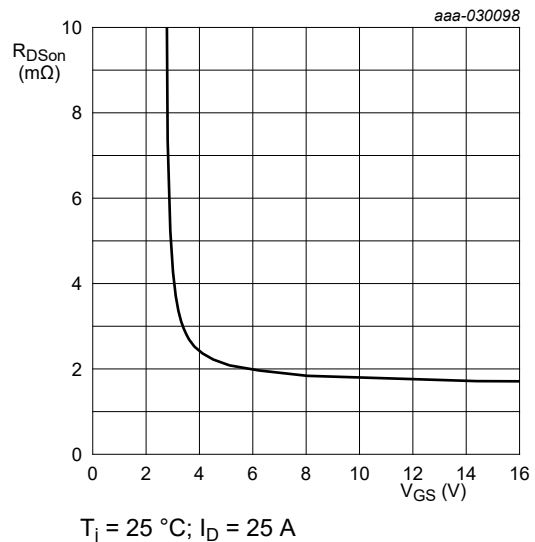


**Fig. 8.** Drain-source on-state resistance as a function of gate-source voltage; typical values

N-channel 40 V, 2.1 mΩ, 180 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

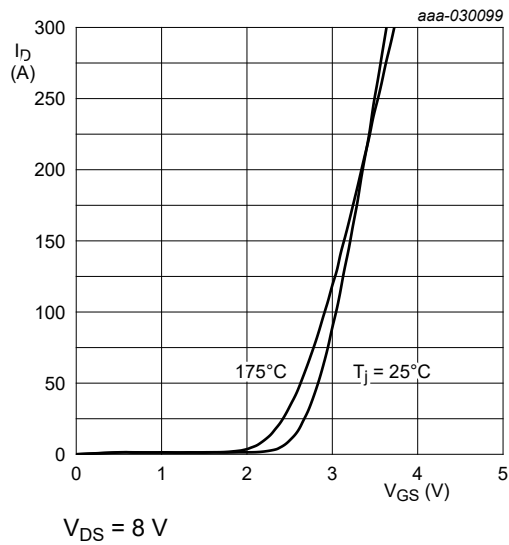


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

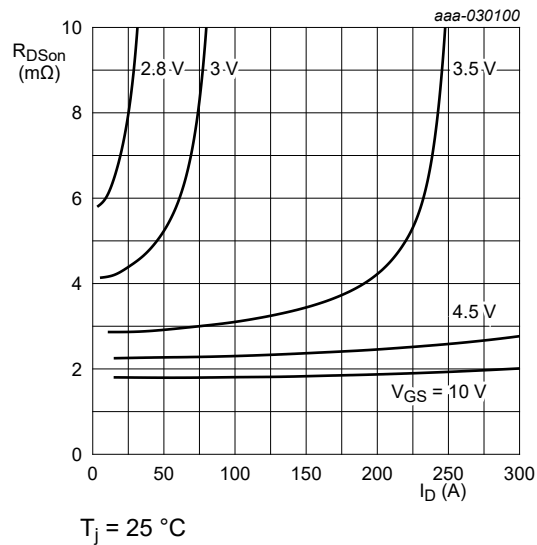


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

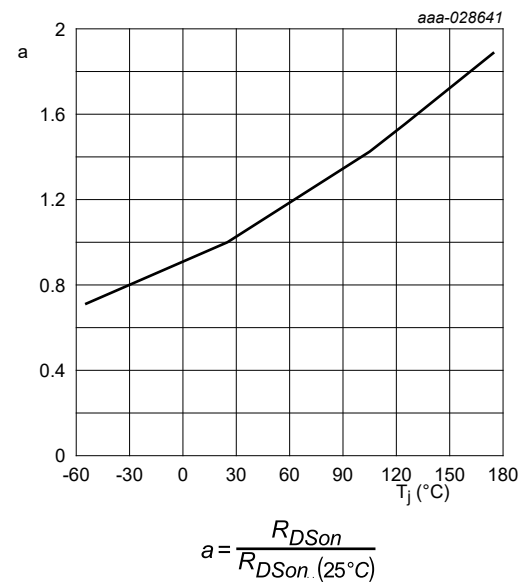


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

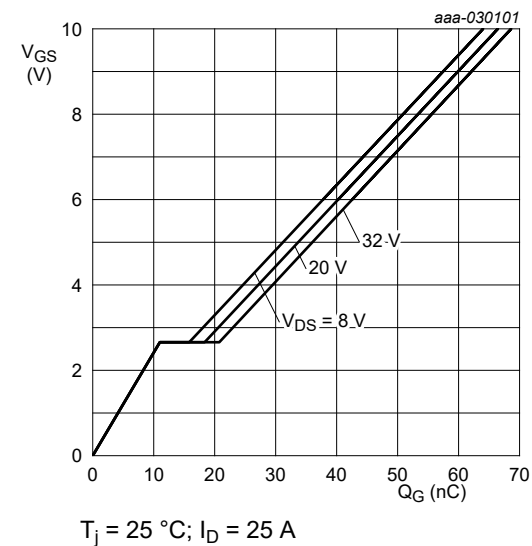
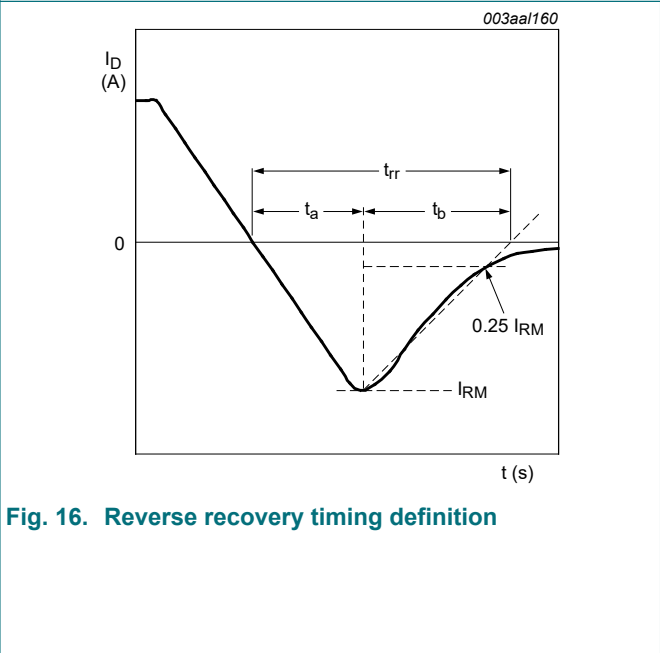
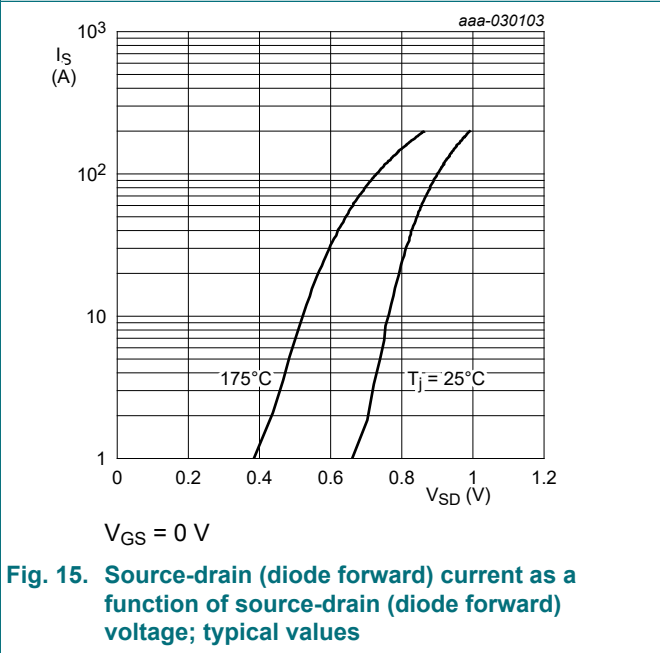
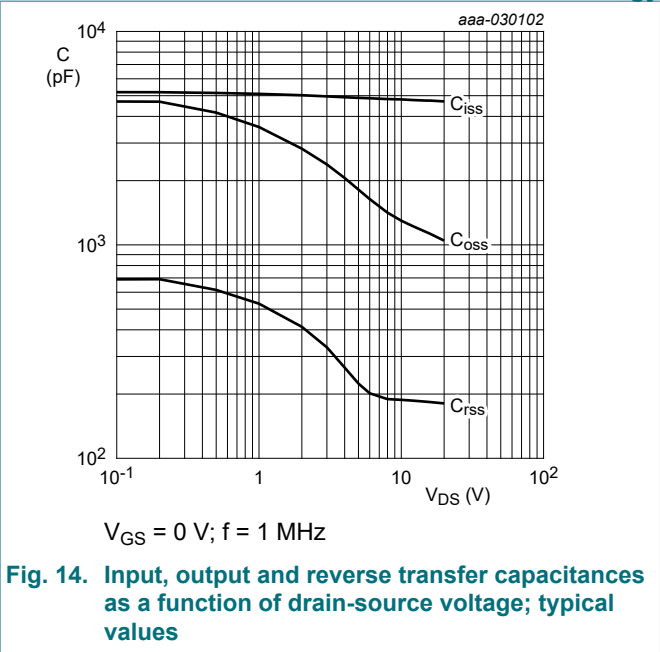
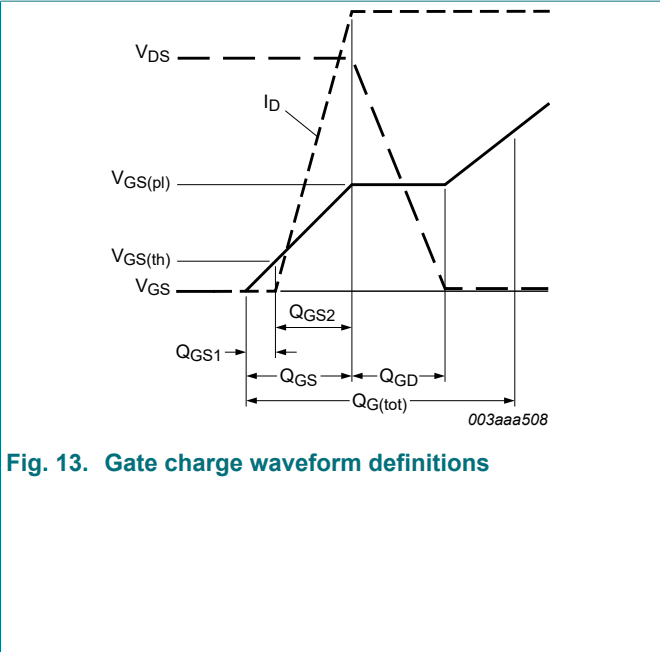


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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11. Package outline

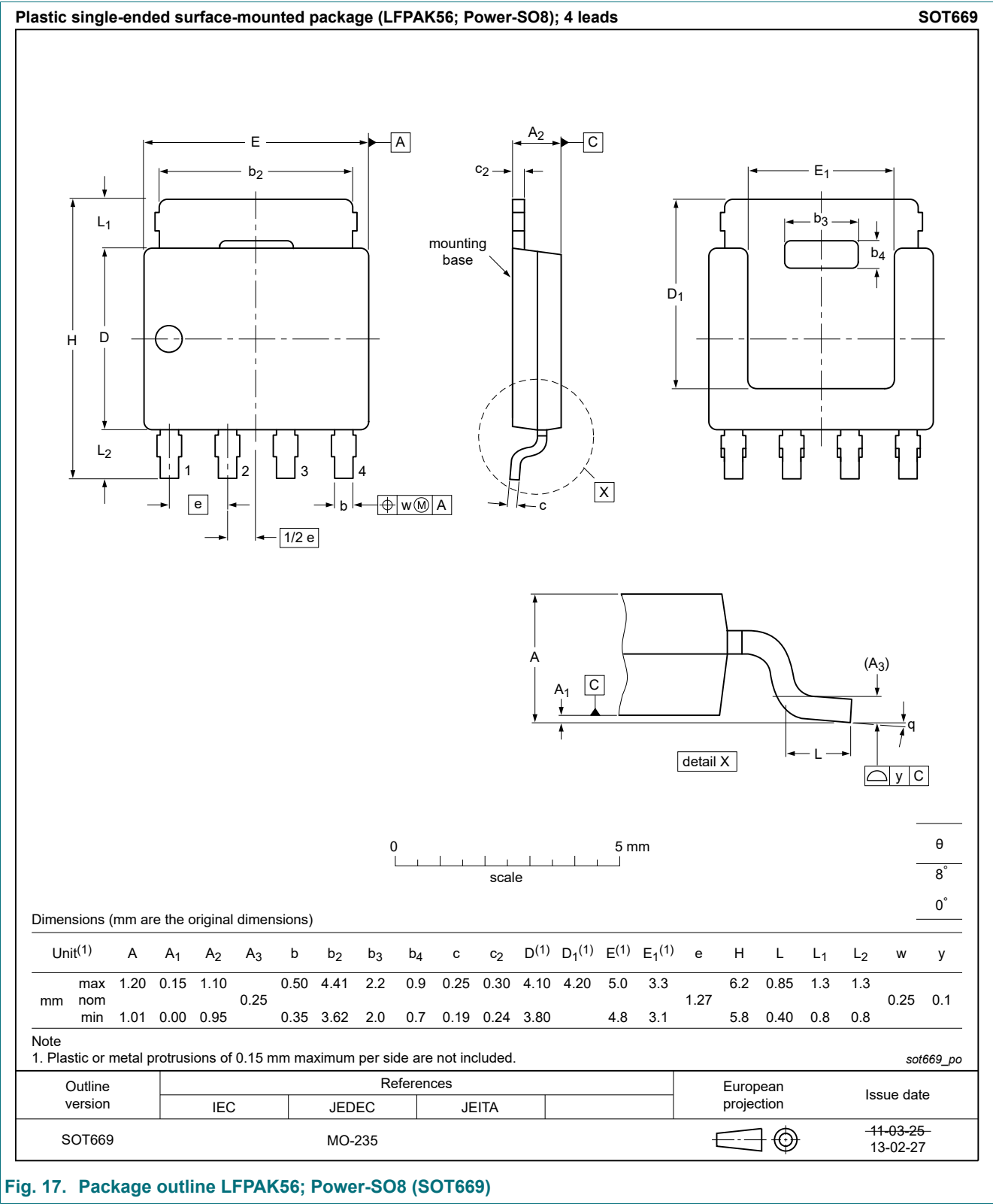
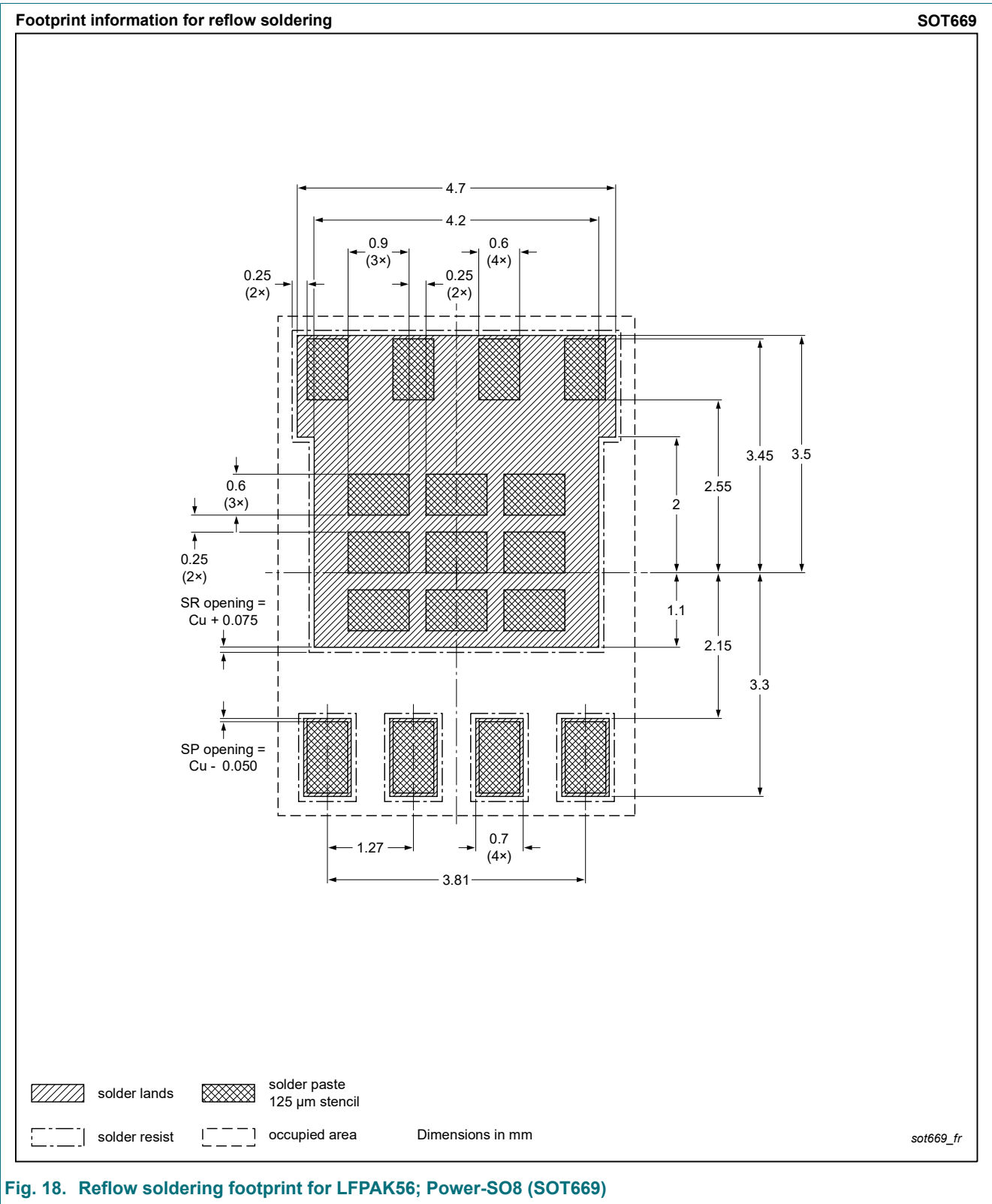


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering



Wave soldering footprint information for LPAK56 package

SOT669

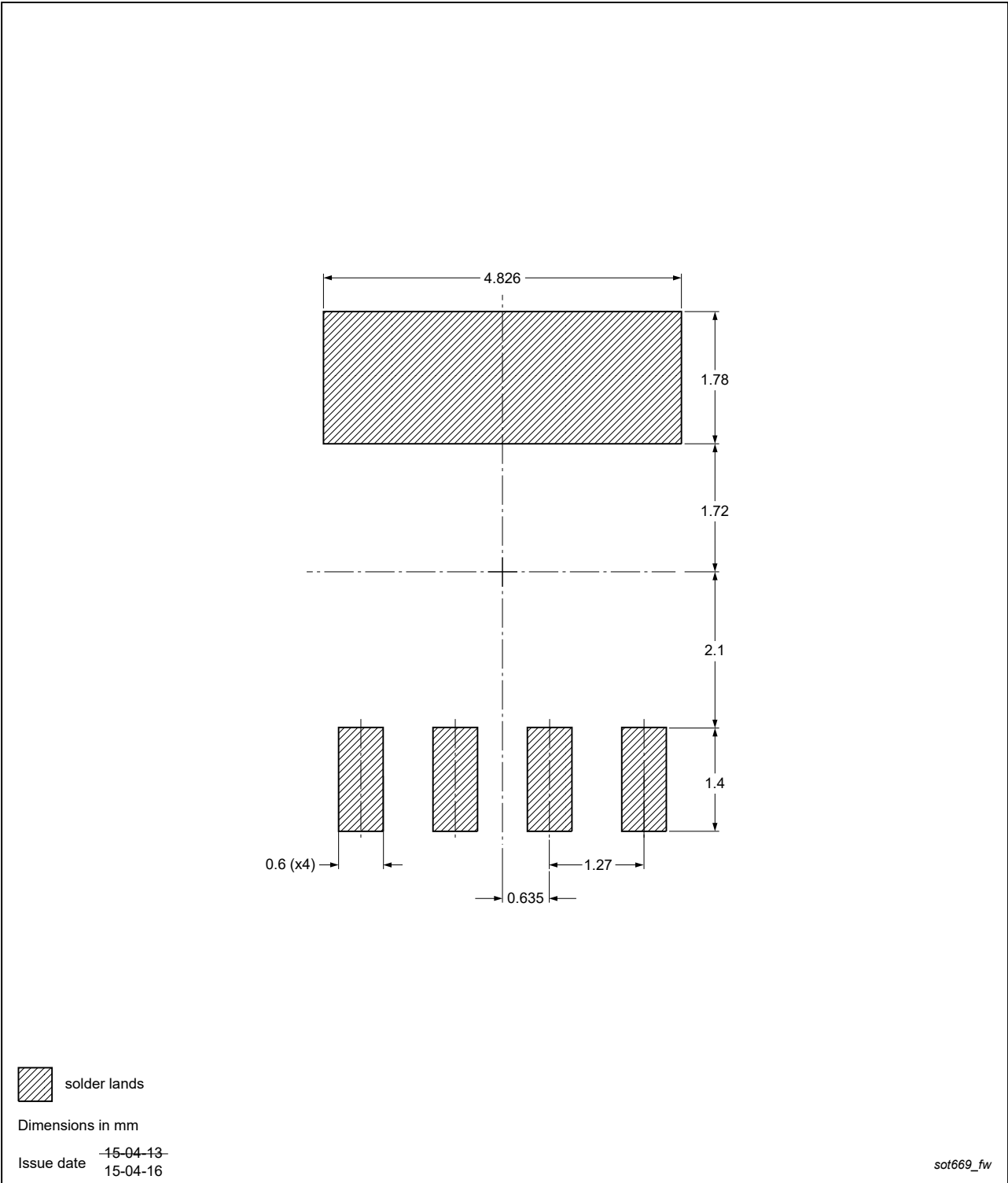


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

## N-channel 40 V, 2.1 mΩ, 180 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

### 13. Legal information

#### Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

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Date of release: 25 September 2019