

REVISIONS																			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED																
A	Added Arrhenius equation for unbiased bake under margin test method A, back end margin test step C. Corrected military part numbers for device types 01 and 02. Technical changes made to 1.2.2, table I, figure 1, figure 2, figure 4, figure 5, 4.3.1, and table II. Added vendor CAGE 34649 for device type 05. Editorial changes throughout.	89-01-19	M. A. Frye																
B	Add device type 08 for vendor CAGE number 66579. Add vendor CAGE number 34335 to the drawing as a source of supply for the 08 device with changes to table I. Deleted programming cycle timing waveform and table III from drawing. Also deleted ESDS from drawing. Editorial changes throughout.	89-10-30	M. A. Frye																
C	Deleted vendor CAGE number 34335 as a source of supply for device type 08. Added vendor CAGE number 34335 as a source of supply for device types 01 through 07. Deleted figure 5. Editorial changes throughout.	90-02-26	M. A. Frye																
D	Changes in accordance with NOR 5962-R079-95.	95-02-15	M. A. Frye																
E	Added provisions for QD certification. Added CAGE 0C7V7 to drawing as a source of supply for device type 07. Updated boilerplate. - glg	99-12-03	Raymond Monnin																
F	Boilerplate update, part of 5-year review. ksr	06-09-29	Raymond Monnin																
G	Corrected footnote 1/ on section 1.2.2 package style heading to include all packages. Corrected test method number in 4.3.2 b (1). ksr	09-03-30	Robert M. Heber																
H	Update drawing to meet current MIL-PRF-38535 requirements. - glg	17-01-11	Charles Saffle																
J	Update to meet current MIL-PRF-38535 requirements. - llb	24-03-05	James Eschmeyer																
																			

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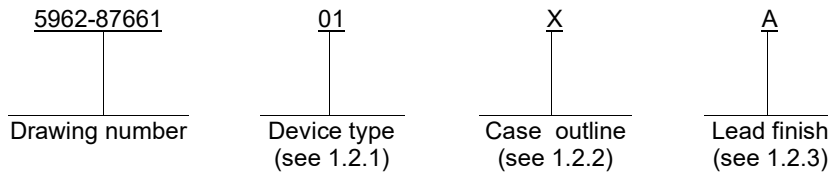
PMIC N/A	PREPARED BY Rick C. Officer CHECKED BY D. A. DiCenzo	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	APPROVED BY Robert P. Evans	
	DRAWING APPROVAL DATE 87-10-23	
	REVISION LEVEL J	

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 16K X 8-BIT ULTRA VIOLET ERASABLE PROGRAMMABLE READ ONLY MEMORY (UVEPROM), MONOLITHIC SILICON		
SIZE A	CAGE CODE 67268	5962-87661
SHEET 1 OF 11		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	27C128	16K x 8-bit UVEPROM	90 ns
02	27C128	16K x 8-bit UVEPROM	120 ns
03	27C128	16K x 8-bit UVEPROM	150 ns
04	27C128	16K x 8-bit UVEPROM	170 ns
05	27C128	16K x 8-bit UVEPROM	200 ns
06	27C128	16K x 8-bit UVEPROM	250 ns
07	27C128	16K x 8-bit UVEPROM	300 ns
08	27C128	16K x 8-bit UVEPROM	70 ns

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	CQCC1-N32	32	rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC}) 2/	-0.6 V dc to 6.25 V dc
Supply voltage range (V_{PP}) 2/	-0.6 V dc to 14.0 V dc
All input voltage range except A_9 2/	-0.6 V dc to 6.25 V dc
Input voltage range (A_9) 2/	-0.6 V dc to 13.5 V dc
Output voltage range 2/	-0.6 V dc to $V_{CC} + 1.0$ V dc
Storage temperature range	-65°C to +150°C
Power dissipation	300 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 3/
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 4/	4.5 V dc to 5.5 V dc
Supply voltage range (V_{PP}) 5/	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.0 V dc to 6.5 V dc (TTL)
High level input voltage range (V_{IH})	$V_{CC} - 0.2$ V dc to $V_{CC} + 0.2$ V dc (CMOS)
Low level input voltage range (V_{IL})	-0.1 V dc to 0.8 V dc (TTL)
Low level input voltage range (V_{IL})	GND -0.2 to GND +0.2 V dc (CMOS)
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Under absolute maximum ratings, voltages are with respect to GND.

3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

4/ V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP} . The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

5/ V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (± 0.5 V).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's QM plan, the "QD" certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be specified by the manufacturer prior to delivery.

3.6.1 Erase of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified program or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific but will guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	I _{OH} = -400 μA	1, 2, 3	All	2.4		V
Low level output voltage	V _{OL}	I _{OL} = 2.1 mA	1, 2, 3	All		0.45	V
Input current (leakage)	I _I	V _I = 0 V to 5.5 V	1, 2, 3	All		±10	μA
Output current (leakage)	I _O	V _O = 0 V to V _{CC}	1, 2, 3	All		±10	μA
V _{PP} supply current	I _{PP1}	V _{PP} = V _{CC} = 5.5 V	1, 2, 3	All		100	μA
V _{PP} supply current (during program pulse) 1/	I _{PP2}	V _{PP} = 13 V	1	01 - 07		50	mA
				08		60	
Operating supply current (active)	I _{CC1}	V _{CC} = 5.5 V, $\overline{CE} = V_{IL}$, f = 1/t _{AVQV} , 01-08 = 0 mA	1, 2, 3	01		70	mA
				02		60	
				03 – 07		25	
				08		85	
Standby power supply current (TTL)	I _{CC2}	V _{CC} = 5.5 V, $\overline{CE} = 2.0$ V, f = 0	1, 2, 3	01 – 07		3.0	mA
				08		200	
Standby power supply current (CMOS)	I _{CC3}	V _{CC} = 5.5 V, $\overline{CE} = V_{CC}$, f = 0	1, 2, 3	01 – 07		300	μA
				08		500	
Input capacitance	C _{IN}	V _I = 0 V, f = 1 MHz, see 4.3.1c	4	All		10	pF
Output capacitance	C _{OUT}	V _O = 0 V, f = 1 MHz, see 4.3.1c	4	All		14	pF
Functional tests		see 4.3.1e	7, 8A, 8B				
Address access time 2/	t _{AVQV}	See figures 3 and 4	9, 10, 11	01		90	ns
				02		120	
				03		150	
				04		170	
				05		200	
				06		250	
				07		300	
				08		70	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable access time <u>2/</u>	t _{ELQV}	See figures 3 and 4	9, 10, 11	01		90	ns
				02		120	
				03		150	
				04		170	
				05		200	
				06		250	
				07		300	
				08		70	
Output enable access time <u>2/</u>	t _{OLQV}	See figures 3 and 4	9, 10, 11	01, 02		50	ns
				03, 04		70	
				05		75	
				06		100	
				07		120	
				08		25	
CE or OE disable to output in high Z <u>1/</u>	t _{EHQZ} , t _{OHQZ}	See figures 3 and 4	9, 10, 11	01 – 04		50	ns
				05, 06		60	
				07		105	
				08		25	
CE or OE enable to output valid <u>1/</u>	t _{EHQV} , t _{OHQV}	See figures 3 and 4	9, 10, 11	All	0		ns

1/ May not be tested, but shall be guaranteed to the limits specified in table I.

2/ For all switching characteristics and timing measurements, inputs pulse levels are 0.40 V and 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.

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Device types	ALL	
Case Outlines	X	Y
Terminal Number	Terminal Symbol	
1	V _{PP}	NC
2	A ₁₂	V _{PP}
3	A ₇	A ₁₂
4	A ₆	A ₇
5	A ₅	A ₆
6	A ₄	A ₅
7	A ₃	A ₄
8	A ₂	A ₃
9	A ₁	A ₂
10	A ₀	A ₁
11	O ₁	A ₀
12	O ₂	NC
13	O ₃	O ₁
14	GND	O ₂
15	O ₄	O ₃
16	O ₅	GND
17	O ₆	NC
18	O ₇	O ₄
19	O ₈	O ₅
20	$\overline{CE}$	O ₆
21	A ₁₀	O ₇
22	$\overline{OE}$	O ₈
23	A ₁₁	$\overline{CE}$
24	A ₉	A ₁₀
25	A ₈	$\overline{OE}$
26	A ₁₃	NC
27	PGM	A ₁₁
28	V _{CC}	A ₉
29	---	A ₈
30	---	A ₁₃
31	---	PGM
32	---	V _{CC}

NC = no connection

FIGURE 1. Terminal connections.

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Mode	Function pins (see note 1)							
	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	A_9	A_0	$O_1 - O_8$
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	D_{OUT}
Outside disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	X	X	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	X	X	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	X	X	High-Z
Signature mode (see notes 2, 3, and 4)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_H	V_{IL}	MFG Code
						V_H	V_{IH}	Device code

NOTES:

1. X can be V_{IL} or V_{IH} .
2. $V_H = 12\text{ V} \pm 0.5\text{ V}$.
3. All other address must be held at V_{IL} .
4. See 6.6.

FIGURE 2. Truth table.

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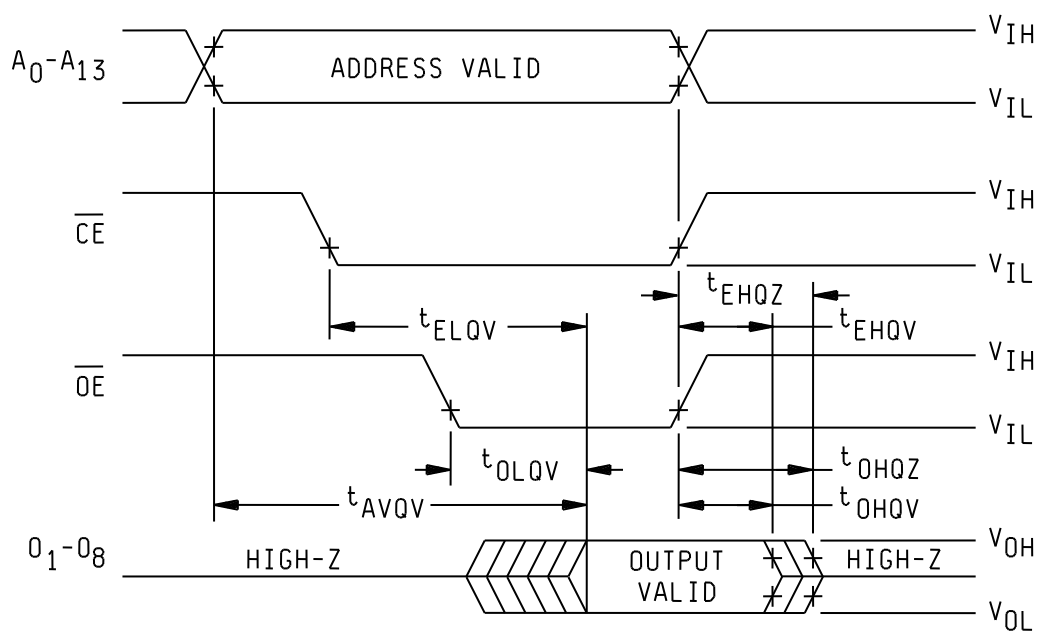


FIGURE 3. Read cycle timing waveform.

PARAMETER MEASUREMENT INFORMATION

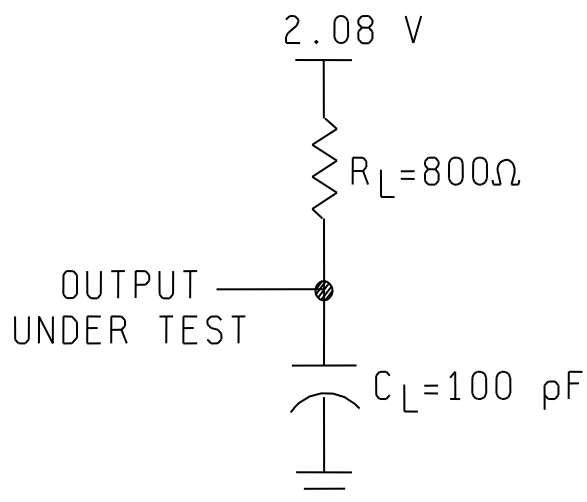


FIGURE 4. Output load circuit.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883 and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.
- d. All devices selected for testing shall have a checkerboard pattern or equivalent. After completion of all testing, the devices shall be verified and erased (except devices submitted for groups C and D testing).
- e. Subgroups 7, 8A, and 8B shall include verification of the truth table.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10 or 1, 2, 3

1/ * Indicates PDA applies to subgroups 1.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** See 4.3.1c.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- c. All devices selected for testing shall be programmed with a checkerboard pattern, then verified, and erased.

4.4 Erasing procedures. The recommended erasing procedure shall be as specified by the device manufacturer and shall be made available upon request.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-03-05

Approved sources of supply for SMD 5962-87661 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8766101XA	0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-90 AM27C128-90/BXA QP27C128-90/XA WS27C128F-90DMB
5962-8766101YA	0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-90 AM27C128-90/BUA QP27C128-90/YA WS27C128F-90CMB
5962-8766102XA	0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-120 AM27C128-120/BXA QP27C128-120/XA WS27C128L-12DMB
5962-8766102YA	0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-120 AM27C128-120/BUA QP27C128-120/YA WS27C128L-12CMB
5962-8766103XA	<u>3/</u> 0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-15BXA 27C128-150 AM27C128-150/BXA QP27C128-150/XA WS27C128L-15DMB
5962-8766103YA	<u>3/</u> <u>3/</u> 0C7V7 0C7V7 <u>3/</u>	27C128-15BUC AM27C128-150/BUA 27C128-150 QP27C128-120/YA WS27C128L-15CMB
5962-8766104XA	<u>3/</u> 0C7V7 <u>3/</u> 0C7V7 <u>3/</u>	27C128-17BXA 27C128-170 AM27C128-170/BXA QP27C128-170/XA WS27C128L-17DMB
5962-8766104YA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u>	27C128-170 27C128-17BUC AM27C128-170/BUA QP27C128-170/YA WS27C128L-17CMB
5962-8766105XA	0C7V7 <u>3/</u> <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u> <u>3/</u>	27C128-200 27C128-20BXA AM27C128-200/BXA MD27C128-20 QP27C128-200/XA SMJ27C128-20JM WS27C128L-20DMB

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 24-03-05

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8766105YA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u>	27C128-200 27C128-20BUC AM27C128-200/BUA QP27C128-200/YA WS27C128L-20CMB
5962-8766106XA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u> <u>3/</u>	27C128-250 27C128-25BXA AM27C128-250/BXA QP27C128-250/XA SMJ27C128-25JM WS27C128L-25DMB
5962-8766106YA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u>	27C128-250 27C128-25BUC AM27C128-250/BUA QP27C128-250/YA WS27C128L-25CMB
5962-8766107XA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u> <u>3/</u>	27C128-300/BXA 27C128-30BXA AM27C128-300/BXA QP27C128-300/XA SMJ27C128-30JM WS27C128L-30DMB
5962-8766107YA	0C7V7 <u>3/</u> <u>3/</u> 0C7V7 <u>3/</u>	27C128-300 27C128-30BUC AM27C128-300/BUA QP27C128-300/YA WS27C128L-30CMB
5962-8766108XA	0C7V7 0C7V7 0C7V7	27C128-70 QP27C128-70/XA WS57C128FB-70DMB
5962-8766108YA	0C7V7 0C7V7 0C7V7	27C128-70 QP27C128-70/YA WS57C128FB-70CMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>	<u>Manufacturing code</u>	<u>Device code</u>
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035	01H	16H

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