MOSFET – Power, Single N-Channel, TOLL

80 V, 1.05 mΩ, 351 A

NVBLS1D1N08H

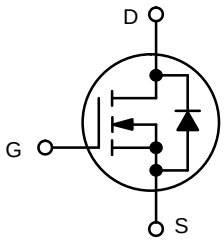
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	1.05 mΩ @ 10 V	351 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- Lowers Switching Noise/EMI
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation



N−CHANNEL MOSFET

TOLL
CASE 100CU

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	80	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25 °C	I_D	351	A
		T_C = 100 °C		248	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25 °C	P_D	311	W
		T_C = 100 °C		156	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25 °C	I_D	41	A
		T_A = 100 °C		29	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25 °C	P_D	4.2	W
		T_A = 100 °C		2.1	
Pulsed Drain Current	T_A = 25°C, t_p = 10 µs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	259	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 31.9 A)			E_{AS}	1580	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case − Steady State	$R_{\theta JC}$	0.48	°C/W
Junction-to-Ambient − Steady State (Note 2)	$R_{\theta JA}$	35.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM

NVBLS1D1N08H = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				57		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25 °C			10	μA
			T_J = 125 °C			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 650 μA		2.0	2.9	4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.7		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.92	1.05	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5 V, I_D = 50 A			213		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 40 V			11200		pF
Output Capacitance	C_{OSS}				1600		
Reverse Transfer Capacitance	C_{RSS}				49		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 64 V; I_D = 50 A			166		nC
Threshold Gate Charge	$Q_{G(TH)}$				29		
Gate-to-Source Charge	Q_{GS}				44		
Gate-to-Drain Charge	Q_{GD}				35		
Plateau Voltage	V_{GP}				4		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 64 V, I_D = 50 A, R_G = 6 Ω			45		ns
Rise Time	t_r				43		
Turn-Off Delay Time	$t_{d(OFF)}$				141		
Fall Time	t_f				43		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25 °C		0.76	1.2	V
			T_J = 125 °C		0.6		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			92		ns
Reverse Recovery Charge	Q_{RR}				234		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

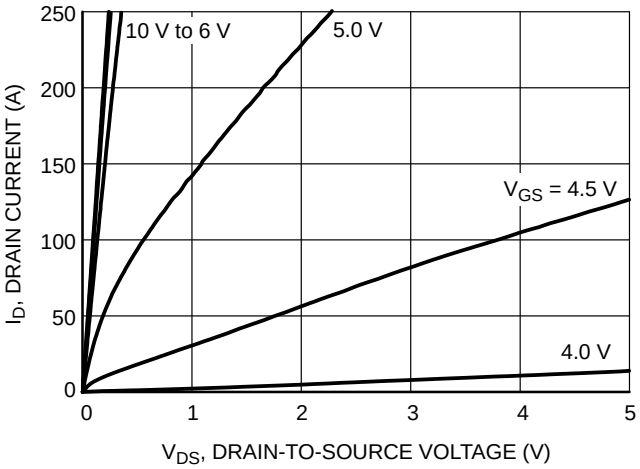

Figure 1. On-Region Characteristics

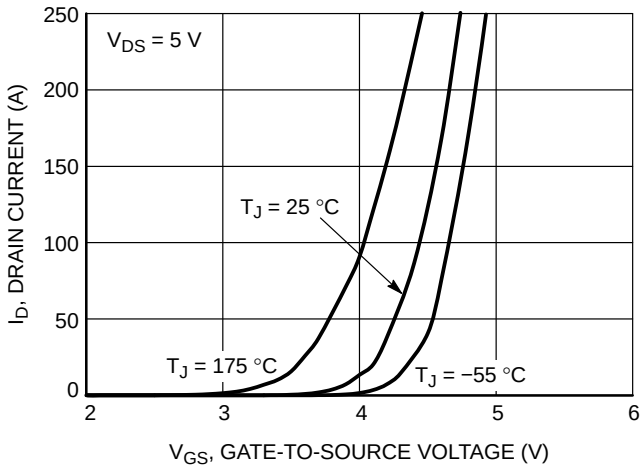

Figure 2. Transfer Characteristics

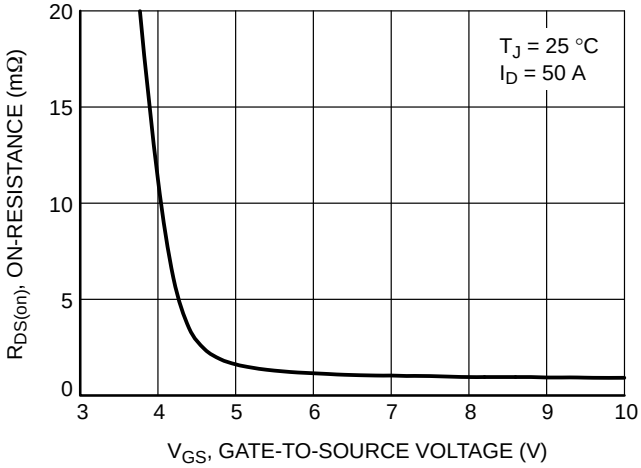

Figure 3. On-Resistance vs. Gate-to-Source Voltage

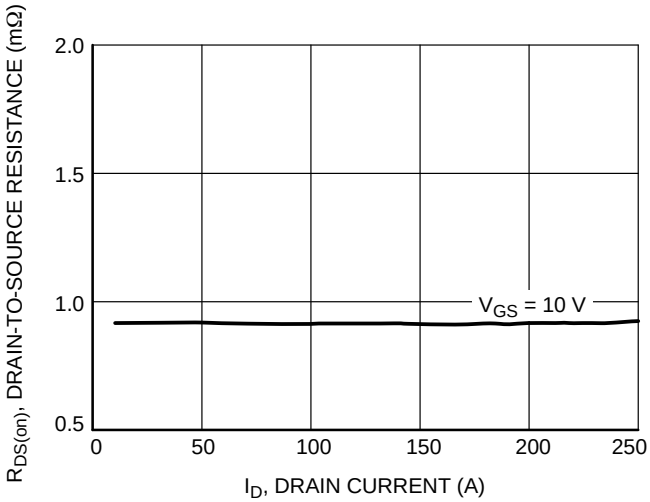

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

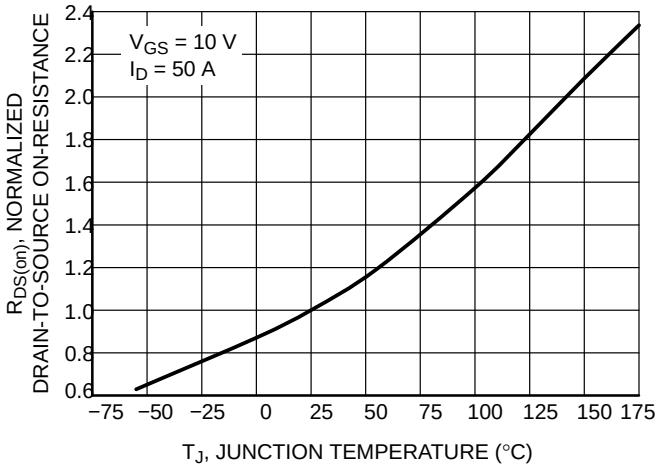

Figure 5. On-Resistance Variation with Temperature

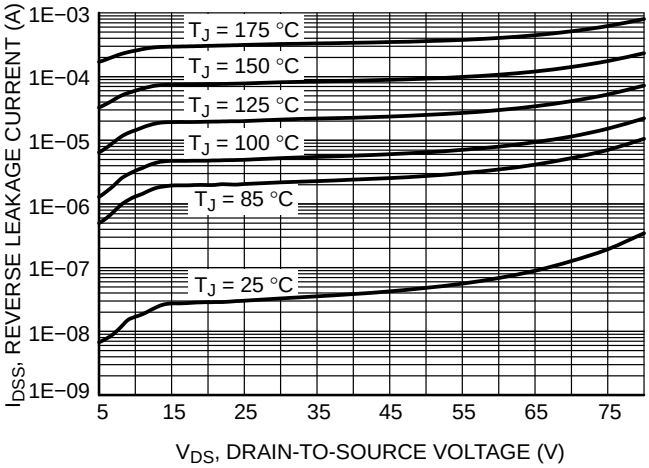

Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

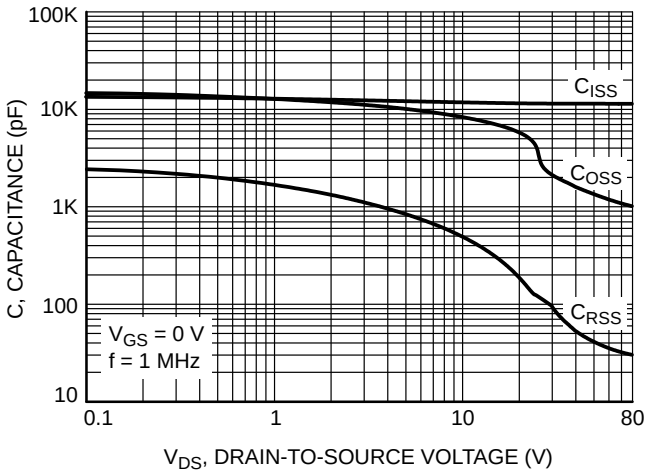

Figure 7. Capacitance Variation

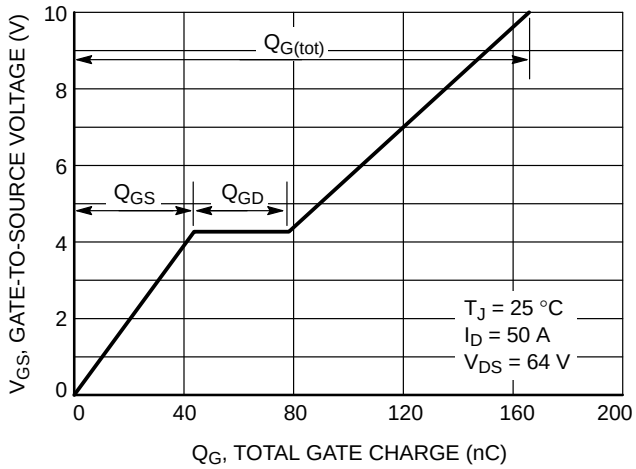

Figure 8. Gate-to-Source Voltage vs. Total Charge

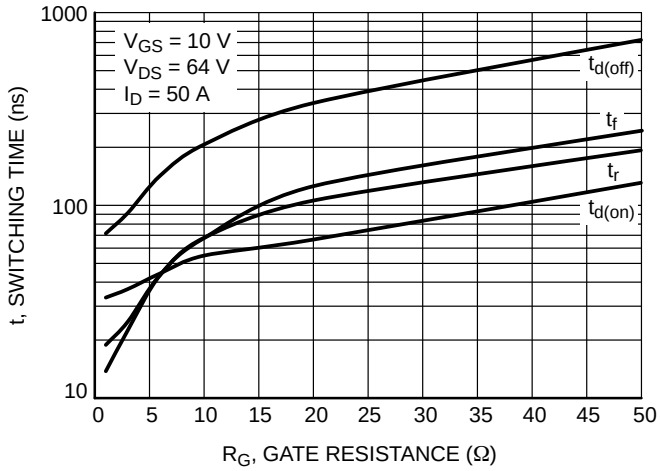

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

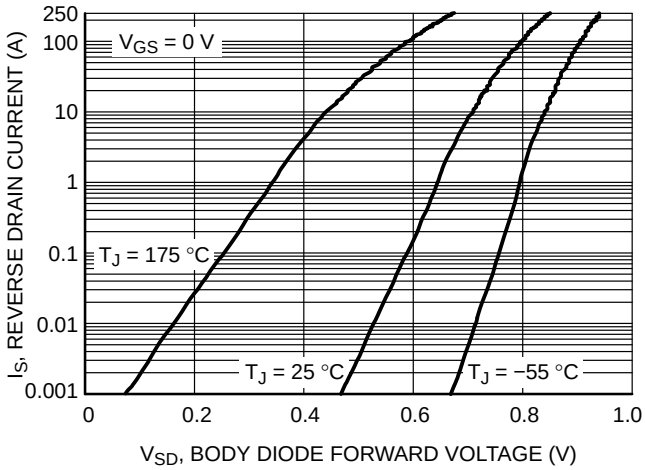

Figure 10. Diode Forward Voltage vs. Current

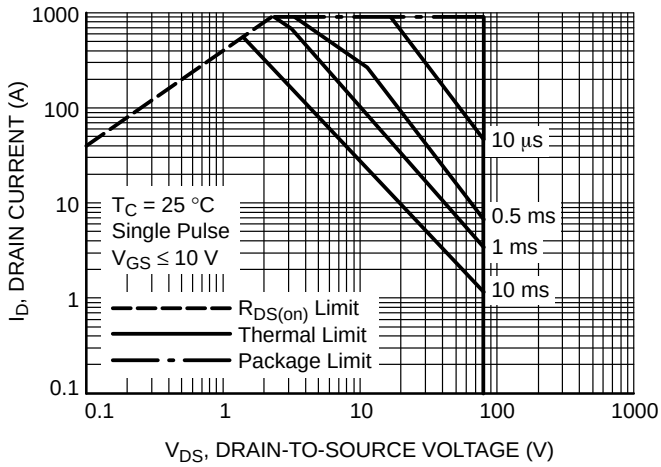

Figure 11. Maximum Rated Forward Biased Safe Operating Area

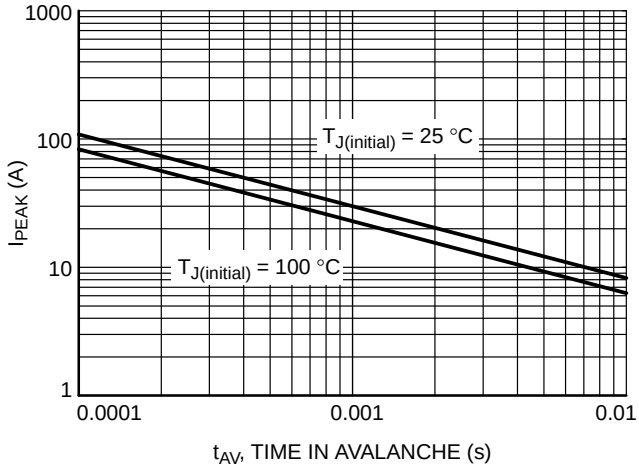

Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

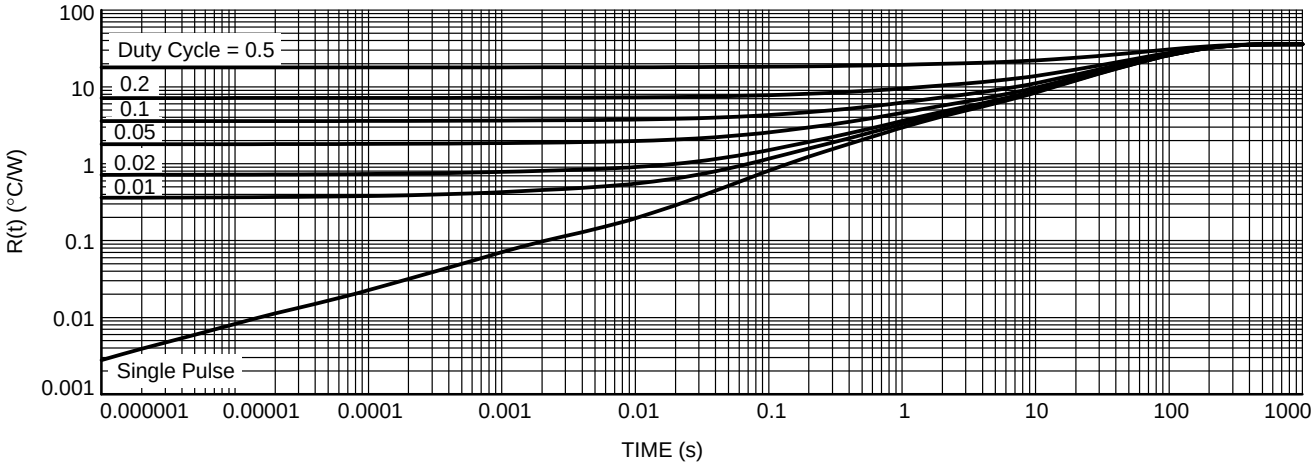

Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVBLS1D1N08H	NVBLS 1D1N08H	M0-299A (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the Data Sheet to **onsemi** format.	10/15/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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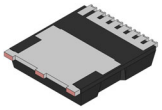
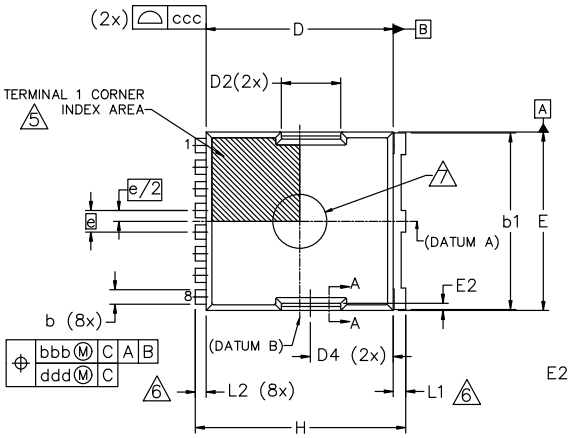
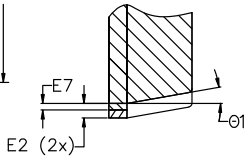


H−PSOF8L 10.38x9.90x2.30, 1.20P
CASE 100CU
ISSUE G

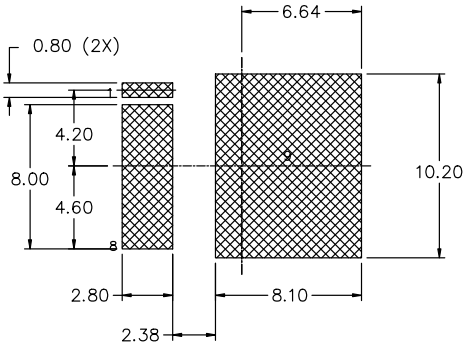
DATE 24 AUG 2026



TOP VIEW

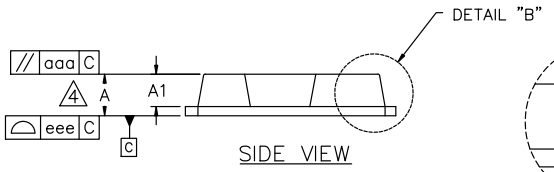


SECTION "A−A"
SCALE: 2X

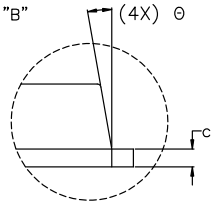


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

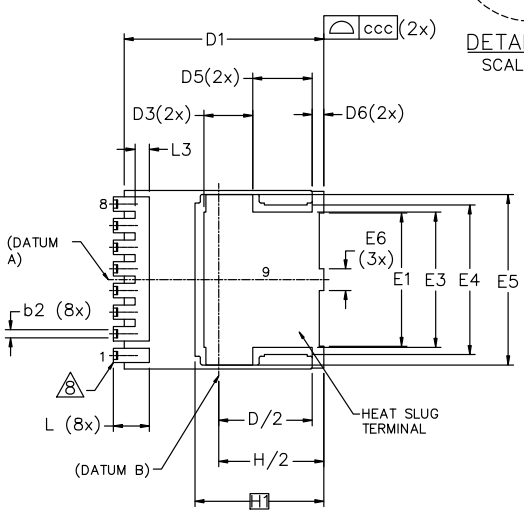


SIDE VIEW



DETAIL "B"
SCALE: 2X

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO−299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. COPLANARITY APPLIES TO EXPOSED PAD AND LEADS..
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



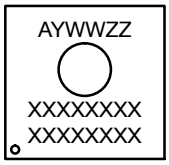
BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	H−PSOF8L 10.38x9.90x2.30, 1.20P	PAGE 1 OF 1

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