EN6340QI 4A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN6340QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter. It integrates the inductor, MOSFET switches, small-signal circuits and compensation in an advanced 4mm x 6mm x 2.5mm 34-pin QFN package.

The EN6340QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architectures. The device's advanced circuit techniques, high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- High Efficiency (Up to 95%)
- Excellent Ripple and EMI Performance
- Up to 4A Continuous Operating Current
- 2.7V to 6.6V Input Voltage Range
- 0.5% V_{FB} Initial Accuracy
- 1.5% V_{OUT} Accuracy (Line, Load, Temp)
- 2MHz Switching Frequency
- 60mm^2 Optimized Total Solution Size
- Programmable Soft-Start
- Power OK Indicator
- Thermal, Over-Current, Short Circuit, Under-Voltage and Pre-Bias Protections
- Pin Compatible with EN6363QI (6A)
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Point of Load Regulation for FPGAs, Distributed Power Architectures, Low-Power ASICs, Multi-Core, Communication Processors and DSPs
- Space Constrained Applications Needing High Power Density
- 5V/3.3V Bus Architectures Needing High Efficiency

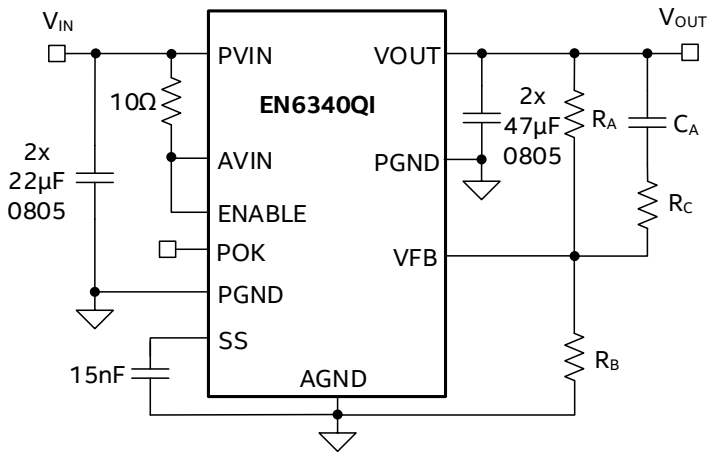


Figure 1: Simplified Applications Circuit

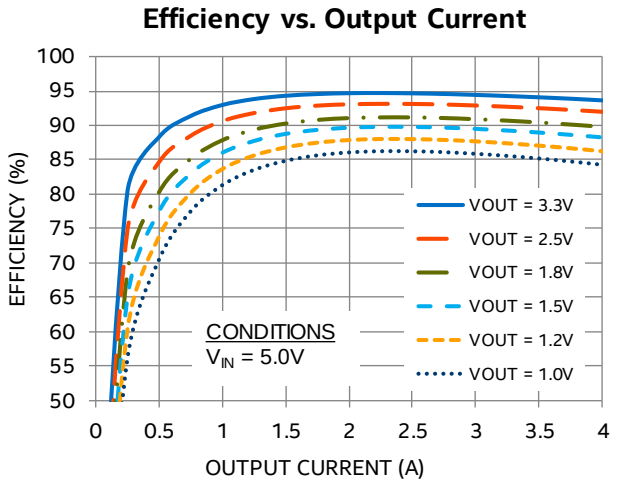


Figure 2: Efficiency at V_{IN} = 5V

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN6340QI	EN6340QI	-40°C to +125°C	34-pin (4mm x 6mm x 2.5mm) QFN
EVB-EN6340QI	EN6340QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

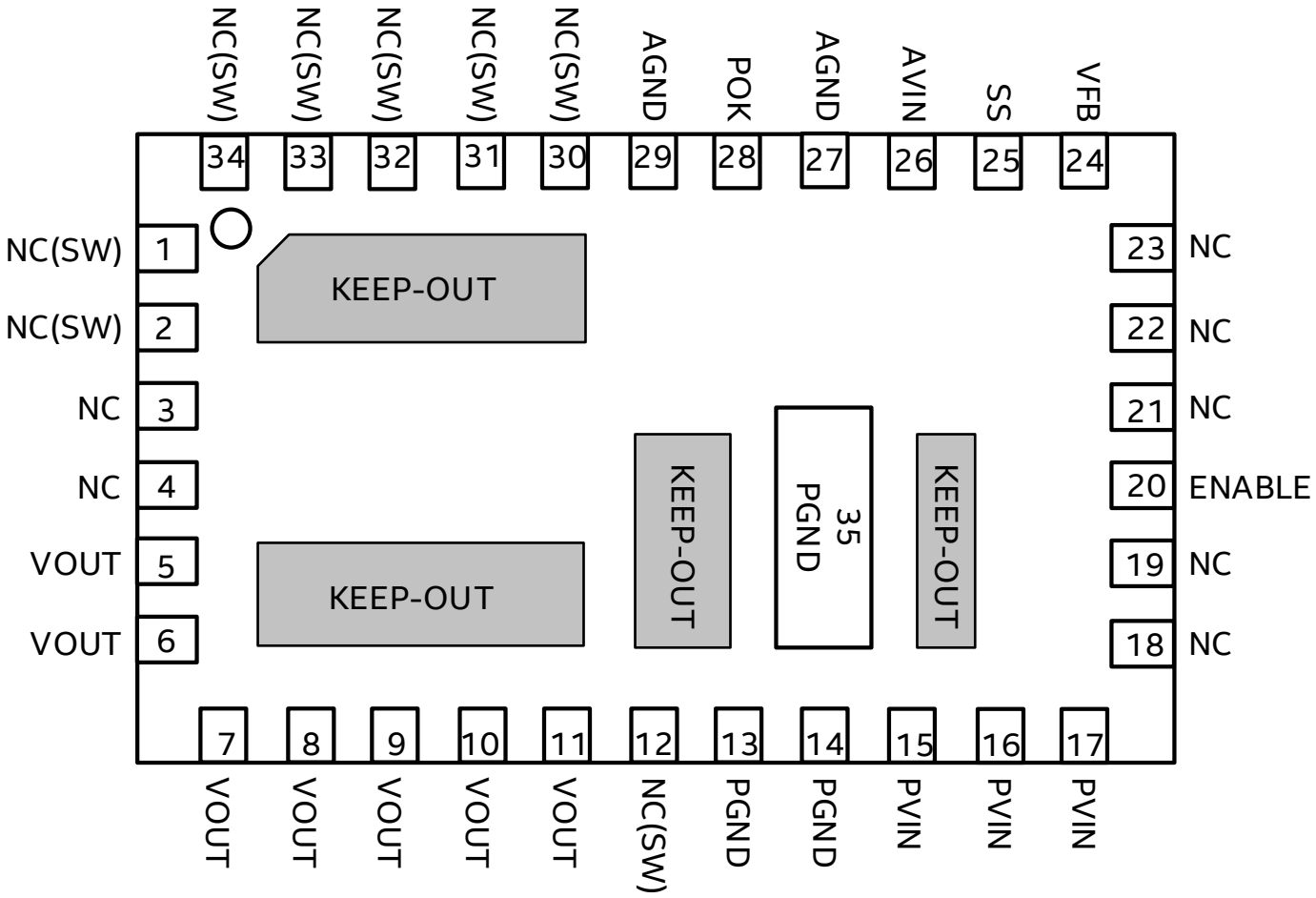


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

NOTE C: Keep-Out are No Connect pads that should not to be electrically connected to each other or to any external signal, ground or voltage. They do not need to be soldered to the PCB.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 2, 12, 30, 31, 32, 33, 34	NC(SW)	-	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
3, 4, 18, 19, 21, 22, 23	NC	-	No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
5, 6, 7, 8, 9, 10, 11	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins. Refer to the Layout Recommendation section.
13, 14	PGND	Ground	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
15, 16, 17	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin. Refer to the Layout Recommendation section.
20	ENABLE	Analog	Input Enable. Applying logic high or floating the ENABLE pin will enable the device and initiate a soft-start. Applying logic low disables the output and switching stops.
24	VFB	Analog	External feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) and resistor (R_C) are required in parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage being equal to 0.6V.
25	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start Operation in the Functional Description section for more details.
26	AVIN	Power	Input power supply for the controller. Connect to input voltage at a quiet point. Refer to the Layout Recommendation section.
27, 29	AGND	Power	Ground for internal control circuits. Connect to the power ground plane with a via right next to the pin.
28	POK	Digital	Power OK is an open drain transistor used for power system state indication. POK is logic high when V_{OUT} is within ±10% of V_{OUT} nominal and has an internal 100kΩ pull-up resistance to AVIN.
35	PGND	Ground	Power ground thermal pad. Not a perimeter pin. Connect thermal pad to the system GND plane for heat-sinking purposes. Refer to the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	7.0	V
ENABLE, POK		-0.3	V_{IN}+0.3	V
VFB, SS		-0.3	2.5	V
NC(SW) Voltage DC	V_{SW}		7.0	V
NC(SW) Voltage Peak < 5ns	V_{SW_PEAK}	-2.0	10.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.7	6.6	V
Output Voltage Range	V_{OUT}	0.6	$V_{IN} - V_{DO}$ (1)	V
Output Current Range	I_{OUT}		4	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	25	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	12.5	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

(1) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = PVIN = AVIN = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN = AVIN	2.7		6.6	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted	2.2	2.3	2.4	V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted	1.7	2.075	2.2	V
Under Voltage Lock-Out Hysteresis	$V_{UVLOHYS}$			225		mV
Shut-Down Supply Current	I_S	ENABLE = 0V		500	700	µA
AVIN Quiescent Current	I_{AVINQ}	AVIN only		3.5	10	mA
No Load Quiescent Current	I_{VINQ}	PVIN and AVIN V_{OUT} = 1.2V		40		mA
Feedback Pin Voltage [3]	V_{FB}	V_{OUT} = 0.6V, I_{LOAD} = 0, T_A =25°C	0.597	0.6	0.603	V
Feedback Pin Voltage (Line, Load, Temp.)	V_{FB}	2.7V ≤ V_{IN} ≤ 6.6V 0A ≤ I_{LOAD} ≤ 4A -40°C ≤ T_A ≤ 85°C	0.591	0.6	0.609	V
Feedback pin Input Leakage Current [4]	I_{FB}	VFB pin input leakage current	-10		10	nA
V_{OUT} Rise Time Range [4]	t_{RISE}	Capacitor programmable	0.2		20	ms
Soft Start Capacitance Range [4]	C_{SS_RANGE}		10		100	nF
Soft-Start Charging Current	I_{SS}		3.5	5	6.5	µA
Drop-Out Voltage [4]	V_{DO}	V_{INMIN} - V_{OUT} at full load		200	320	mV
Drop-Out Resistance [4]	R_{DO}	Input to output resistance		50	80	mΩ
Continuous Output Current	I_{OUT}		0		4	A
Over Current Trip Level	I_{OCP}	V_{IN} = 5V, V_{OUT} = 1.2V	4.5	6.5		A

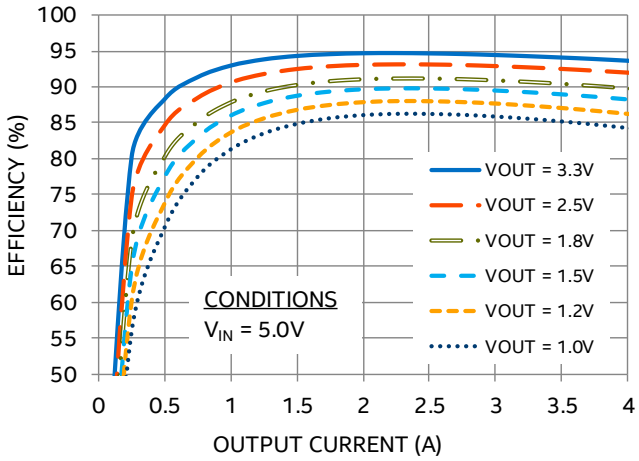
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Retry Time (4)	T_{CL_TRY}			17		ms
Precision Disable Threshold	$V_{DISABLE}$	ENABLE pin logic going low	0.95	1.01	1.07	V
Precision Enable Threshold	V_{EN}	ENABLE pin logic going high	1.08	1.12	1.16	V
ENABLE Hysteresis	EN_{HYS}			110		mV
ENABLE Pin Input Current	I_{EN}	Device not switching; ENABLE pin has ~110kΩ pull down		40	90	µA
ENABLE Pull-Up Resistance	R_{EN_UP}	Not a passive element and changes with VIN		190		kΩ
ENABLE Pull-Down Resistance	R_{EN_DOWN}	Not a passive element and changes with VIN		110		kΩ
Switching Frequency	F_{SW}	Free running frequency of oscillator	1.8	2.0	2.2	MHz
POK High Range	POK_{RANGE}	Typical percentage range within V_{OUT} nominal when POK is asserted high		±10		%
POK Low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK High Voltage	V_{POKH}	$2.7V \le V_{IN} \le 6.6V$			V_{IN}	V
POK Pin Leakage Current (4)	I_{POKH}	POK is high			1	µA

(3) The VFB pin is a sensitive node. Do not touch VFB while the device is in regulation.

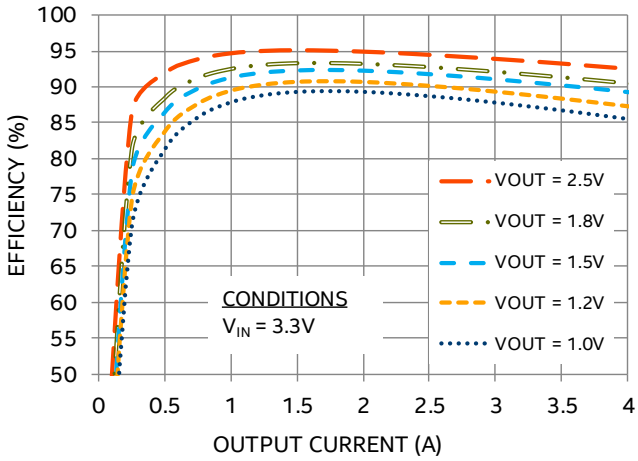
(4) Parameter not production tested but is guaranteed by design.

TYPICAL PERFORMANCE CURVES

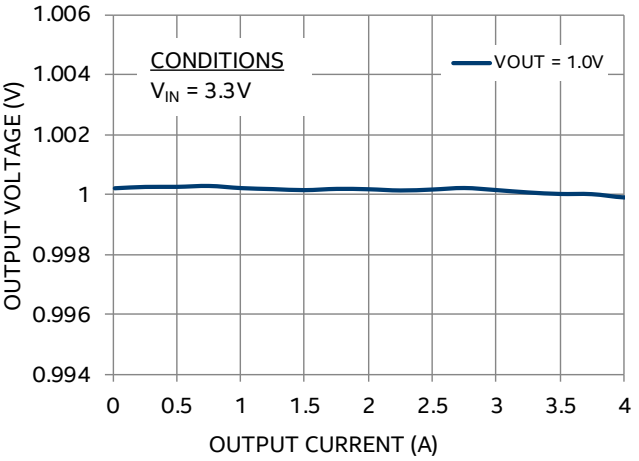
Efficiency vs. Output Current



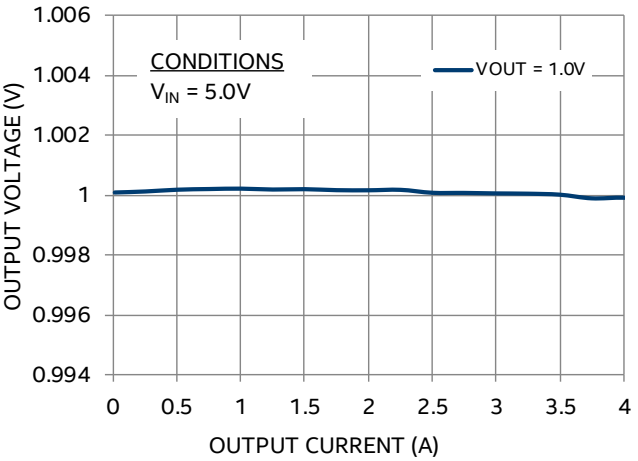
Efficiency vs. Output Current



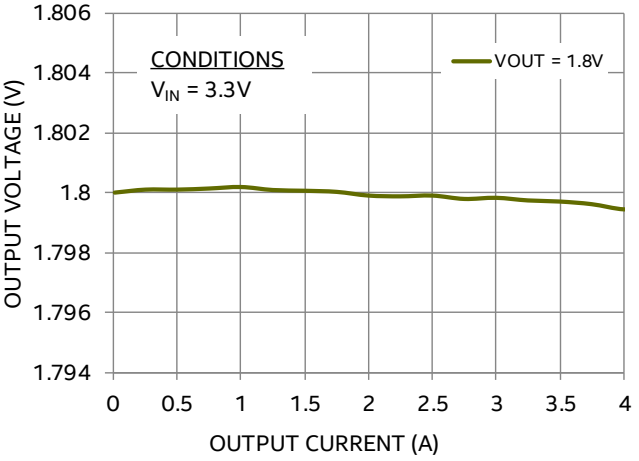
Output Voltage vs. Output Current



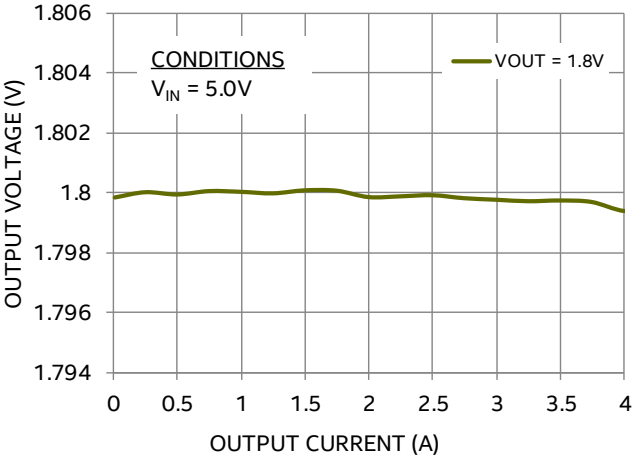
Output Voltage vs. Output Current



Output Voltage vs. Output Current

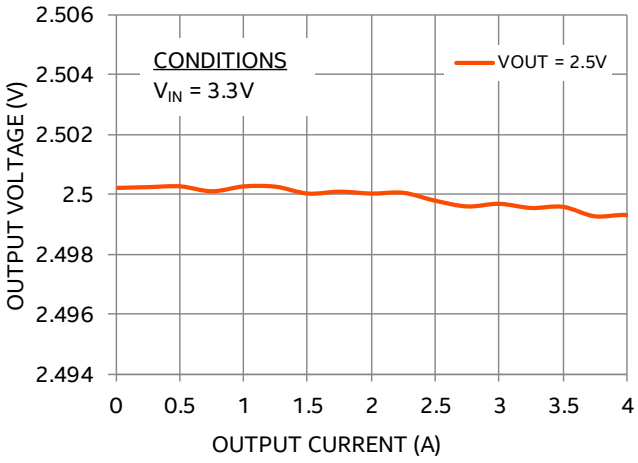


Output Voltage vs. Output Current

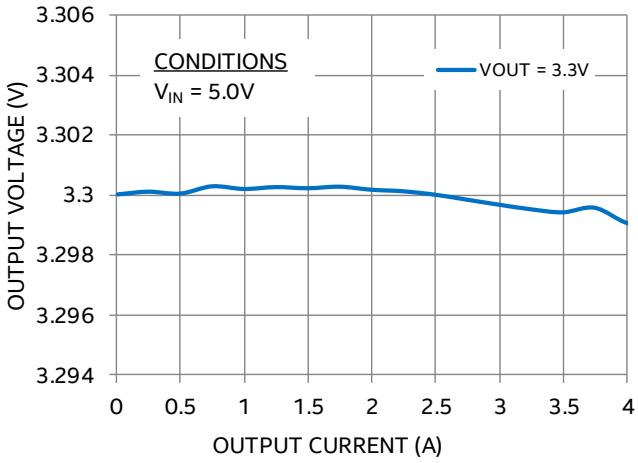


TYPICAL PERFORMANCE CURVES (CONTINUED)

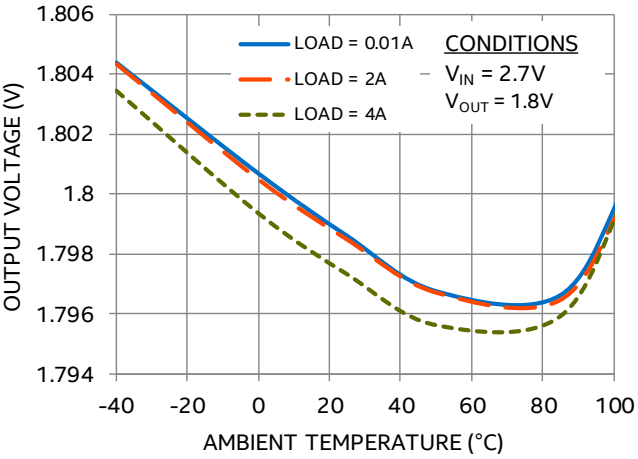
Output Voltage vs. Output Current



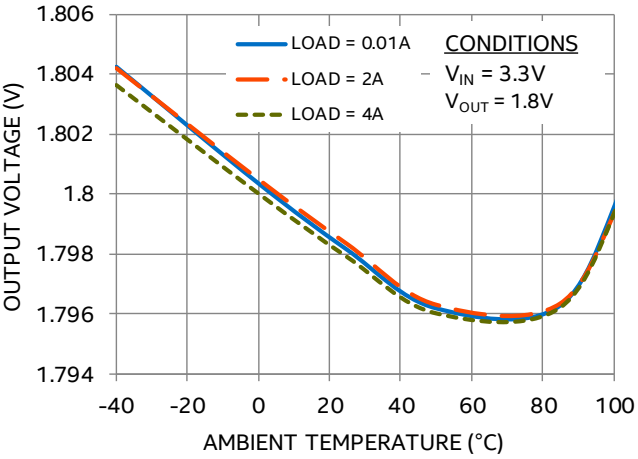
Output Voltage vs. Output Current



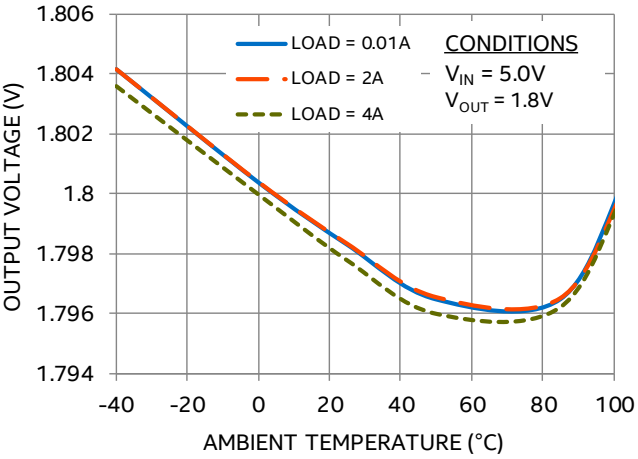
Output Voltage vs. Temperature



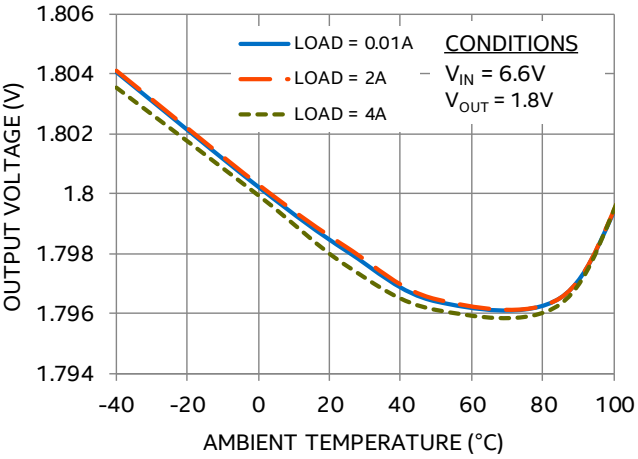
Output Voltage vs. Temperature



Output Voltage vs. Temperature

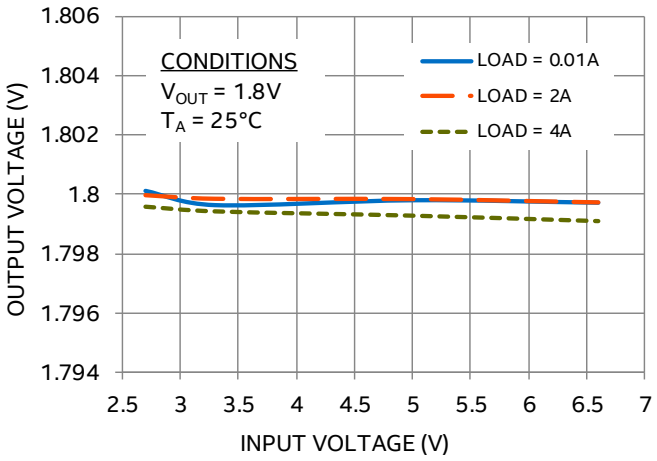


Output Voltage vs. Temperature

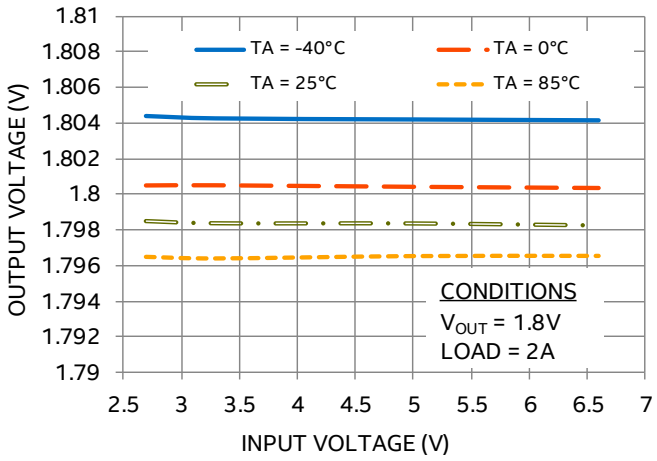


TYPICAL PERFORMANCE CURVES (CONTINUED)

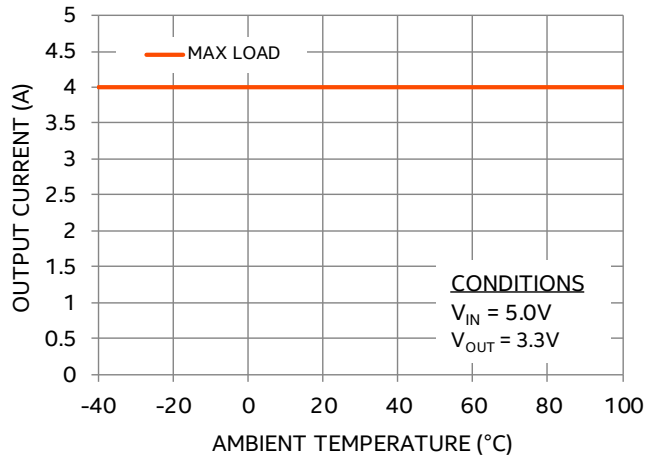
Input Voltage vs. Output Voltage



Input Voltage vs. Output Voltage



No Thermal Derating



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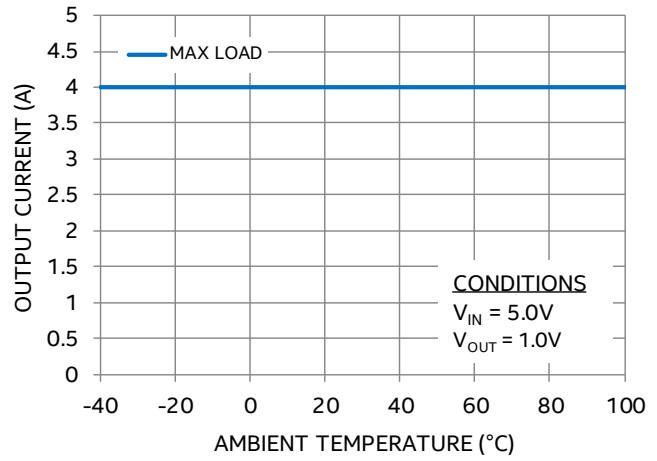
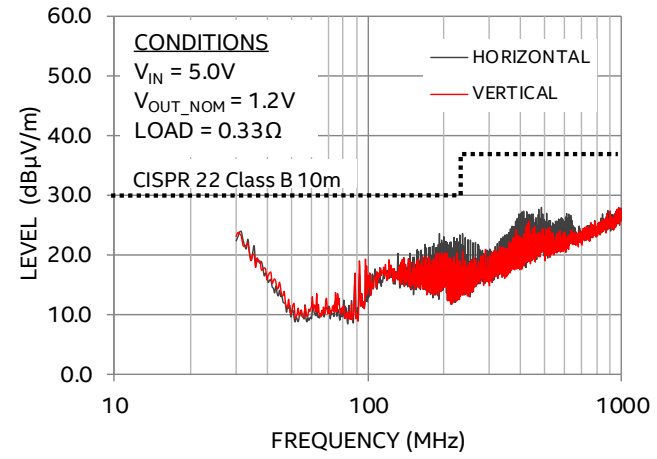


EMI Performance



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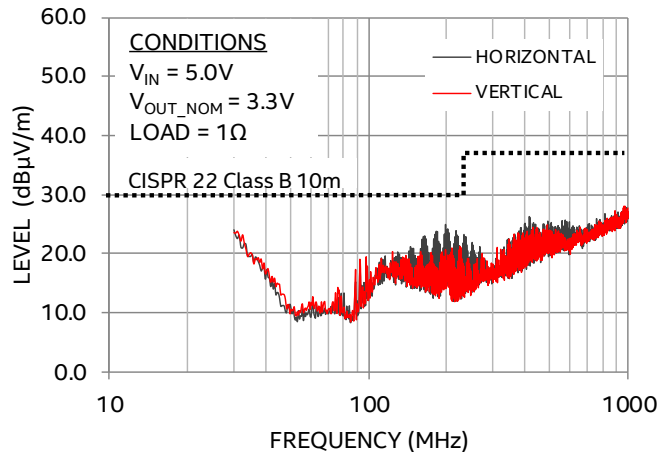
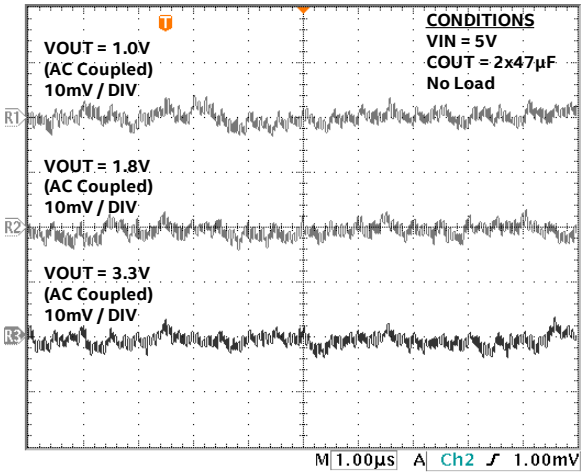
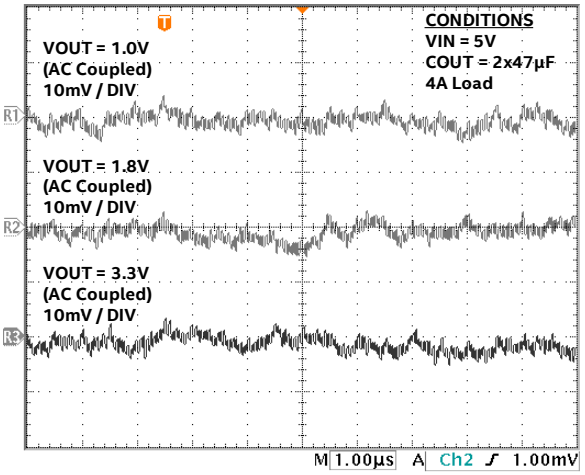


TYPICAL PERFORMANCE CHARACTERISTICS

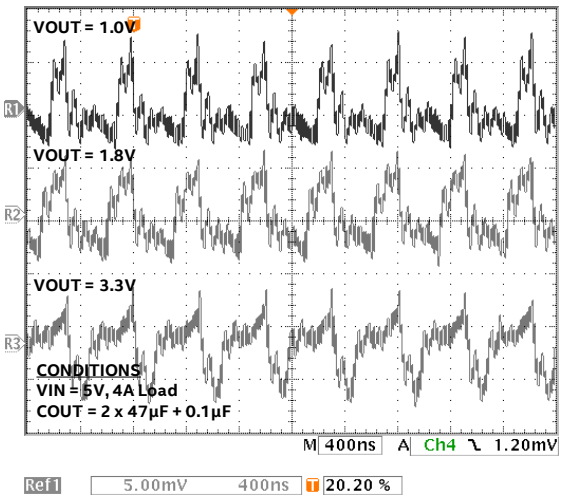
Output Ripple at 20MHz Bandwidth



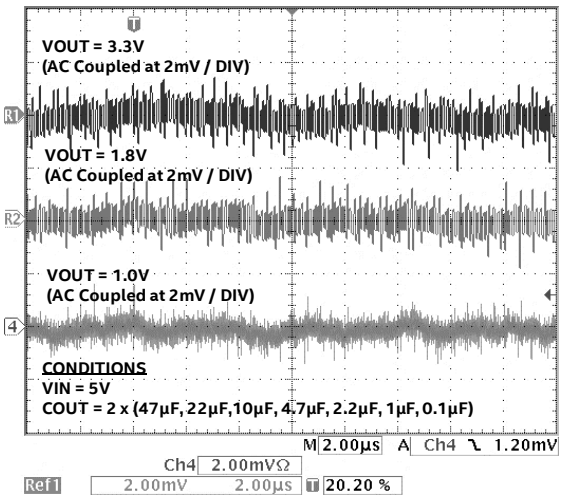
Output Ripple at 20MHz Bandwidth



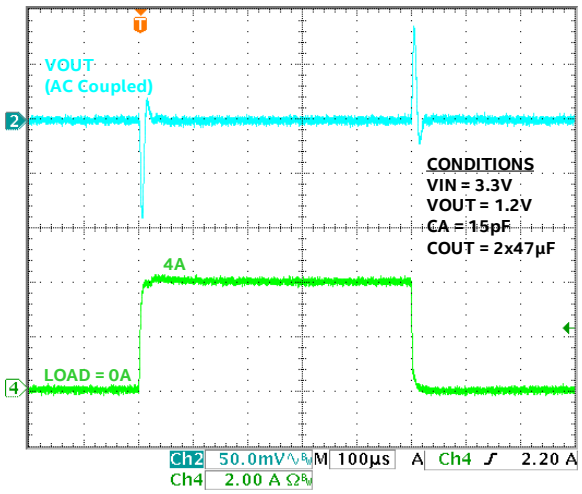
Output Ripple at 500MHz Bandwidth



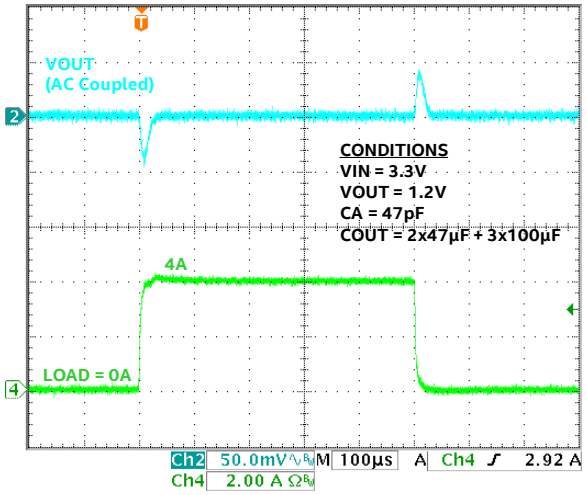
Output Ripple at 500MHz Bandwidth



Load Transient 0 to 4A

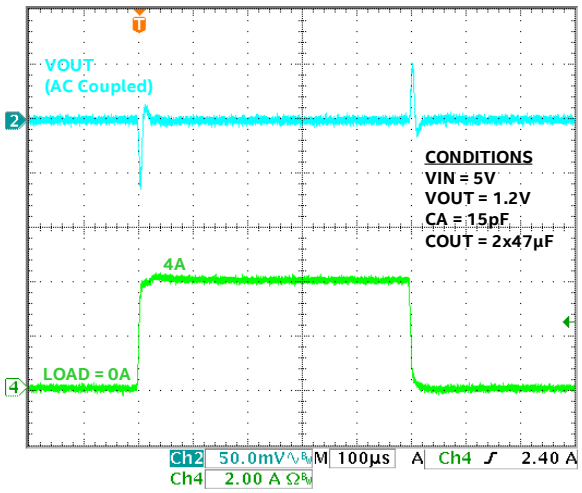


Improved Load Transient 0 to 4A



TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Load Transient 0 to 4A



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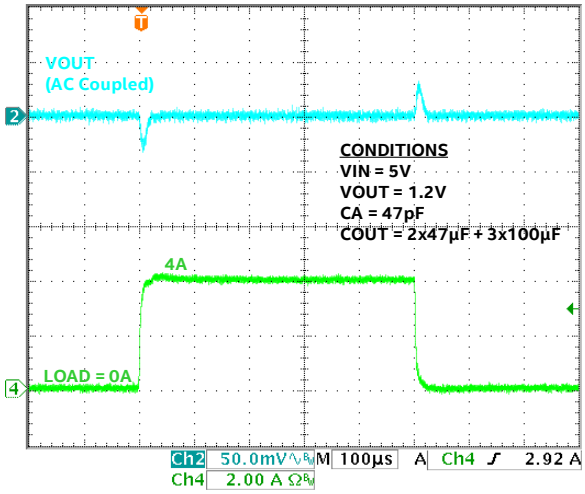
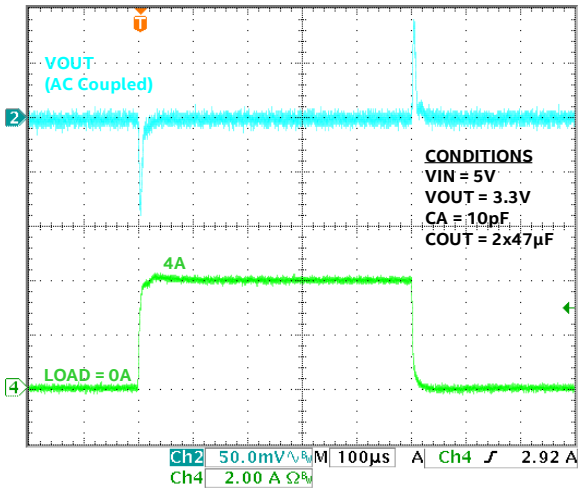


Load Transient 0 to 4A



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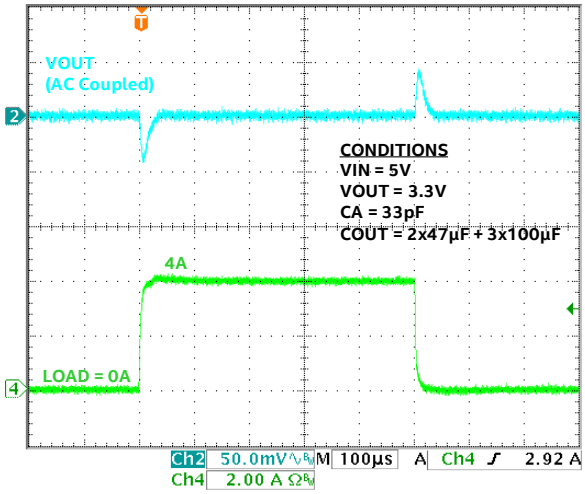
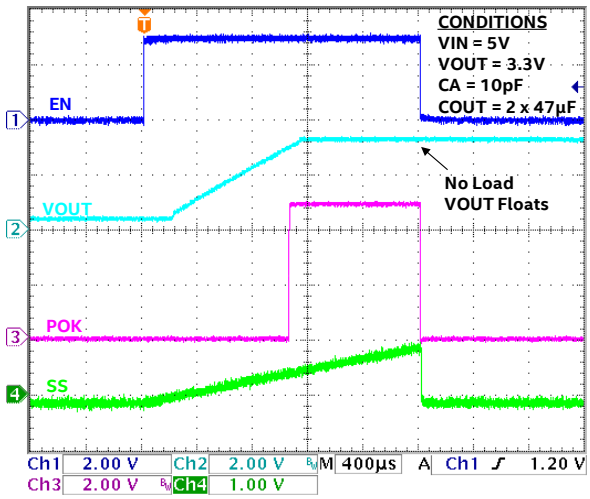
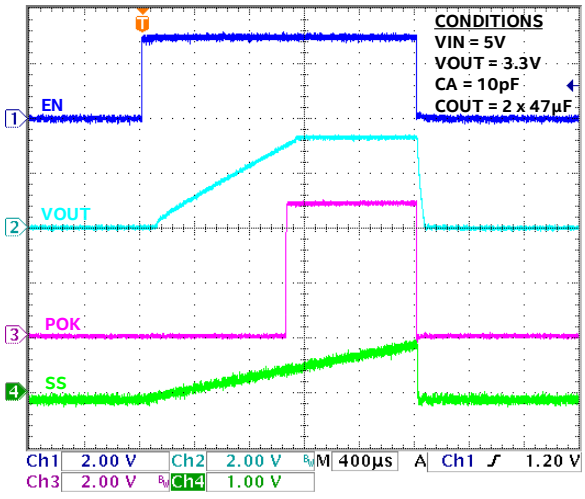


Startup and Shutdown at No Load

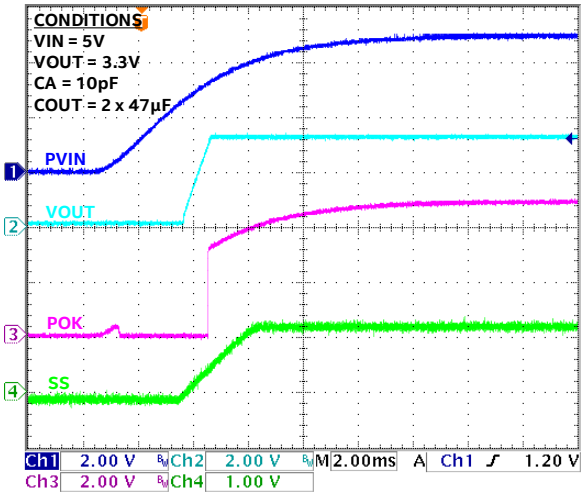


Startup and Shutdown at 4A Load

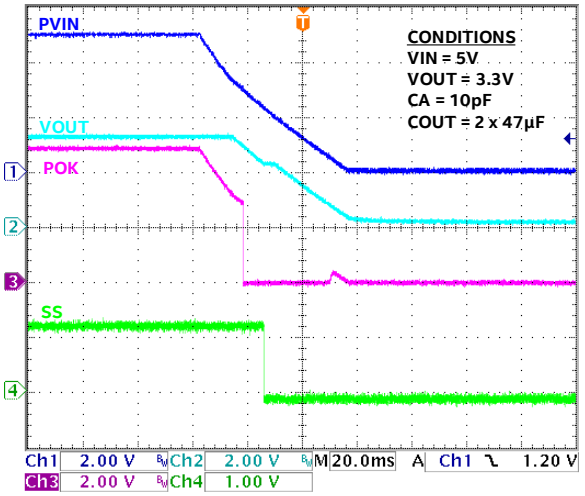


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

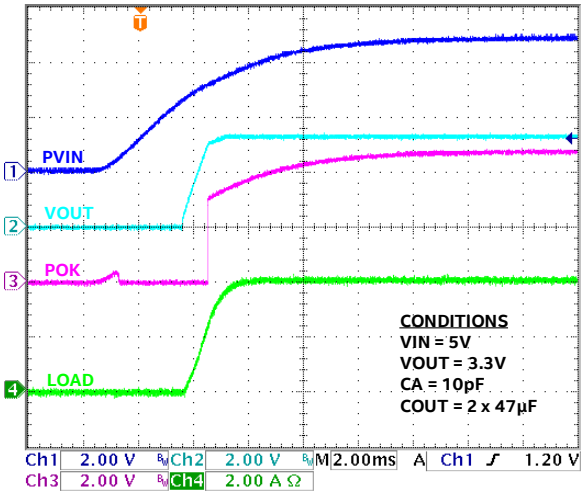
VIN Startup at No Load



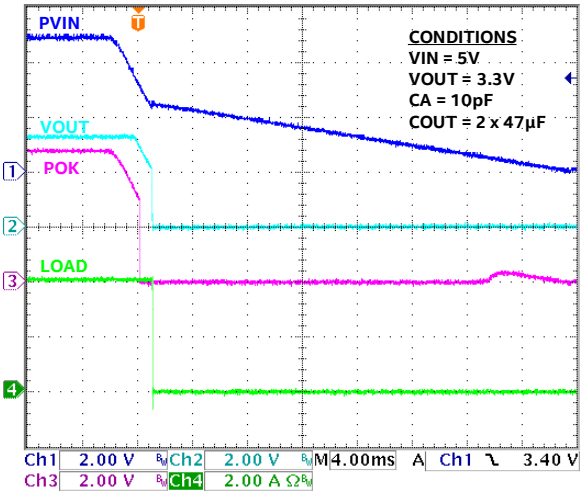
VIN Shutdown at No Load



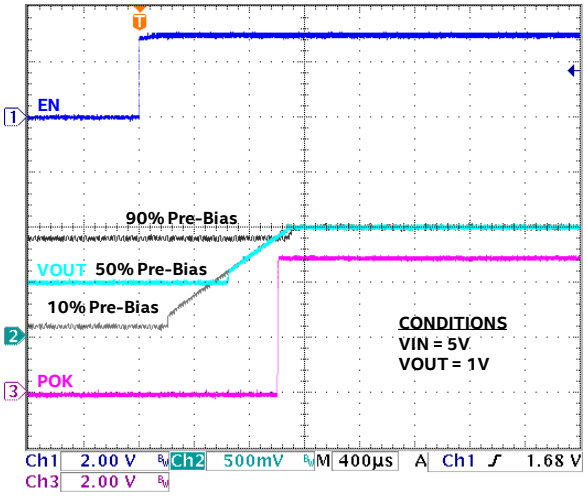
VIN Startup at 4A Load



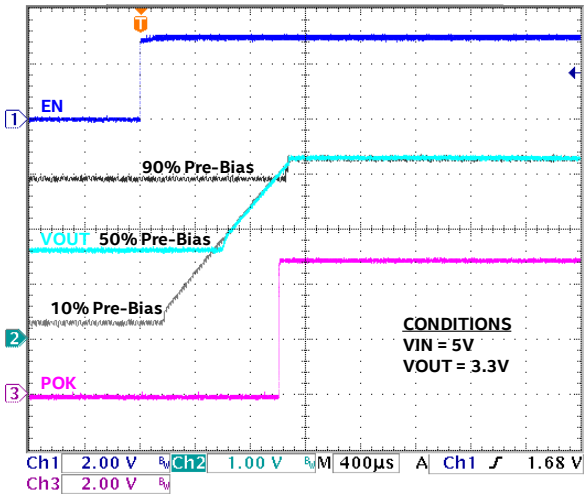
VIN Shutdown at 4A Load



Pre-Bias Startup

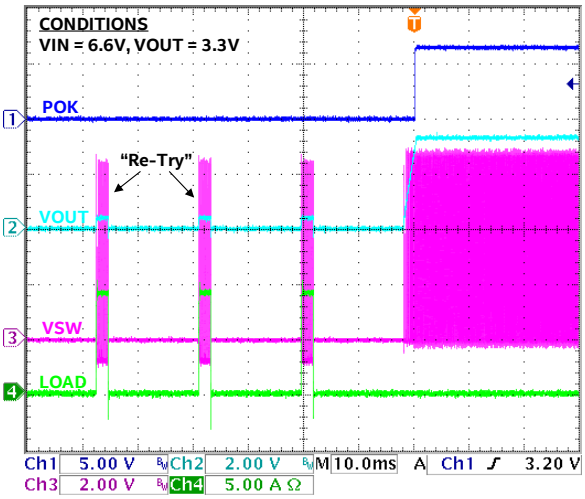


Pre-Bias Startup

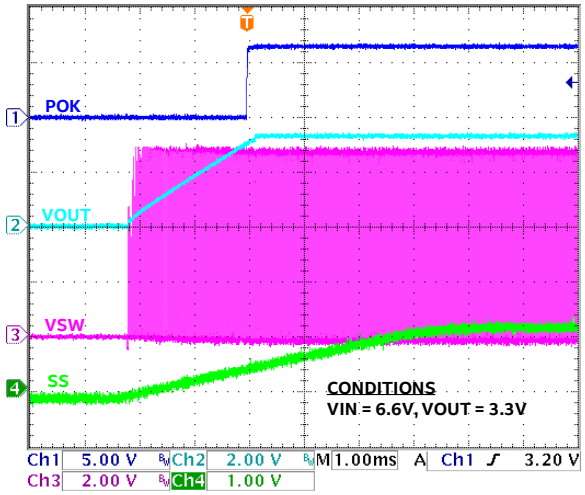


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

Short Circuit and Recovery



Short Circuit and Recovery



FUNCTIONAL BLOCK DIAGRAM

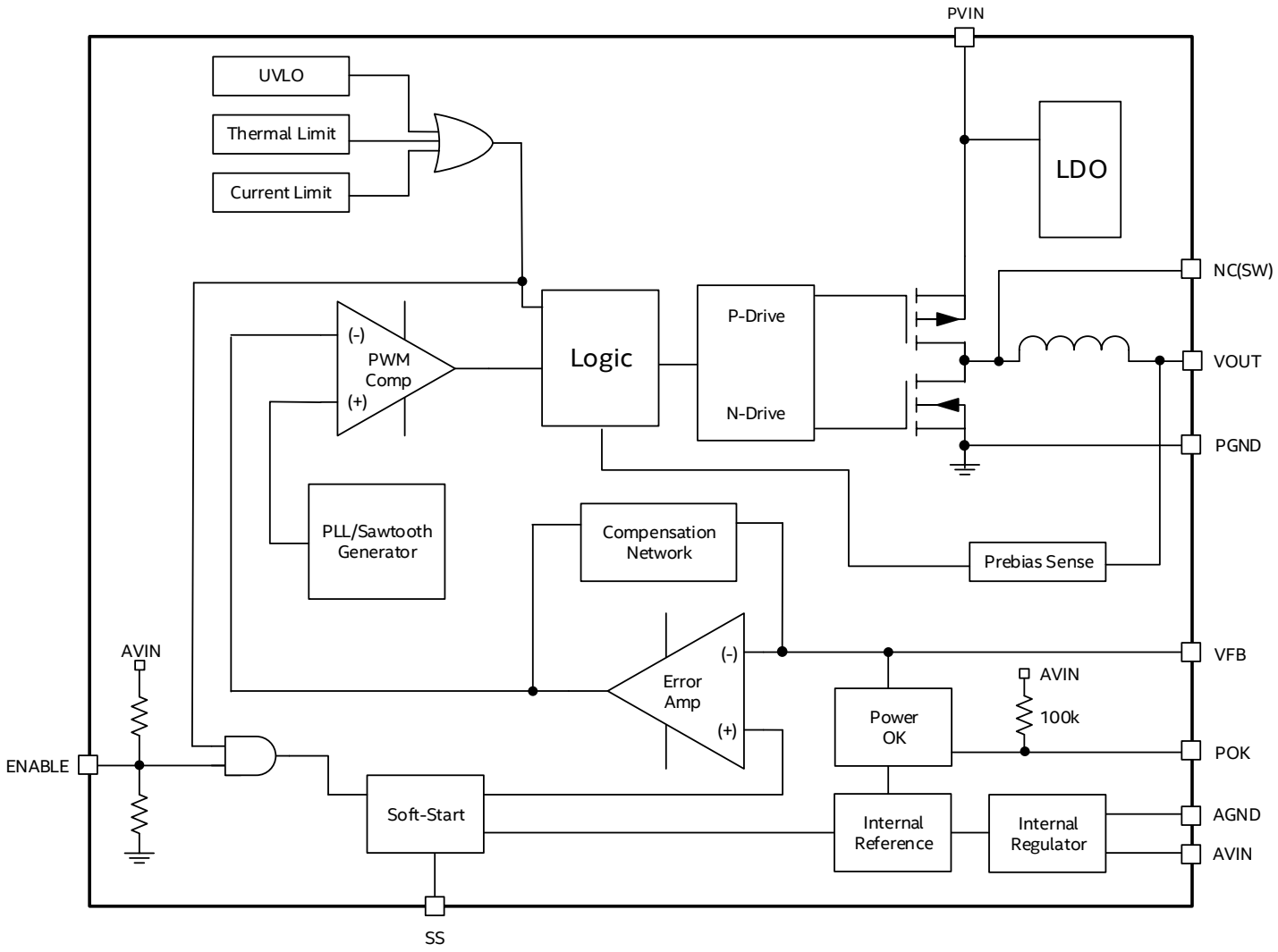


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN6340QI is a synchronous DC-DC PowerSoC with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.7V to 6.6V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device, but a phase-lead capacitor and resistor are required to complete the compensation network. The type III voltage mode architecture with integrated compensation maximizes loop bandwidth without increasing complexity. This architecture is designed to maintain stability with excellent gain and phase margin and improve transient response. The enhanced voltage mode architecture also provides high noise immunity at light load and maintains excellent line and load regulation. Up to 4A of continuous output current can be drawn from this converter. The 2MHz switching frequency allows the use of smaller case size input and output capacitors within a small footprint.

The EN6340QI architecture includes the following features.

Operational Features:

- Precision enable circuit with tight threshold range
- Soft-start circuit allowing controlled startup when the converter is initially powered up
- Power OK circuit indicating the output voltage is greater than 90% of programmed value

Protection Features:

- Over-current protection from short circuit or excessive load current
- Thermal shutdown with hysteresis to prevent over temperature stress
- Output voltage pre-bias startup protection for smooth monotonic startup
- Under-voltage lockout protection to prevent under-voltage operation

Precision Enable Operation

The enable (ENABLE) pin provides a mean to startup or to shutdown the device. When the ENABLE pin is asserted high, the device will undergo a normal soft-start where the output will rise monotonically into regulation. Asserting a logic low on this pin will deactivate the device by turning off the internal power switches and the POK flag will also be pulled low. The ENABLE pin is connected through an internal divider network to AVIN and AGND. If left floating, the ENABLE voltage will be equal to the AVIN voltage and the value set by the divider network ratio (~2.5):

$$V_{EN\ (FLOATING)} \approx AVIN / 2.5$$

The precision enable circuit ensures the device will enable or disable within a tight voltage range for both high or low logic. In order to ensure a known state the ENABLE pin should be pulled high or low. See the Electrical Characteristics Table for technical specifications for the ENABLE pin.

Soft-Start Operation

The soft-start circuitry will reduce inrush current during startup as the regulator charges the output voltage up to nominal level gradually. The output rise time is controlled by the soft-start capacitor, which is placed between the SS pin and the AGND pin. When the part is enabled, the soft-start (SS) current generator charges the SS capacitor in a linear manner. Once the voltage on the SS capacitor reaches 0.6V, the controller selects the intenral bandgap voltage as the reference. The voltage across the SS capacitor will continue ramping up until it reaches around 1.27V. The rise time is defined as the time needed by the output voltage to go from zero to the programmed value. The rise time (t_{RISE}) is given by the following equation:

$$t_{RISE}\ [ms] = C_{ss}\ [nF] \times 0.13$$

With a 10nF soft-start capacitance on the SS pin, the soft-start rise time will be set to 1.3ms. The recommended range for the value of the SS capacitor is between 10nF and 100nF. Note that excessive bulk capacitance on the output can cause an over current event on startup if the soft-start time is too low. Refer to the Compensation and Transient Response section for details on proper bulk capacitance usage.

POK Operation

The Power OK (POK) is an open drain signal (with internal 100kΩ pull-up to AVIN) to indicate if the output voltage is within the specified range. POK is asserted high when the rising output voltage exceeds 90% of the programmed output voltage. For a stronger pull-up, an external resistor may be connected to AVIN. If the

nominal output voltage falls outside the set range (typically 90% to 110% of nominal) the POK signal will be asserted low by an internal 4mA pull-down transistor.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through the topside power PFET. When the sensed current exceeds the over current trip point (see Electrical Characteristics Table), both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. In the event the OCP circuit trips at least 7 consecutive PWM cycles, the device enters a retry mode; the device is disabled for about 17ms and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists. The OCP circuit will disable operation and protect the device from excessive current during operation without compromising the full load capability of the device.

Thermal Protection

The thermal shutdown circuit disables the device operation (switching stops) when the junction temperature exceeds 160°C. When the junction temperature drops by approximately 25°C, the converter will re-start with a normal soft-start. By preventing operation at excessive temperatures, the thermal shutdown circuit will protect the device from overstress.

Pre-Bias Startup Protection

The EN6340QI supports startup into a pre-biased output. A proprietary circuit ensures the output voltage rises from the pre-bias voltage level to the programmed output voltage on startup. During this soft-start period, the voltage rise is monotonic for output voltage range from 0% to 90% of nominal. If the pre-bias voltage is above 90% on startup, there might be a slight dip (~3%) in output voltage before it rises monotonically. If the pre-bias voltage is above 100% of nominal during startup, the device will not switch until the soft-start period is over. Note that when the device begins switching and the pre-bias output voltage is higher than nominal, the bottomside NFET will discharge the output quickly (but limited to 2-cycles to prevent excessive current) to bring the voltage back into regulation. The pre-bias protection circuit is designed to prevent improper behavior on startup regardless of the pre-bias output voltage during soft-start.

Input Under-Voltage Lock-Out (UVLO)

When the device input voltage falls below UVLO, switching is disabled to prevent operation at insufficient voltage levels. During startup, the UVLO circuit ensures that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits are incorporated in order to ensure high noise immunity and prevent a false trigger in the UVLO voltage region.

APPLICATION INFORMATION

Output Voltage Setting

The EN6340QI output voltage is programmed using a simple resistor divider network (R_A and R_B). Figure 5 shows the resistor divider configuration.

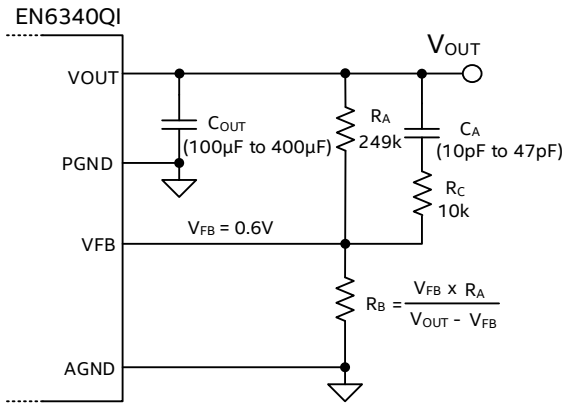


Figure 5: V_{OUT} Resistor Divider & Compensation Capacitor

The recommended R_A resistor value is 249kΩ and the feedback voltage is typically 0.6V. Depending on the output voltage (V_{OUT}), the R_B resistor value may be calculated as shown in Figure 5. Since the accuracy of the output voltage setting is dependent upon the feedback voltage and the external ressitors, 1% or better resistors are recommended. The external compensation capacitor (C_A) and resistor (R_C) is also required in parallel with R_A. Depending on input and output voltage, the recommended external compensation values are shown in Table 1.

Table 1: External Compensation Recommendations

V_{IN}	V_{OUT}	R_B	C_A	R_A	R_C	C_{OUT} (0805)
3.3V	0.6V	OPEN	18pF	249kΩ	10kΩ	2 x 47µF
	0.9V	498kΩ	18pF			
	1.0V	374kΩ	18pF			
	1.2V	249kΩ	15pF			
	1.5V	165kΩ	15pF			
	1.8V	124kΩ	15pF			
	2.5V	78.7kΩ	12pF			
5V	0.6V	OPEN	15pF	249kΩ	10kΩ	2 x 47µF
	0.9V	498kΩ	15pF			
	1.0V	374kΩ	15pF			
	1.2V	249kΩ	15pF			
	1.5V	165kΩ	15pF			
	1.8V	124kΩ	12pF			
	2.5V	78.7kΩ	12pF			
	3.3V	54.9kΩ	10pF			

Compensation and Transient Response

The EN6340QI uses an enhanced type III voltage mode control architecture. Most of the compensation is internal, which simplifies the design. In some applications, improved transient performance may be desired with additional output capacitors (C_{OUT}). In such an instance, the phase-lead capacitor (C_A) can be adjusted depending on the total output capacitance. Using Table 1 as the reference for C_A, if C_{OUT} is increased, then the C_A should also be increased. The relationship is linearly shown below:

$$\Delta C_{OUT} \approx +100\mu F \rightarrow \Delta C_A \approx +10pF$$

As C_{OUT} increases and the C_A value is adjusted, the device bandwidth will reach its optimization level (at around $1/10^{th}$ of the switching frequency). As shown in Table 1, the recommended C_A value is lower for the 5V input than 3.3V input. This is to ensure that the loop bandwidth is not over extended due to the increased gain at the higher input voltage range. The C_A value may be extrapolated for other input voltages. The limitation for adjusting the compensation is based on diminished return. Further adjustments by increasing C_{OUT} and increasing C_A may not yield better transient response or in some situations cause lower gain and phase margin. Over compensating with excessive output capacitance may also cause the device to trigger current limit on startup due to the energy required to charge the output up to regulation level. Due to such limitations, the recommended maximum output capacitance (C_{OUT_MAX}) is 400µF and the recommended maximum phase-lead capacitance (C_{A_MAX}) is 47pF.

Input Capacitor Selection

The input of synchronous buck regulators can be very noisy and should be decoupled properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. The EN6340QI requires a minimum of 2 x 22µF 0805 input capacitors. As the distance of the input power source to the input of the EN6340QI is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Table 2: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
22µF ±20%, 10V X5R, 0805	Taiyo Yuden	LMK212BBJ226MG-T
	Murata	GRM21BR61A226ME51
	TDK	C2012X5R1A226M125AB

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency and output decoupling. The EN6340QI requires a minimum of 2 x 47µF 0805 output capacitors. Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Table 3: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
47µF ±20%, 6.3V, X5R, 0805	Taiyo Yuden	JMK212BBJ476MG-T
	Murata	GRM21BR60J476ME15
	TDK	C2012X5R0J476M125AC

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance (ESR) and effective series inductance (ESL):

$$Z = ESR + ESL$$

The resonant frequency of a ceramic capacitor is inversely proportional to the capacitance. Lower capacitance corresponds to higher resonant frequency. When two capacitors are placed in parallel, the benefit of both are combined. It is beneficial to decouple the output with capacitors of various capacitance and size. Placing them all in parallel reduces the impedance and will hence result in lower output ripple.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

THERMAL CONSIDERATIONS

Thermal considerations are important elements of power supply design. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be taken into account. The Intel Enpirion PowerSoC technology helps alleviate some of those concerns.

The EN6340QI DC-DC converter is packaged in a 4mm x 6mm x 2.5mm 34-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 160°C.

The following example and calculations illustrate the thermal performance of the EN6340QI with the following parameters:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 4A

First, calculate the output power.

$P_{OUT} = V_{OUT} \times I_{OUT} = 3.3V \times 4A = 13.2W$

Next, determine the input power based on the efficiency (η) shown in Figure 6.

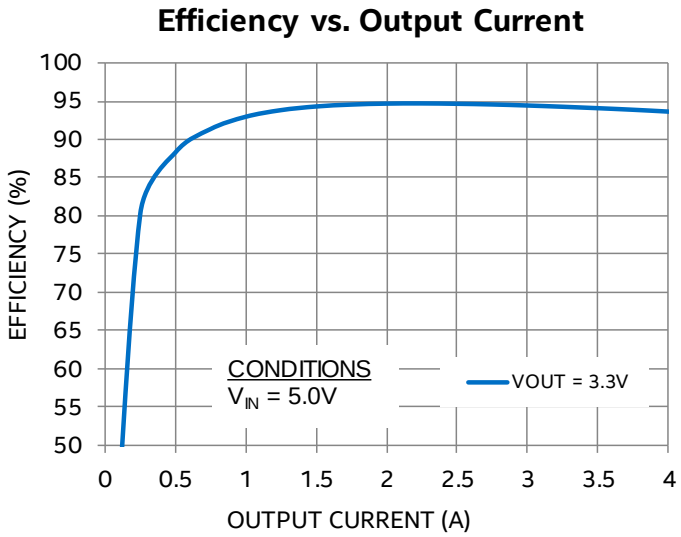


Figure 6: Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 4A, η ≈ 94%

$\eta = P_{OUT} / P_{IN} = 94\% = 0.94$

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 13.2W / 0.94 \approx 14W$

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D = P_{IN} – P_{OUT}$

$= 14W – 13.2W \approx 0.8W$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN6340QI has a θ_{JA} value of 12.5°C/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

$\Delta T = P_D \times \theta_{JA}$

$\Delta T \approx 0.8W \times 12.5°C/W \approx 10°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 10°C \approx 35°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} – P_D \times \theta_{JA}$

$\approx 125°C – 10°C \approx 115°C$

The maximum ambient temperature the device can reach is 115°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUITS

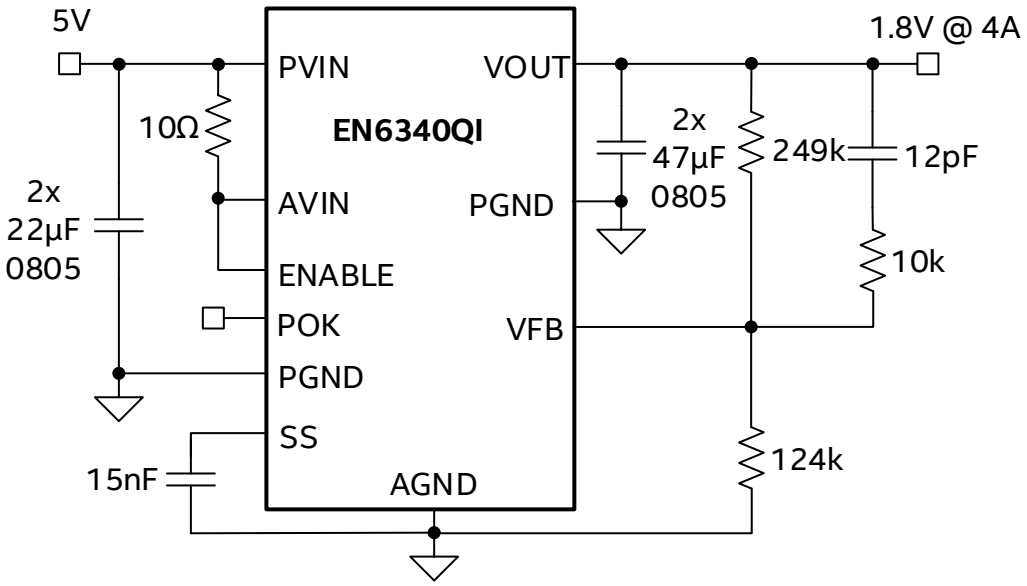


Figure 7: Smallest Solution Size Application Circuit for V_{OUT} = 1.8V

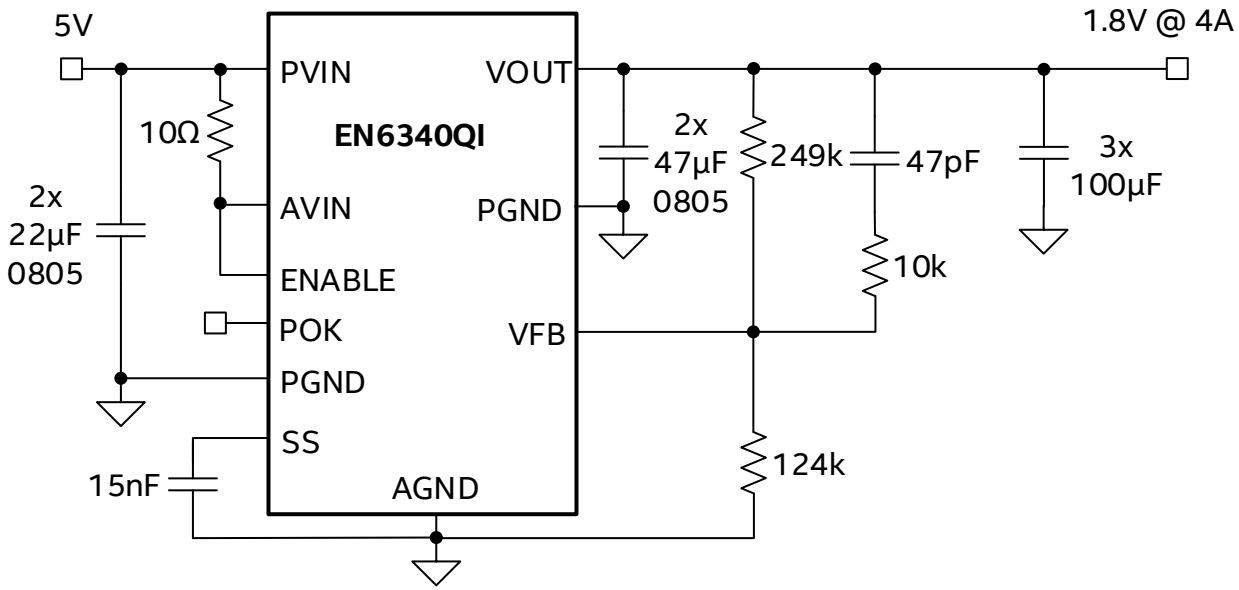


Figure 8: Improved Transient Response Application Circuit for V_{OUT} = 1.8V

LAYOUT RECOMMENDATIONS

Figure 9 shows critical components and layer 1 traces of a recommended minimum footprint EN6340QI layout. ENABLE and other small signal pins need to be connected and routed according to specific customer application. Visit the Enpirion Power Solutions website at www.altera.com/powersoc for more information regarding layout. Please refer to this Figure 9 while reading the layout recommendations in this section.

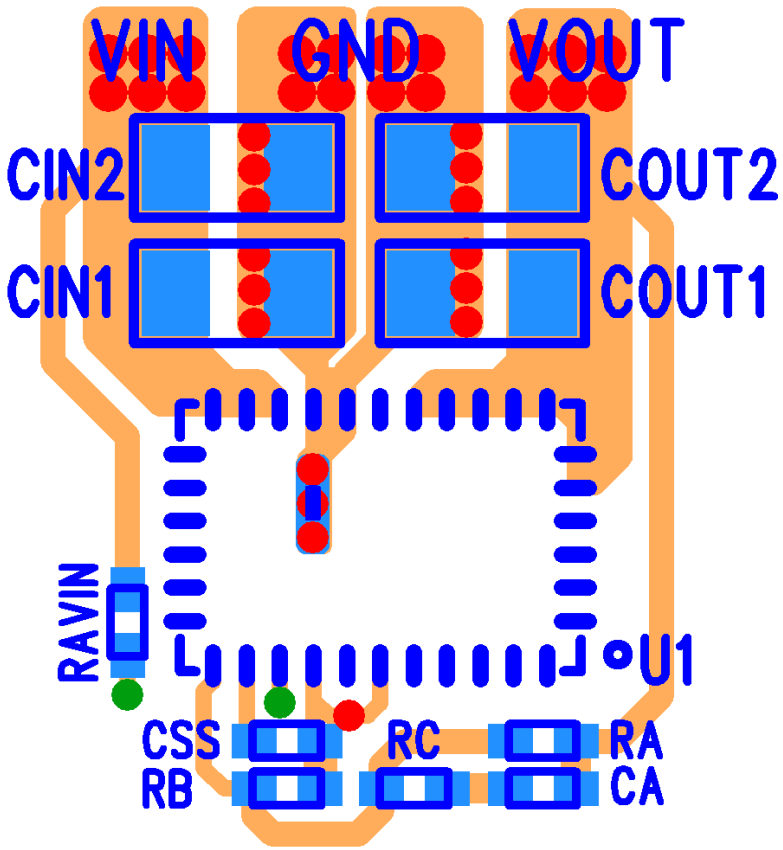


Figure 9: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6340QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the EN6340QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Half of the PGND pins are dedicated to the input circuit and the other half to the output circuit. The slit shown in Figure 9 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be on the 2nd layer (below the surface layer). This ground plane should be continuous and un-interrupted.

Recommendation 4: The large thermal pad underneath the device must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figure 9.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. Put the vias under the capacitors along the edge of the GND copper closest to the Voltage copper. Please see Figure 9. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 9 this connection is made at the input capacitor furthest from the PVIN pin and on the input source side. Avoid connecting AVIN near the PVIN pin even though it is the same node as the input ripple is higher there.

Recommendation 7: The V_{OUT} sense point should be connected at the last output filter capacitor furthest from the VOUT pins. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 8: Keep R_A, C_A, R_C and R_B close to the VFB pin (see Figure 9). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane. The AGND should connect to the PGND at a single point from the AGND pin to the PGND plane on the 2nd layer.

Recommendation 9: The layer 1 metal under the device must not be more than shown in Figure 9. See the following section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance such as in reduced electrical lead resistance and in overall footprint; however, they do require some special considerations.

In the assembly process lead frame construction requires some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached for mechanical support. This results in several small pads being exposed on the bottom of the package, as shown in Figure 10.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the board. The PCB top layer under the EN6340QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 10 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by solder mask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. See Figure 11 for details.

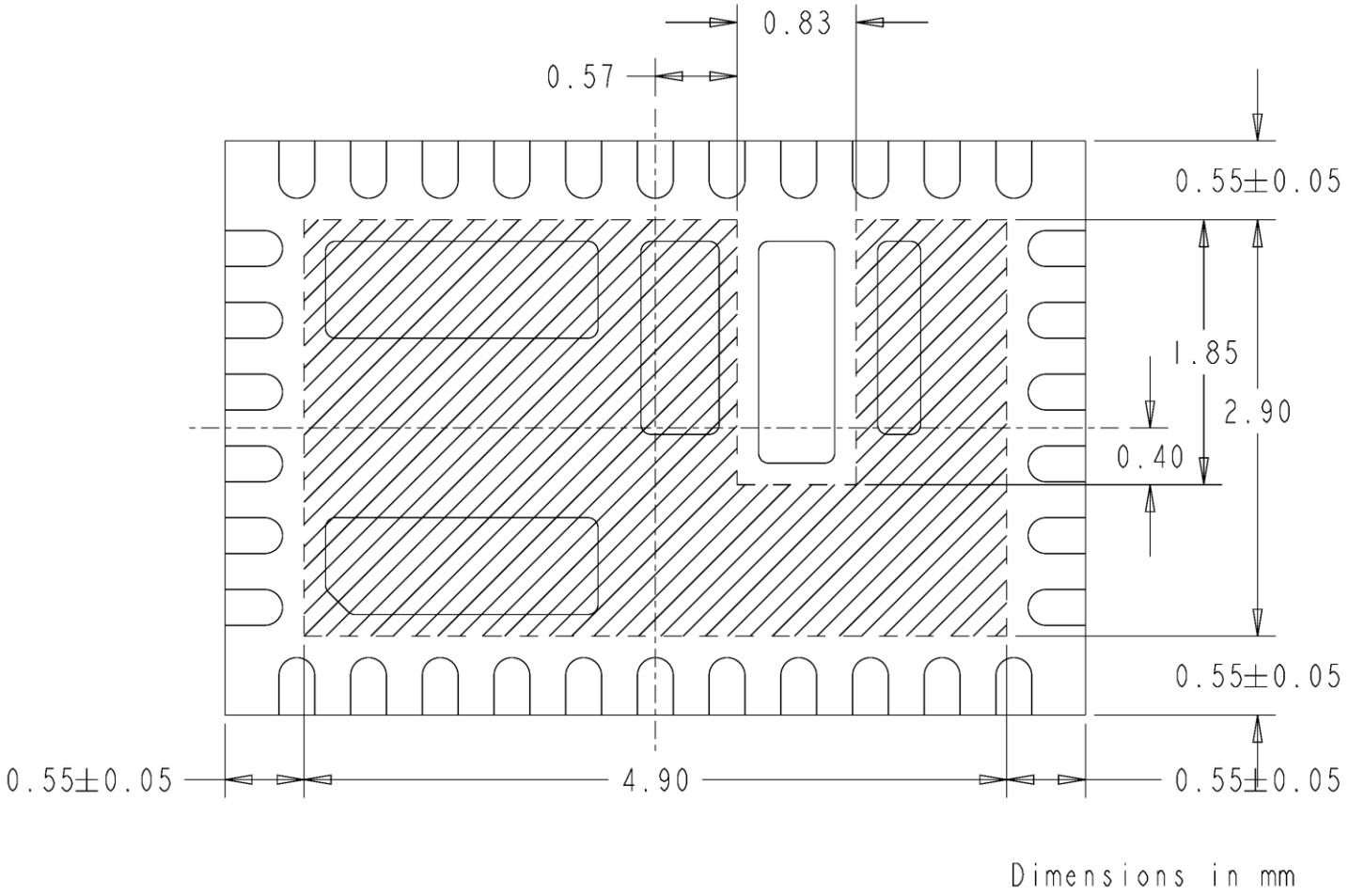


Figure 10: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

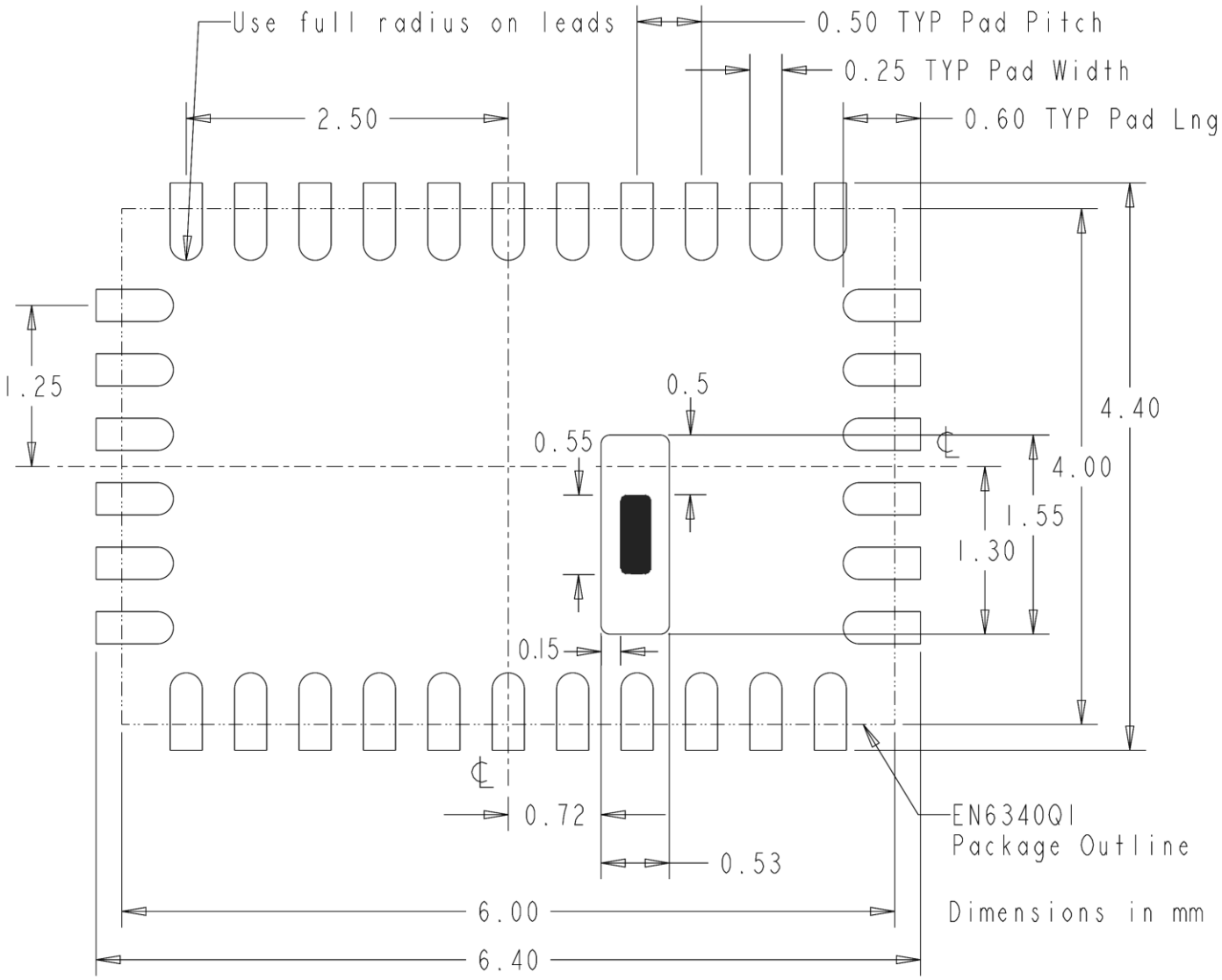


Figure 11: Landing Pattern with Solder Stencil (Top View)

The solder stencil aperture for the thermal PGND pad is shown in Figure 11 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

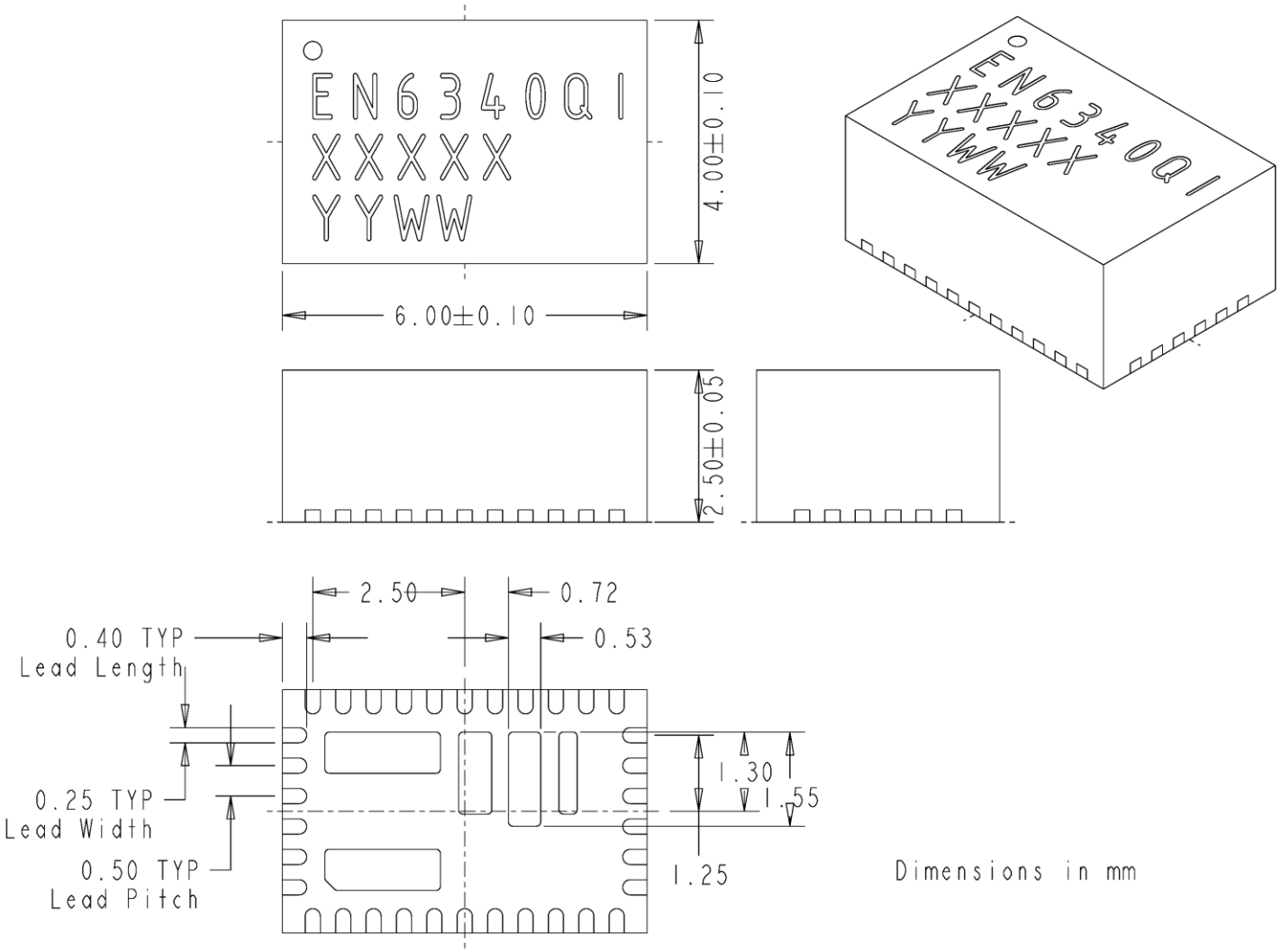


Figure 12: EN6340QI Package Dimensions

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
A	July, 2017	Initial Release
B	Aug, 2017	Updated EMI Performance Curves on page 10 from 3m to 10m
C	March, 2018	Updated minimum operating VOUT to 0.6V from 0.75V
D	August, 2018	Updated RB value in Table 1 for 0.9V from 590k to 498k

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion